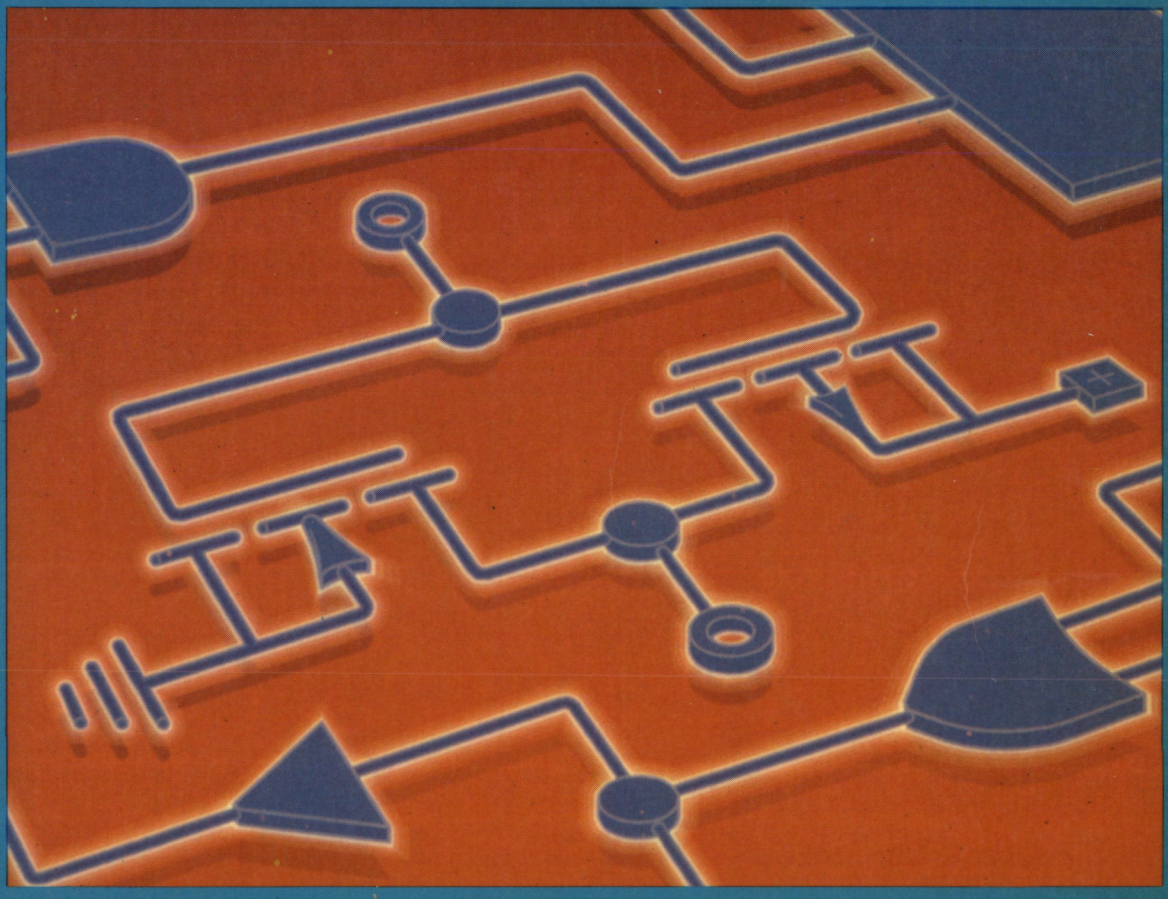
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MOTOROLA Semiconductors



CMOS LOGIC DATA

Master Index 1

Product Selection Guide
Equivalent Gate Count 2

The "Better" Program 3

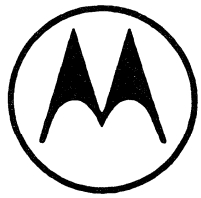
B and UB Series Family Data 4

CMOS Handling and Design Guidelines 5

Data Sheets 6

CMOS Reliability 7

Package Dimensions 8



MOTOROLA

CMOS LOGIC DATA

Prepared by
Technical Information Center

This book presents technical data for the broad line of CMOS logic integrated circuits and demonstrates Motorola's continued commitment to Metal-Gate CMOS. Complete specifications are provided in the form of data sheets. In addition, a Product Selector Guide and a Handling and Design Guidelines chapter have been included to familiarize the user with these circuits.

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Master Index 1

1

MASTER INDEX

This index includes Motorola's entire MC14000 series CMOS products, although this book contains data sheets for Logic Devices only. Data sheets for devices in other books are designated in the page number column as:

SF — See DL130, CMOS/NMOS Special Functions Data
Telecom — See DL136, Telecommunications Data
MCU — See DL132R1, Single-Chip Microcomputer Data
MPU — See DL133, 8-Bit Microprocessor and Peripheral Data

Device Number MC	Description	Page Number
14000UB	Dual 3-Input NOR Gate Plus Inverter	6-3
14001B	Quad 2-Input NOR Gate	6-6
14001UB	Quad 2-Input NOR Gate	6-15
14002B	Dual 4-Input NOR Gate	6-20
14002UB	Dual 4-Input NOR Gate	6-20
14006B	18-Bit Static Shift Register	6-21
14007UB	Dual Complementary Pair Plus Inverter	6-25
14008B	4-Bit Full Adder	6-29
14011B	Quad 2-Input NAND Gate	6-35
14011UB	Quad 2-Input NAND Gate	6-35
14012B	Dual 4-Input NAND Gate	6-36
14012UB	Dual 4-Input NAND Gate	6-36
14013B	Dual D Flip-Flop	6-37
14014B	8-Bit Static Shift Register	6-41
14015B	Dual 4-Bit Static Shift Register	6-45
14016B	Quad Analog Switch/Multiplexer	6-51
14017B	Decade Counter	6-58
14018B	Presettable Divide-by-N Counter	6-63
14020B	14-Bit Binary Counter	6-67
14021B	8-Bit Static Shift Register	6-71
14022B	Octal Counter	6-72
14023B	Triple 3-Input NAND Gate	6-77
14023UB	Triple 3-Input NAND Gate	6-77
14024B	7-Stage Ripple Counter	6-78
14025B	Triple 3-Input NOR Gate	6-83
14025UB	Triple 3-Input NOR Gate	6-83
14027B	Dual J-K Flip-Flop	6-84
14028B	BCD-to-Decimal/Binary-to-Octal Decoder	6-88
14029B	Presettable Binary/BCD Up/Down Counter	6-93
14032B	Triple Serial Adder (Positive Logic)	6-99

Device Number MC	Description	Page Number
14034B	8-Bit Universal Bus Register	6-104
14035B	4-Bit Shift Register	6-111
14038B	Triple Serial Adder (Negative Logic)	6-115
14040B	12-Bit Binary Counter	6-116
14042B	Quad Transparent Latch	6-120
14043B	Quad NOR R-S Latch	6-124
14044B	Quad NAND R-S Latch	6-124
14046B	Phase-Locked Loop	SF
14049UB	Hex Inverting Buffer	6-128
14050B	Hex Non-Inverting Buffer	6-128
14051B	8-Channel Analog Multiplexer/Demultiplexer	6-132
14052B	Dual 4-Channel Analog Multiplexer/Demultiplexer	6-132
14053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	6-132
14060B	14-Bit Binary Counter and Oscillator	6-139
14066B	Quad Analog Switch/Multiplexer	6-143
14067B	16-Channel Analog Multiplexer/Demultiplexer	6-149
14068B	8-Input NAND Gate	6-157
14069UB	Hex Inverter	6-158
14070B	Quad Exclusive OR Gate	6-160
14071B	Quad 2-Input OR Gate	6-162
14072B	Dual 4-Input OR Gate	6-163
14073B	Triple 3-Input AND Gate	6-164
14075B	Triple 3-Input OR Gate	6-165
14076B	Quad D-Type Register	6-166
14077B	Quad Exclusive NOR Gate	6-170
14078B	8-Input NOR Gate	6-171
14081B	Quad 2-Input AND Gate	6-172
14082B	Dual 4-Input AND Gate	6-173
14093B	Quad 2-Input NAND Schmitt Trigger	6-174
14094B	8-Bit Bus-Compatible Shift/Store Register	6-178
14097B	Dual 8-Channel Analog Multiplexer/Demultiplexer	6-182
14099B	8-Bit Addressable Latch	6-183
14106B	Hex Schmitt Trigger	6-189
14160B	Synchronous Presettable BCD Counter	6-193
14161B	Synchronous Presettable 4-Bit Binary Counter	6-193
14162B	Synchronous Presettable BCD Counter	6-193
14163B	Synchronous Presettable 4-Bit Binary Counter	6-193
14174B	Hex D Flip-Flop	6-202
14175B	Quad D Flip-Flop	6-206
14194B	4-Bit Universal Shift Register	6-210
14400	PCM Mono-circuit	Telecom
14401	PCM Mono-circuit	Telecom
14402	PCM Mono-circuit	Telecom
14403	PCM Mono-circuit	Telecom
14405	PCM Mono-circuit	Telecom
14408	Binary-to-Phone Pulse Converter	Telecom

Device Number MC	Description	Page Number
14409	Binary-to-Phone Pulse Converter	Telecom
14410	2-of-8 Tone Encoder	Telecom
14411	Bit-Rate Frequency Generator	Telecom
14412	Universal Low-Speed Modem	Telecom
14413	PCM Sampled Data Filter	Telecom
14414	PCM Sampled Data Filter	Telecom
14415	Quad Precision Timer/Driver	6-214
14416	PCM Time Slot Assigner Circuit	Telecom
14417	PCM Time Slot Assigner Circuit	Telecom
14418	PCM Time Slot Assigner Circuit	Telecom
14419	2-of-8 Keypad-to-Binary Encoder	Telecom
14422	Remote Control Transmitter (Product Cancelled)	—
14430	Input Address Encoder	Telecom
14433	3½ Digit A/D Converter	SF
14435	3½ Digit A/D Logic Subsystem (Product Cancelled)	SF
14442	Microprocessor-Compatible A/D Converter	SF
14443	6-Channel A/D Converter Subsystem	SF
14444	Microprocessor-Compatible A/D Converter	SF
14447	6-Channel A/D Converter Subsystem	SF
14457	Remote Control Transmitter	SF
14458	Remote Control Receiver	SF
14460	Automotive Speed Control Processor	6-219
14461	Smoke Detector Circuit (Product Cancelled)	—
14462	Smoke Detector Circuit (Product Cancelled)	—
14464	Smoke Detector Circuit (Product Cancelled)	—
14465	Smoke Detector Circuit (Product Cancelled)	—
14466	Low Cost Smoke Detector	SF
14467-1	Low Cost Smoke Detector	SF
14468	Interconnectable Smoke Detector	SF
14469	Addressable Asynchronous Receiver/Transmitter	SF
14490	Hex Contact Bounce Eliminator	6-225
14495-1	Hexadecimal-to-7 Segment Latch/Decoder ROM/Driver	SF
14497	PCM Remote Control Transmitter	SF
14499	7-Segment LED Display Decoder/Driver with Serial Interface	SF
14500B	Industrial Control Unit	6-232
14501UB	Triple Gate	6-238
14502B	Strobed Hex Inverter/Buffer	6-242
14503B	Hex 3-State Buffer	6-246
14504B	TTL- or CMOS-to-CMOS Hex Level Shifter	6-250
14506B	Dual Expandable AOI Gate (Superseded by 14506UB)	—
14506UB	Dual Expandable AOI Gate	6-253
14508B	Dual 4-Bit Latch	6-258
14510B	Presettable BCD Up/Down Counter	6-263
14511B	BCD-to-7-Segment Latch/Decoder/Driver	SF
14512B	8-Channel Data Selector	6-271
14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	SF

Device Number MC	Description	Page Number
14514B	4-Bit Transparent Latch/4-to-16 Line Decoder (High)	6-275
14515B	4-Bit Transparent Latch/4-to-16 Line Decoder (Low)	6-275
14516B	Presettable Binary Up/Down Counter	6-281
14517B	Dual 64-Bit Static Shift Register	6-289
14518B	Dual BCD Up Counter	6-293
14519B	4-Bit AND/OR Selector	6-298
14520B	Dual Binary Up Counter	6-302
14521B	24-Stage Frequency Divider	6-303
14522B	Programmable BCD Down Counter	6-309
14526B	Programmable 4-Bit Binary Down Counter	6-309
14527B	BCD Rate Multiplier	6-317
14528B	Dual Monostable Multivibrator (Not Recommended for New Designs)	6-323
14529B	Dual 4-Channel Analog Data Selector	6-329
14530B	Dual 5-Input Majority Logic Gate	6-335
14531B	12-Bit Parity Tree	6-340
14532B	8-Bit Priority Encoder	6-343
14534B	5 Cascaded BCD Counters	6-349
14536B	Programmable Timer	6-356
14538B	Dual Precision Monostable Multivibrator	6-367
14539B	Dual 4-Channel Data Selector/Multiplexer	6-375
14541B	Programmable Oscillator-Timer	6-379
14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals	SF
14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	SF
14547B	High-Current BCD-to-7-Segment Decoder/Driver	SF
14548B	Dual Monostable Multivibrator (Retriggerable/Resettable)	6-384
14549B	Successive Approximation Register	SF
14551B	Quad 2-Channel Analog Multiplexer/Demultiplexer	6-391
14553B	3-Digit BCD Counter	6-398
14554B	2 × 2-Bit Parallel Binary Multiplier	6-404
14555B	Dual Binary to 1-of-4 Decoder (Active High Outputs)	6-408
14556B	Dual Binary to 1-of-4 Decoder (Active Low Outputs)	6-408
14557B	1-to-64 Bit Variable Length Shift Register	6-411
14558B	BCD-to-7-Segment Decoder	SF
14559B	Successive Approximation Register	SF
14560B	NBCD Adder	6-415
14561B	9's Complementer	6-426
14562B	128-Bit Static Shift Register	6-432
14566B	Industrial Time-Base Generator	6-436
14568B	Phase Comparator and Programmable Counters	SF
14569B	Programmable Dual 4-Bit Binary/BCD Down Counter	6-442
14572UB	Hex Gate	6-452
14573	Quad Programmable Op Amp	SF
14574	Quad Programmable Comparator	SF
14575	Programmable Dual Op Amp/Dual Comparator	SF
14580B	4 × 4 Multiport Register	6-455

Device Number MC	Description	Page Number
14581B	4-Bit Arithmetic Logic Unit	6-460
14582B	Look-Ahead Carry Block	6-465
14583B	Dual Schmitt Trigger	6-469
14584B	Hex Schmitt Trigger	6-475
14585B	4-Bit Magnitude Comparator	6-478
14597B	8-Bit Bus-Compatible Counter Latch	6-482
14598B	8-Bit Bus-Compatible Addressable Latch	6-482
14599B	8-Bit Addressable Latch	6-488
142100	4 × 4 Crosspoint Switch	Telecom
142101	4 × 4 × 2 Crosspoint Switch	Telecom
143403	Quad Line Driver	Telecom
144110	Hex D/A Converter with Serial Interface	SF
144111	Quad D/A Converter with Serial Interface	SF
145000	48-Segment Multiplexed LCD Driver (Master)	SF
145001	44-Segment Multiplexed LCD Driver (Slave)	SF
145026	Remote Control Encoder	SF
145027	Remote Control Decoder	SF
145028	Remote Control Decoder	SF
145029	Remote Control Decoder	SF
145040	Analog-to-Digital Converter with Serial Interface	SF
145041	Analog-to-Digital Converter with Serial Interface	SF
145100	4 × 4 Cross Point Switch	Telecom
145104	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145106	PLL Frequency Synthesizer	SF
145107	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145109	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145112	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145143	PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145144	4-Bit Data Bus Input PLL Frequency Synthesizer (Not Recommended for New Designs)	SF
145145-1	4-Bit Data Bus Input PLL Frequency Synthesizer	SF
145146-1	4-Bit Data Bus Input PLL Frequency Synthesizer	SF
145151-1	Parallel Input PLL Frequency Synthesizer	SF
145152-1	Parallel Input PLL Frequency Synthesizer	SF
145155-1	Serial Input PLL Frequency Synthesizer	SF
145156-1	Serial Input PLL Frequency Synthesizer	SF
145157-1	Serial Input PLL Frequency Synthesizer	SF
145158-1	Serial Input PLL Frequency Synthesizer	SF
145159-1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	SF
145402	13-Bit Linear Codec	Telecom
145406	RS-232 Interface	Telecom
145409	Pulse Dialer	Telecom
145411	Baud Rate Generator	Telecom
145412	Pulse/Tone Reperatory Dialer	Telecom
145413	Pulse/Tone Reperatory Dialer	Telecom
145414	Dual Tuneable Low-Pass Sampled Data Filters	Telecom
145415	Dual Tuneable Linear Phase Low-Pass Sampled Data Filters	Telecom
145418	Master Digital Loop Transceiver	Telecom

Device Number MC	Description	Page Number
145419	Slave Digital Loop Transceiver	Telecom
145421	160 kbps ISDN Universal Digital Loop Transceiver	Telecom
145422	MDPSK Universal Digital Loop Transceiver (2-Wire Master)	Telecom
145425	160 kbps ISDN Universal Digital Loop Transceiver	Telecom
145426	MDPSK Universal Digital Loop Transceiver (2-Wire Slave)	Telecom
145428	Data Set Interface	Telecom
145429	Telset Audio Interface Circuit	Telecom
145432	2600 Hz Tone Signalling Filter	Telecom
145433	Tuneable Notch/Band-Pass Filter	Telecom
145439	Transcoder	Telecom
145440	Low-Speed Modem Filter	Telecom
145441	Low-Speed Modem Filter	Telecom
145445	300 Baud FSK Modem	Telecom
145450	1200 Baud FSK Modem	Telecom
145453	33-Segment LCD Driver with Serial Interface	SF
146805	Family of 8-Bit CMOS MCUs/MPUs	MCU,MPU
146818	Real-Time Clock/RAM	MCU,MPU
146823	Parallel Interface	MCU,MPU
1468705	8-Bit CMOS MCUs with EPROM	MCU,MPU

Product Selection Guide
Equivalent Gate Count

2

CMOS Selection Guide by Function

Device	Function	Page
NAND Gates		
MC14011B	Quad 2-Input NAND Gate	6-35
MC14011UB	Quad 2-Input NAND Gate	6-35
MC14093B	Quad 2-Input NAND Schmitt Trigger	6-174
MC14023B	Triple 3-Input NAND Gate	6-77
MC14023UB	Triple 3-Input NAND Gate	6-77
MC14012B	Dual 4-Input NAND Gate	6-36
MC14012UB	Dual 4-Input NAND Gate	6-36
MC14068B	8-Input NAND Gate	6-157
NOR Gates		
MC14001B	Quad 2-Input NOR Gate	6-6
MC14001UB	Quad 2-Input NOR Gate	6-15
MC14025B	Triple 3-Input NOR Gate	6-83
MC14025UB	Triple 3-Input NOR Gate	6-83
MC14000UB	Dual 3-Input NOR Gate plus Inverter	6-3
MC14002B	Dual 4-Input NOR Gate	6-20
MC14002UB	Dual 4-Input NOR Gate	6-20
MC14078B	8-Input NOR Gate	6-171
AND Gates		
MC14081B	Quad 2-Input AND Gate	6-172
MC14073B	Triple 3-Input AND Gate	6-164
MC14082B	Dual 4-Input AND Gate	6-173
OR Gates		
MC14071B	Quad 2-Input OR Gate	6-162
MC14075B	Triple 3-Input OR Gate	6-165
MC14072B	Dual 4-Input OR Gate	6-163
Complex Gates		
MC14070B	Quad Exclusive OR Gate	6-160
MC14077B	Quad Exclusive NOR Gate	6-170
MC14501UB	Triple Gate (Dual 4-Input NAND Gate and 2-Input NOR/OR Gate or 8-Input AND/NAND Gate)	6-238
MC14506B	Dual Expandable AND-OR-INVERT Gate (superseded by 14506B)	—
MC14519B	4-Bit AND/OR Selector (Quad 2-Channel Data Selector or Quad Exclusive NOR Gate)	6-298
MC14530B	Dual 5-Input Majority Logic Gate	6-335
MC14572UB	Hex Gate (Quad Inverter plus 2-Input NOR Gate plus 2-Input NAND Gate)	6-452

Device	Function	Page
Inverters/Buffers/Level Translator		
MC14007UB	Dual Complementary Pair plus Inverter	6-25
MC14049UB	Hex Inverting Buffer	6-128
MC14050B	Hex Noninverting Buffer	6-128
MC14069UB	Hex Inverter	6-158
MC14502B	Strobed Hex Inverter/Buffer	6-242
MC14503B	Hex 3-State Buffer	6-246
MC14504B	TTL or CMOS to CMOS Hex Level Shifter	6-250
MC14584B	Hex Schmitt Trigger	6-475
Decoders/Encoders		
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	6-88
MC14514B	4-Bit Latch/4-to-16 Line Decoder (High)	6-275
MC14515B	4-Bit Latch/4-to-16 Line Decoder (Low)	6-275
MC14532B	8-Bit Priority Encoder	6-343
MC14555B	Dual Binary to 1-of-4 Decoder/Demultiplexer	6-408
MC14556B	Dual Binary to 1-of-4 Decoder/Demultiplexer (Inverting)	6-408
Multiplexers/Demultiplexers/Bilateral Switches		
MC14016B	Quad Analog Switch/Quad Multiplexer	6-5
MC14066B	Quad Analog Switch/Quad Multiplexer	6-143
MC14053B	Triple 2-Channel Analog Multiplexer/Demultiplexer	6-132
MC14052B	Dual 4-Channel Analog Multiplexer/Demultiplexer	6-132
MC14529B	Dual 4-Channel Analog Data Selector	6-329
MC14539B	Dual 4-Channel Data Selector/Multiplexer	6-375
MC14051B	8-Channel Analog Multiplexer/Demultiplexer	6-132
MC14512B	8-Channel Data Selector	6-271
MC14097B	Dual 8-Channel Analog Multiplexer/Demultiplexer	6-182
MC14067B	16-Channel Analog Multiplexer/Demultiplexer	6-149
MC14519B	4-Bit AND/OR Selector	6-298
MC14551B	Quad 2-Channel Analog Multiplexer/Demultiplexer	6-391
Schmitt Triggers		
MC14093B	Quad 2-Input NAND Schmitt Trigger	6-174
MC14583B	Dual Schmitt Trigger	6-469
MC14106B	Hex Schmitt Trigger	6-189
MC14584B	Hex Schmitt Trigger	6-475
Flip-Flops/Latches		
MC14013B	Dual Type D Flip-Flop	6-37
MC14027B	Dual J-K Flip-Flop	6-84
MC14042B	Quad Transparent Latch	6-120
MC14043B	Quad NOR R-S Latch	6-124
MC14044B	Quad NAND R-S Latch	6-124
MC14076B	Quad D-Type Register	6-166
MC14175B	Quad Type D Flip-Flop	6-206

Device	Function	Page
MC14508B	Dual 4-Bit Latch	6-258
MC14174B	Hex Type D Flip-Flop	6-202
MC14099B	8-Bit Addressable Latch	6-183
MC14597B	8-Bit Bus-Compatible 3-State Latches-Internal Counter	6-482
MC14598B	8-Bit Bus-Compatible 3-State Latches-Binary Address	6-482
MC14599B	8-Bit Addressable Latch with Bidirectional Port	6-488

2

Shift Registers

MC14035B	4-Bit Parallel-In/Parallel-Out Shift Register	6-111
MC14194B	4-Bit Bidirectional Universal Shift Register	6-210
MC14015B	Dual 4-Bit Static Shift Register	6-45
MC14014B	8-Bit Static Shift Register	6-41
MC14021B	8-Bit Static Shift Register	6-71
MC14034B	8-Bit Universal Bus Register	6-104
MC14094B	8-Stage Shift/Store Register	6-178
MC14006B	18-Bit Static Shift Register	6-20
MC14557B	1-to-64 Bit Variable Length Shift Register	6-411
MC14517B	Dual 64-Bit Static Shift Register	6-289
MC14562B	128-Bit Static Shift Register	6-432

Counters

MC14024B	Seven-Stage Ripple Counter	6-78
MC14017B	Decade Counter	6-58
MC14018B	Presettable Divide-by-N Counter	6-63
MC14160B	Presettable BCD Counter (Asynchronous Clear)	6-193
MC14162B	Presettable BCD Counter (Synchronous Clear)	6-193
MC14029B	Presettable Binary/BCD Up/Down Counter	6-93
MC14510B	Presettable BCD Up/Down Counter	6-263
MC14522B	Programmable BCD Down Counter	6-309
MC14040B	12-Bit Binary Counter	6-116
MC14020B	14-Bit Binary Counter	6-67
MC14060B	14-Bit Binary Counter and Oscillator	6-139
MC14022B	Octal Counter	6-72
MC14161B	Presettable 4-Bit Binary Counter (Asynchronous Clear)	6-193
MC14163B	Presettable 4-Bit Binary Counter (Synchronous Clear)	6-193
MC14516B	Presettable Binary Up/Down Counter	6-281
MC14526B	Programmable 4-Bit Binary Down Counter	6-309
MC14518B	Dual BCD Up Counter	6-293
MC14520B	Dual Binary Up Counter	6-302
MC14569B	Programmable Dual Binary/BCD Counter	6-442
MC14553B	Three-Digit BCD Counter	6-398
MC14534B	5 Cascaded BCD Counters	6-349
MC14566B	Industrial Time Base Generator	6-436

Device	Function	Page
Oscillators/Timers		
MC14060B	14-Bit Binary Counter and Oscillator	6-139
MC14521B	24-Stage Frequency Divider	6-303
MC14536B	Programmable Timer	6-356
MC14541B	Programmable Oscillator/Timer	6-379
Multivibrators		
MC14528B	Dual Retriggerable/Resettable Monostable Multivibrator	6-323
MC14538B	Dual Precision Retriggerable/Resettable Monostable Multivibrator	6-367
MC14548B	Dual Retriggerable/Resettable Monostable Multivibrator	6-384
Adders/Comparators		
MC14008B	4-Bit Full Adder	6-29
MC14032B	Triple Serial Adder (Positive Logic)	6-99
MC14038B	Triple Serial Adder (Negative Logic)	6-115
MC14560B	NBCD Adder	6-415
MC14561B	9's Complementer	6-426
MC14582B	Look-Ahead Carry Block	6-465
MC14585B	4-Bit Magnitude Comparator	6-478
ALU/Rate Multipliers		
MC14527B	BCD Rate Multiplier	6-317
MC14554B	2 × 2-Bit Parallel Binary Multiplier	6-404
MC14581B	4-Bit Arithmetic Logic Unit	6-460
Parity Checker		
MC14531B	12-Bit Parity Tree	6-340
Memory		
MC14580B	4 × 4 Multiport Register	6-455
Microprocessor/Industrial Control		
MC14500B	Industrial Control Unit	6-232
Other Complex Functions		
MC14415	Quad Precision Timer/Driver	6-214
MC14460	Automotive Speed Control Processor	6-219
MC14490	Hex Contact Bounce Eliminator	6-225

EQUIVALENT GATE COUNT

The following is a list of equivalent gate counts for some of Motorola's CMOS devices. In general for CMOS, the number of equivalent gates is equal to the total number of transistors on chip divided by four. This list includes only those devices with equivalent gate counts known at the time of this printing.

DEVICE	EQUIVALENT GATE COUNT	DEVICE	EQUIVALENT GATE COUNT
MC14000UB	3.5	MC14175B	39.5
MC14001B	8	MC14410	245
MC14001UB	4	MC14411	205
MC14002B	7	MC14412	400
MC14002UB	4	MC14433	375
MC14006B	61.5	MC14469	378
MC14007UB	1.5	MC14490	136.5
MC14008B	40	MC14503B	17
MC14011B	8	MC14504B	37.5
MC14011UB	4	MC14508B	42
MC14012B	7	MC14510B	74
MC14012UB	4	MC14511B	54
MC14013B	16	MC14512B	17
MC14016B	8	MC14514B	59
MC14017B	62.5	MC14515B	67
MC14023B	9	MC14516B	61
MC14023UB	4.5	MC14517B	119
MC14024B	59	MC14518B	43.5
MC14025B	9	MC14520B	43.5
MC14025UB	4.5	MC14522B	86
MC14028B	26	MC14526B	86
MC14029B	65.5	MC14527B	46
MC14034B	145	MC14528B	24
MC14035B	38.5	MC14532B	38.5
MC14040B	73	MC14536B	103
MC14042B	17.5	MC14538B	38
MC14046B	35	MC14539B	20
MC14049UB	3	MC14541B	93
MC14050B	6	MC14543B	52
MC14051B	48.5	MC14549B	122
MC14052B	48.5	MC14553B	147.5
MC14053B	32.5	MC14555B	21
MC14066B	13	MC14556B	25
MC14068B	8	MC14557B	232.5
MC14069UB	3	MC14559B	122
MC14071B	10	MC14568B	137.25
MC14072B	8	MC14569B	156
MC14073B	10.5	MC14572UB	4
MC14075B	10.5	MC14573	7
MC14078B	7.5	MC14574	9
MC14081B	10	MC14575	11
MC14082B	8	MC145106	220.5
MC14093B	16	MC145146-1	1423
MC14094B	79	MC145151-1	2000
MC14099B	70	MC145152-1	2000
MC14161B	72.5	MC145155-1	1626
MC14163B	72.5	MC145156-1	1626
MC14174B	43.5	MC145158-1	1626

The "Better" Program 3

The "BETTER" Program

Motorola's reliability and quality-enhanced program was developed to provide improved levels of quality and reliability for standard commercial products.

The "BETTER" program is offered on Metal-Gate CMOS in dual-in-line ceramic and plastic packages.

Motorola standard commercial integrated circuits are manufactured under stringent in-process controls and quality inspections combined with the industry's finest outgoing quality inspections. The "BETTER" program offers three levels of extra processing each tailored to meet different user needs at nominal costs.

The program is designed to:

- Eliminate Incoming Electrical Inspection
- Estimate Need for Independent Test Labs and Associated Extra Time and Costs
- Reduce Field Failures
- Reduce Service Calls
- Reduce Equipment Downtime
- Reduce Board and System Rework
- Reduce Infant Mortality
- Save Time and Money
- Increase End-Customer Satisfaction

3

BETTER PROCESSING — STANDARD PRODUCT PLUS:

100% Screen	Level I "S"	Level II "D"	Level III "DS"
Temp Cycle 10 Cycles — 25°C to +150°C	X		X
25°C Functional and Parametric Test	X	X	X
High Temperature Test*	X		X
Burn-In		X	X
25°C Post Burn-In Functional and Parametric Test		X	X

*T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

"BETTER" AQL GUARANTEES

Test	Condition	AQL* Level I	AQL* Level II	AQL* Level III
High Temperature Functional	T_A = 100°C or T_A Max	0.065		0.065
DC Parametric	T_A = 25°C	0.065	0.065	0.065
DC Parametric	T_A Max	0.39		0.39
External Visual and Mechanical	Major/Minor	0.065	0.065	0.065
Hermeticity (Not Applicable to Plastic Packages)	Gross/Fine	0.15	0.15	0.15

*"AQL" values shown are for reference only. "LTPD" type sampling plans that are equal to or tighter than values indicated may be used. Also, the guaranteed electrical and visual/mechanical AQL levels will be progressively tightened. Contact your nearest Motorola sales office for current values.

PART MARKING

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

HOW TO ORDER

MC14001B — Part Identification

CP — Standard Package Suffix

S — "BETTER" PROCESSING
LEVEL I = SUFFIX S
LEVEL II = SUFFIX D
LEVEL III = SUFFIX DS

B and UB Series Family Data

4

B AND UB SERIES CMOS FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized# family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- 3-18 volt operational limits
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range
- Direct Interface to High-Speed CMOS
- Maximum input current of ± 1 μA at 15 volt power supply over the temperature range
- Parameters specified at 5.0, 10, and 15 volt supply
- Noise margins: B Series
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10 V supply
  2.5 V min @ 15 V supply

  UB Series
  0.5 V min @ 5.0 V supply
  1.0 V min @ 10 V supply
  1.0 V min @ 15 V supply

The industry-standardized maximum ratings are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

Load Capacitance, C_L, of 50 pF
Input Voltage equal to $V_{SS} - V_{DD}$ (Rail-to-Rail swing)
Input pulse rise and fall times of 20 ns
Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage
Three different supply voltages: 5, 10, and 15 V

Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose inputs and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

#Specifications coordinated by EIA/JEDEC Solid-State Products Council.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". This "1" or "0" output level is defined as a deviation from the supply (V_{DD}) and ground (V_{SS}) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltages and the defined output deviations lead to the calculated noise margins. Noise margin is defined as the difference between V_{IL} or V_{IH} and V_{out} (output deviation). As an example, for a noninverting buffer at V_{DD} = 5.0 volts: V_{IL} = 1.5 volts and V_{out} = 0.5 volts. Therefore, Noise Margin equals $V_{IL} - V_{out}$ = 1.0 volt. This figure is useful while cascading stages (See Figure 1). With the input to the first stage at a worst-case voltage level (V_{IL} = 1.5 V), the output is guaranteed to be no greater than 0.5 volts with a 5.0 volt supply. Since the maximum allowable logic 0 for the second stage is 1.5 volts, this 0.5 volt output provides a 1.0 volt margin for noise to the next stage.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one low-power Schottky TTL input.

B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables, or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed, since only a single stage is involved.

The B and UB series, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices, such as High-Speed CMOS Logic.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

FIGURE 1

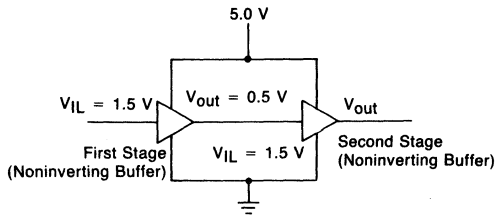


TABLE 1 – EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{DD}	Quiescent Device Current	Mil	5	$V_{in} = V_{SS}$ or V_{DD}		0.25		0.25		7.5	μAdc
			10			0.5		0.5		15	
			15			1.0		1.0		30	
	GATES	Comm	5	All valid input combinations		1.0		1.0		7.5	μAdc
			10			2.0		2.0		15	
			15			4.0		4.0		30	
		Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		1.0		1.0		30	μAdc
			10			2.0		2.0		60	
			15			4.0		4.0		120	
	BUFFERS, FLIP-FLOPS	Comm	5	All valid input combinations		4		4.0		30	μAdc
			10			8		8.0		60	
			15			16		16.0		120	
		Mil	5	$V_{IN} = V_{SS}$ or V_{DD}		5		5		150	μAdc
			10			10		10		300	
			15			20		20		600	
	MSI	Comm	5	All valid input combinations		20		20		150	μAdc
			10			40		40		300	
			15			80		80		600	
V_{OL}	Low-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\mu A$		0.05		0.05		0.05	Vdc
			10			0.05		0.05		0.05	
			15			0.05		0.05		0.05	
V_{OH}	High-Level Output Voltage	All	5	$V_{IN} = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\mu A$	4.95		4.95		4.95		Vdc
			10		9.95		9.95		9.95		
			15		14.95		14.95		14.95		
V_{IL}	Input Low Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V $\lvert I_O \rvert < 1\mu A$		1.5		1.5		1.5	Vdc
			10	$V_O = 1.0V$ or 9.0V		3.0		3.0		3.0	
			15	$V_O = 1.5V$ or 13.5V		4.0		4.0		4.0	
V_{IL}	Input Low Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V $\lvert I_O \rvert < 1\mu A$		1.0		1.0		1.0	Vdc
			10	$V_O = 1.0V$ or 9.0V		2.0		2.0		2.0	
			15	$V_O = 1.5V$ or 13.5V		2.5		2.5		2.5	
V_{IH}	Input High Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V $\lvert I_O \rvert < 1\mu A$	3.5		3.5		3.5		Vdc
			10	$V_O = 1.0V$ or 9.0V	7.0		7.0		7.0		
			15	$V_O = 1.5V$ or 13.5V	11.0		11.0		11.0		
V_{IH}	Input High Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V $\lvert I_O \rvert < 1\mu A$	4.0		4.0		4.0		Vdc
			10	$V_O = 1.0V$ or 9.0V	8.0		8.0		8.0		
			15	$V_O = 1.5V$ or 13.5V	12.5		12.5		12.5		
I_{OL}	Output Low (Sink) Current	Mil	5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.64		0.51		0.36		mAdc
			10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.6		1.3		0.9		
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	4.2		3.4		2.4		
		Com	5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.52		0.44		0.36		mAdc
			10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.3		1.1		0.9		
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	3.6		3.0		2.4		

TABLE 1 – Continued

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{OH}	Output High (Source) Current	Mil	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.25		-0.2		-0.14		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.62		-0.5		-0.35		
			15	V_O = 13.5V, V_{IN} = o or 15V	-1.8		-1.5		-1.1		
		Com	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.2		-0.16		-0.12		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.5		-0.4		-0.3		
			15	V_O = 13.5V V_{IN} = 0 or 15V	-1.4		-1.2		-1.0		
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15V		±0.1		±0.1		±1.0	µAdc
		Comm	15	V_{IN} = 0 or 15V		±0.3		±0.3		±1.0	µAdc
I_{oz}	3-State Output Leakage Current	Mil	15	V_{IN} = 0 or 15V		±0.4		±0.4		±12	µAdc
		Comm	15	V_{IN} = 0 or 15V		±1.6		±1.6		±12	µAdc
C_{IN}	Input Capacitance per unit load	All	–	Any Input				7.5			pF

*T_{LOW} = -55°C for Military temperature range device, -40°C for Commercial temperature range device.
T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.
#Applies for Worst Case input combinations.

TABLE 2 – MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

4

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0.05	–	0.05	
			15	–	0.05	–	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	–	9.95	–	
			15	14.95	–	14.95	–	14.95	–	
Input Voltage B Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	4.0	–	4.0	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	–	3.5	–	
(V_O 1.0 or 9.0 Vdc)			10	7.0	–	7.0	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	–	11.0	–	
Input Voltage UB Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.0	–	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)			10	–	2.0	–	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	2.5	–	2.5	–	2.5	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	4.0	–	4.0	–	4.0	–	
(V_O = 1.0 or 9.0 Vdc)			10	8.0	–	8.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	12.5	–	12.5	–	12.5	–	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
			Min	Max	Min	Max	Min	Max	
Output Drive Current (AL) B Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) B Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) UB Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) UB Gates	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) Other Devices	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	−0.64	–	−0.51	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) Other Devices	I_{OH}								mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	−0.52	–	−0.44	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	7.5	–	–	pF
Gate Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.25	–	7.5	μAdc
		10	–	0.5	–	0.5	–	15	
		15	–	1.0	–	1.0	–	30	
(CL/CP Device)	I_{DD}	5.0	–	1.0	–	1.0	–	7.5	
		10	–	2.0	–	2.0	–	15	
		15	–	4.0	–	4.0	–	30	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Flip-Flop and Buffer Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	1.0	–	1.0	–	30	μAdc
			10	–	2.0	–	2.0	–	60	
			15	–	4.0	–	4.0	–	120	
	(CL/CP Device)	I_{DD}	5.0	–	4.0	–	4.0	–	30	μAdc
			10	–	8.0	–	8.0	–	60	
			15	–	16	–	16	–	120	
MSI Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	5.0	–	5.0	–	150	μAdc
			10	–	10	–	10	–	300	
			15	–	20	–	20	–	600	
	(CL/CP Device)	I_{DD}	5.0	–	20	–	20	–	150	μAdc
			10	–	40	–	40	–	300	
			15	–	80	–	80	–	600	
LSI Quiescent Current		I_{DD}		See Individual Data Sheets.						

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

4

CMOS Handling and Design Guidelines

5

HANDLING AND DESIGN GUIDELINES

HANDLING PRECAUTIONS

All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for Motorola CMOS devices is about 800 Å thick and breaks down at a gate-source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection network shown in Figure 1 is used on each input to the CMOS device.

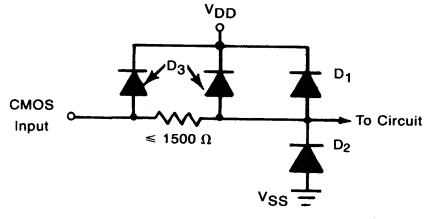
Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4-15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.
5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
7. Nylon or other static generating materials should not come in contact with CMOS devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

5

FIGURE 1 — INPUT PROTECTION NETWORK



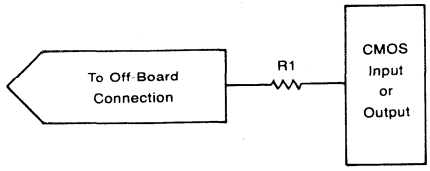
12. The following steps should be observed during board-cleaning operations:
    a. Vapor degreasers and baskets must be grounded to an earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"

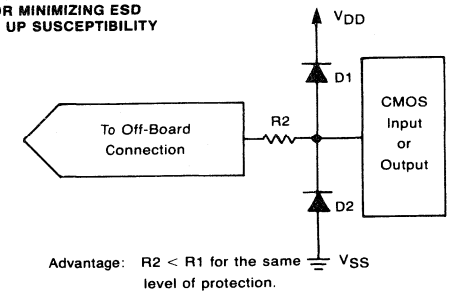
Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769-2963
Or by Calling:.
1-800-328-1368

FIGURE 2 — NETWORKS FOR MINIMIZING ESD AND REDUCING CMOS LATCH UP SUSCEPTIBILITY



Advantage: Requires minimal board area

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized

Disadvantage: More board area, higher initial cost

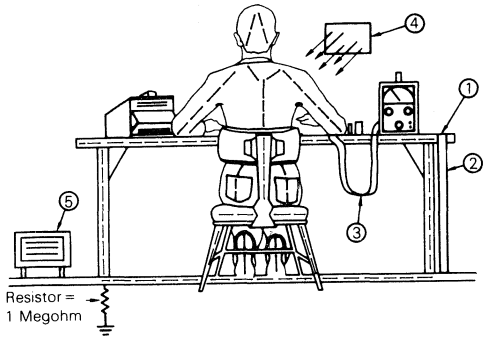
Note: These networks are useful for protecting the following
A digital inputs and outputs
B analog inputs and outputs
C 3-state outputs
D bidirectional (I/O) ports

PROPAGATION DELAY AND RISE TIME vs. SERIES RESISTANCE

$$R \approx \frac{t}{C \cdot k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay or rise time in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for propagation delay calculations
k = 2.3 for rise time calculations

FIGURE 3 — TYPICAL MANUFACTURING WORK STATION



NOTES: 1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

5

POWER SUPPLIES

CMOS devices have low power requirements and the ability to operate over a wide range of supply voltages. These two characteristics allow CMOS designs to be implemented using inexpensive, conventional power supplies, instead of switching power supplies and power supplies with cooling fans. In addition, batteries may be used as either a primary power source or for emergency backup.

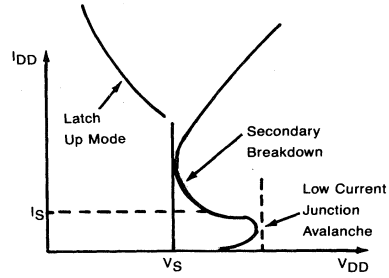
The *absolute* maximum power supply voltage for 14000 Series Metal-gate CMOS is 18.0 Vdc. Figure 4 offers some insight as to how this specification was derived. In the figure, V_S is the maximum power supply voltage and I_S is the sustaining current of the latch-up mode. The value of V_S was chosen so that the secondary breakdown effect may be avoided.

In an ideal system design, a power supply should be designed to deliver only enough current to insure proper operation of all devices. The obvious benefit of this type design is cost savings; an added benefit is protection against the possibility of latch-up related failures. This system protection can be provided by the power supply filter and/or voltage regulator.

CMOS devices can be used with battery or battery backup systems. A few precautions should be taken when designing battery-operated systems:

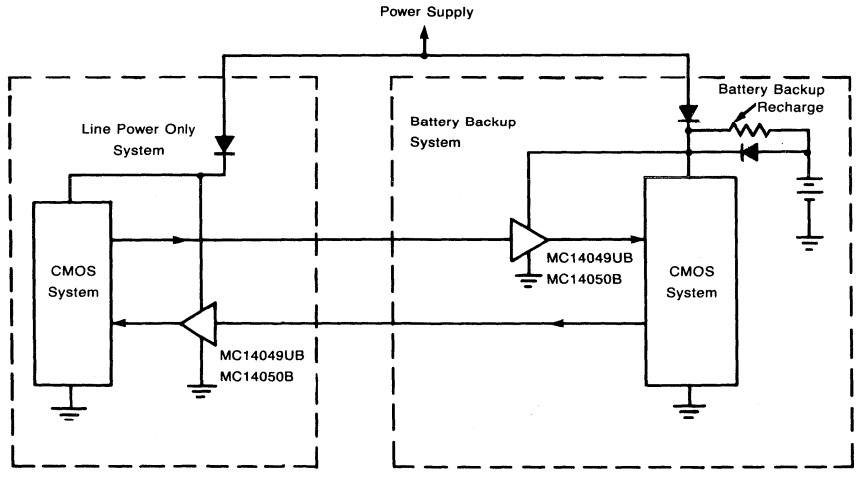
1. The recommended power supply voltage should be observed. For battery backup systems such as the one in Figure 5, the battery voltage must be at least 3.7 Volts (3 Volts from the minimum power supply voltage and 0.7 Volts to account for the voltage drop across the series diode).
2. Inputs that might go above the battery backup voltage should either use a series resistor to limit the input current to less than 10 mA or use the MC14049UB or MC14050B high-to-low voltage translators.
3. Outputs that are subject to voltage levels above V_{DD} or below V_{SS} should be protected with a series resistor to limit the current to less than 10 mA or with clamping diodes.

FIGURE 4 — SECONDARY BREAKDOWN CHARACTERISTICS



V_S = Data Sheet Maximum Supply Rating

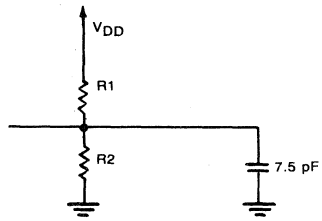
FIGURE 5 — BATTERY BACKUP INTERFACE



INPUTS

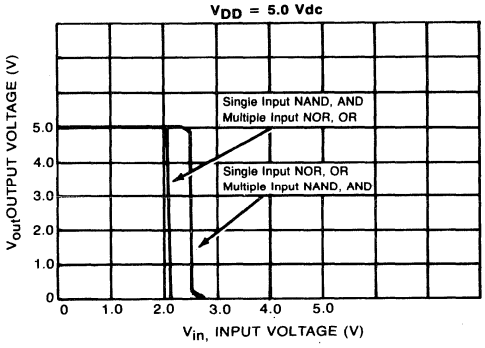
All inputs, while in the recommended operating range ($V_{SS} < V_{in} < V_{DD}$) can be modeled as shown in Figure 6. For input voltages in this range, diodes D1 and D2 are modeled as resistors, representing the reverse bias impedance of the diodes. The maximum input current is worst case, 1 μA, when the inputs are at V_{DD} or V_{SS}, and V_{DD} = 15.0 V. This model does not apply to inputs with pull-up or pull-down resistors.

FIGURE 6 — INPUT MODEL FOR $V_{SS} \leq V_{in} \leq V_{DD}$



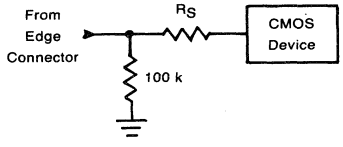
When left open-circuited, the inputs may self-bias at or near the typical switchpoint, where both the P-channel and N-channel transistors are conducting, causing excessive current drain. Due to the high gain of the inverters (see Figure 7), the device may also go into oscillation from any noise in the system. Since CMOS devices dissipate the most power during switching, this oscillation can cause very large current drain and undesired switching.

FIGURE 7 — TYPICAL TRANSFER CHARACTERISTICS FOR BUFFERED DEVICES



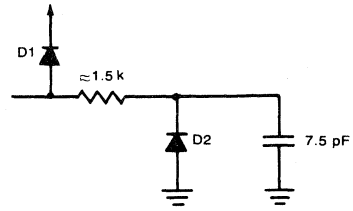
For these reasons, all unused inputs should be connected either to V_{DD} or V_{SS}. For applications with inputs going to edge connectors, a 100 kilohm resistor to V_{SS} should be used, as well as a series resistor for static protection and current limiting (Figure 8). The 100 kilohm resistor will help eliminate any static charges that might develop on the printed circuit board. See Figure 2 for other possible protection arrangements.

FIGURE 8 — EXTERNAL PROTECTION



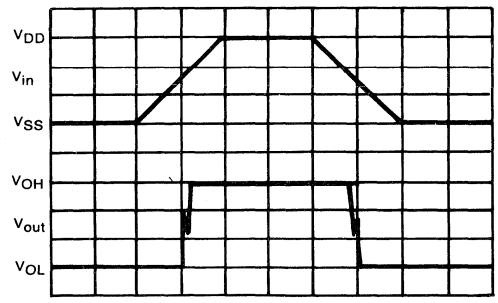
For input voltages outside of the recommended operating range, the CMOS input is modeled as in Figure 9. The resistor-diode protection network allows the user greater freedom when designing a worst case system. The device inputs are guaranteed to withstand voltages from V_{SS} − 0.5 V to V_{DD} + 0.5 V and a maximum current of 10 mA. With the above input ratings, most designs will require no special terminations or design considerations.

FIGURE 9 — INPUT MODEL FOR $V_{in} > V_{DD}$ or $V_{in} < V_{SS}$



Other specifications that should be noted are the maximum input rise and fall times. Figure 10 shows the oscillations that may result from exceeding the 15 μs maximum rise and fall time at V_{DD} = 5.0 V, 5 μs at 10 V, or 4 μs at 15 V. As the voltage passes through the switching threshold region with a slow rise time, any noise that is on the input is amplified, and passed through to the output, causing oscillations. The oscillation may have a low enough frequency to cause succeeding stages to switch, giving unexpected results. If input rise or fall times are expected to exceed 15 μs at 5.0 V, 5 μs at 10 V, or 4 μs at 15 V, Schmitt-trigger devices such as the MC14093B, MC14583B, MC14584B, MC14106B, HC14, or HC132 are recommended for squaring-up these slow transitions.

FIGURE 10 — MAXIMUM RISE AND FALL TIME VIOLATIONS



5

OUTPUTS

All CMOS B-Series outputs are buffered to insure consistent output voltage and current performance. All buffered outputs have guaranteed output voltages of V_{OL} = 0.05 V and V_{OH} = V_{DD} − 0.05 V for V_{in} = V_{DD} or V_{SS} and I_{out} = 0 μA. The output drives for all buffered CMOS devices are such that 1 LSTTL load can be driven across the full temperature range.

CMOS outputs are limited to externally forced output voltages of V_{SS} − 0.5 V ≤ V_{out} ≤ V_{DD} + 0.5 V. When voltages are forced outside of this range, a silicon controlled rectifier (SCR) formed by parasitic transistors can be triggered, causing the device to latch up. For more information on this, see the explanation of CMOS Latch Up in this section.

The maximum rated output current for most outputs is 10 mA. The output short-circuit currents of these devices typically exceed these limits. Care must be taken not to exceed the maximum ratings found on every data sheet.

For applications that require driving high capacitive loads where fast propagation delays are needed (e.g., driving power MOSFETs), two or more outputs on the same chip may be externally paralleled.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 11 shows the cross-section of a typical CMOS inverter and Figure 12 shows the parasitic bipolar devices. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch up condition, transistors Q1 and Q2 are turned ON, each providing the base current necessary for the other to remain in saturation, thereby latching the devices in the ON state. Unlike a conventional SCR, where the device is turned ON by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned ON by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 V or less than V_{SS} − 0.5 V and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below:

1. Insure that inputs and outputs are limited to the maximum rated values, as follows:
   − 0.5 V ≤ V_{in} or V_{out} ≤ V_{DD} + 0.5 V (referenced to V_{SS})
   $|I_{in}$ or $I_{out}|$ ≤ 10 mA (unless otherwise indicated on the data sheet)
2. If voltage transients of sufficient energy to latch up the device are expected on the inputs or outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the maximum rating of 10 mA. (See Figure 2).
3. Sequence power supplies so that the inputs or outputs of CMOS devices are not active before the supply pins are powered up (e.g., recessed edge connectors and/or series resistors may be used in plug-in board applications).
4. Voltage regulating or filtering should be used in board design and layout to insure that power-supply lines are free of excessive noise.
5. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

FIGURE 11 — CMOS WAFER CROSS SECTION

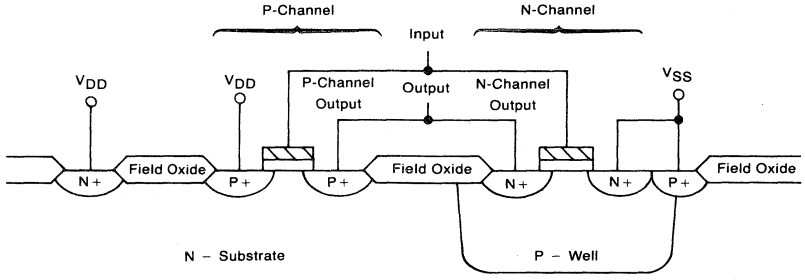
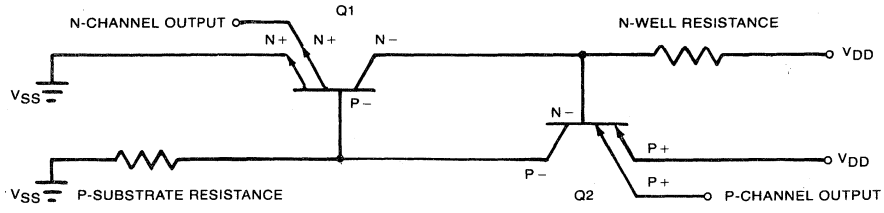


FIGURE 12 — LATCH UP CIRCUIT SCHEMATIC



Data Sheets 6

MOTOROLA

MC14000UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

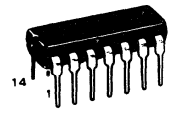
DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

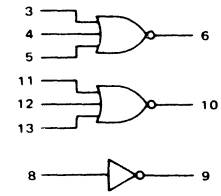
C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

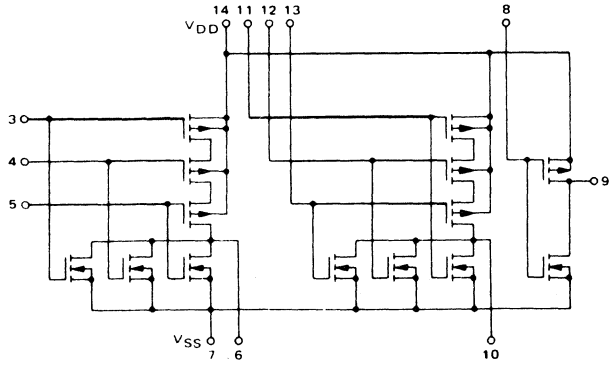
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM

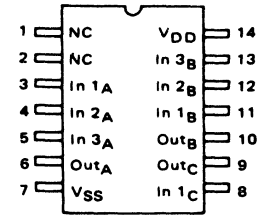


V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



PIN ASSIGNMENT



NC = NO CONNECTION

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	—	1.0	—	2.25	1.0	—	1.0	
(V_O = 9.0 Vdc)		10	—	2.0	—	4.50	2.0	—	2.0	
(V_O = 13.5 Vdc)		15	—	2.5	—	6.75	2.5	—	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
(V_O = 1.0 Vdc)		10	8.0	—	8.0	5.50	—	8.0	—	
(V_O = 1.5 Vdc)		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	
(V_{OH} = 9.5 Vdc)		10	-0.62	—	-0.5	-0.9	—	-0.35	—	
(V_{OH} = 13.5 Vdc)		15	-1.8	—	-1.5	-3.5	—	-1.1	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	—	-0.8	-1.7	—	-0.6	—	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	—	-0.16	-0.36	—	-0.12	—	
(V_{OH} = 9.5 Vdc)		10	-0.5	—	-0.4	-0.9	—	-0.3	—	
(V_{OH} = 13.5 Vdc)		15	-1.4	—	-1.2	-3.5	—	-1.0	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	—	1.1	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I_{in}	15	—	±0.1		±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3		±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	μAdc
		10	—	0.50	—	0.0010	0.50	—	15.0	
		15	—	1.00	—	0.0015	1.00	—	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0		1.0	—	0.0005	1.0	—	7.5	μAdc
		10		2.0	—	0.0010	2.0	—	15.0	
		15		4.0	—	0.0015	4.0	—	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/N							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 μA/kHz) f + I_{DD}/N							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	115	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

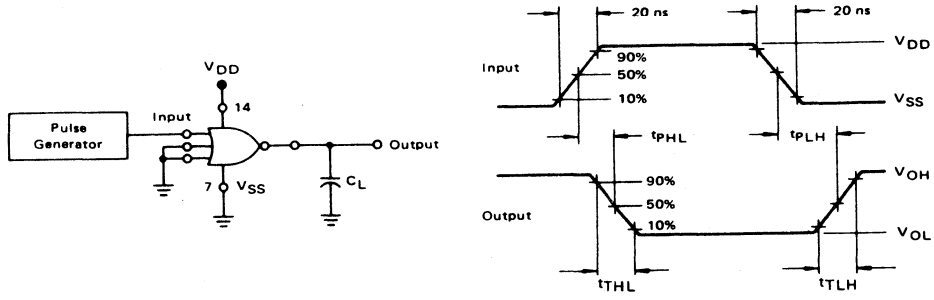


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

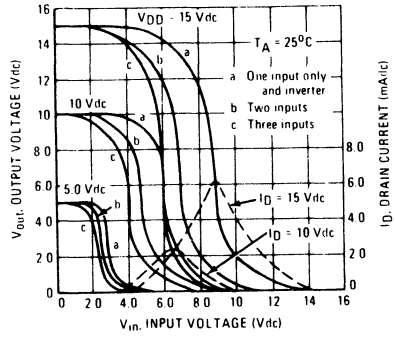
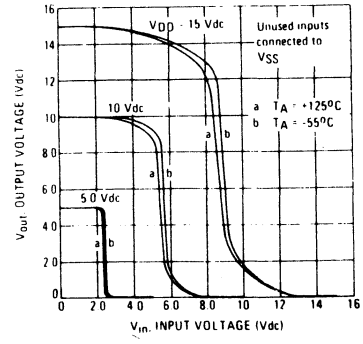


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



6

MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input Nor Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

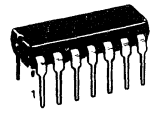
B-SUFFIX SERIES CMOS GATES

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

B-SERIES GATES

6

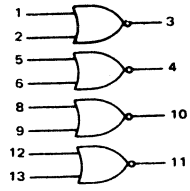
CMOS B-SERIES GATES

LOGIC DIAGRAMS

2 INPUT

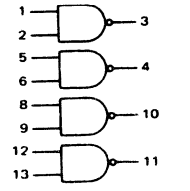
NOR

MC14001B
Quad 2-Input NOR Gate



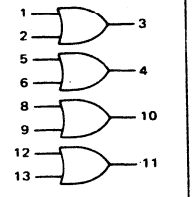
NAND

MC14011B
Quad 2-Input NAND Gate



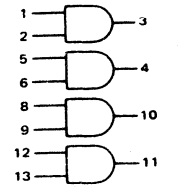
OR

MC14071B
Quad 2-Input OR Gate



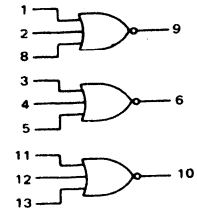
AND

MC14081B
Quad 2-Input AND Gate

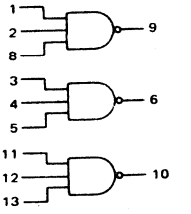


3 INPUT

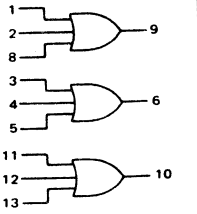
MC14025B
Triple 3-Input NOR Gate



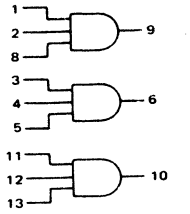
MC14023B
Triple 3-Input NAND Gate



MC14075B
Triple 3-Input OR Gate

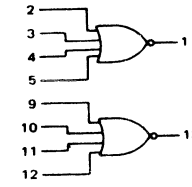


MC14073B
Triple 3-Input AND Gate

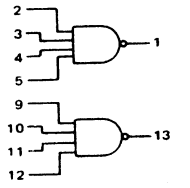


4 INPUT

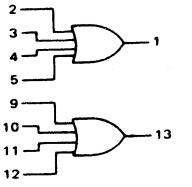
MC14002B
Dual 4-Input NOR Gate



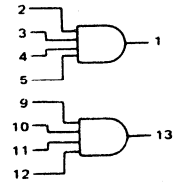
MC14012B
Dual 4-Input NAND Gate



MC14072B
Dual 4-Input OR Gate

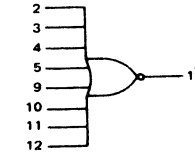


MC14082B
Dual 4-Input AND Gate

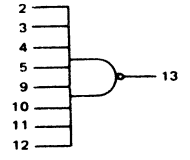


8 INPUT

MC14078B
8-Input NOR Gate



MC14068B
8-Input NAND Gate



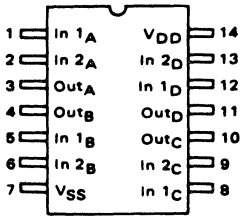
V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

6

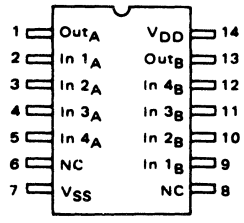
CMOS B-SERIES GATES

PIN ASSIGNMENTS

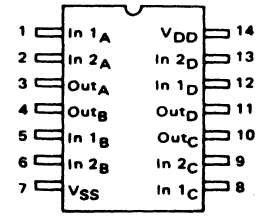
MC14001B
Quad 2-Input NOR Gate



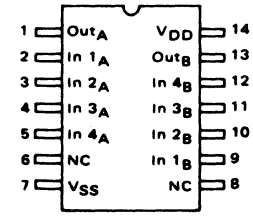
MC14002B
Dual 4-Input NOR Gate



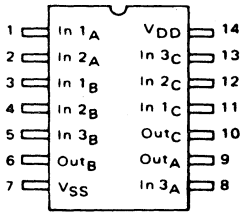
MC14011B
Quad 2-Input NAND Gate



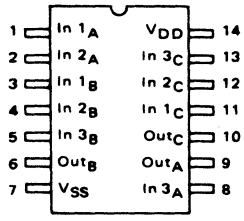
MC14012B
Dual 4-Input NAND Gate



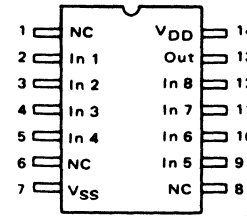
MC14023B
Triple 3-Input NAND Gate



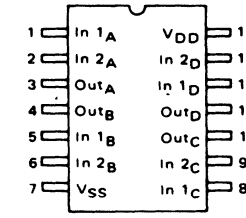
MC14025B
Triple 3-Input NOR Gate



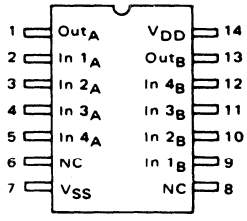
MC14068B
8-Input NAND Gate



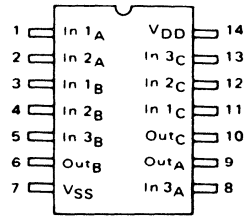
MC14071B
Quad 2-Input OR Gate



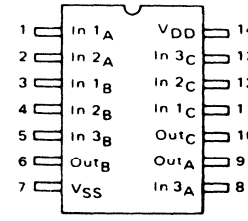
MC14072B
Dual 4-Input OR Gate



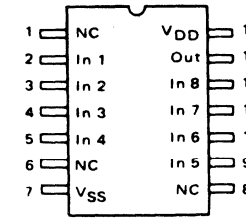
MC14073B
Triple 3-Input AND Gate



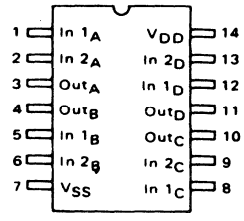
MC14075B
Triple 3-Input OR Gate



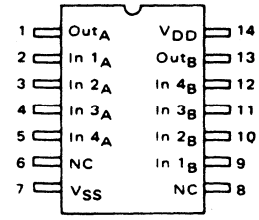
MC14078B
8-Input NOR Gate



MC14081B
Quad 2-Input AND Gate



MC14082B
Dual 4-Input AND Gate



NC = No Connection

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0		0.05		0	0.05		0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05		0	0.05		0.05	
		15		0.05		0	0.05		0.05	
"1" Level	V_{OH}	5.0	4.95		4.95	5.0		4.95		Vdc
V_{in} = 0 or V_{DD}		10	9.95		9.95	10		9.95		
		15	14.95		14.95	15		14.95		
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0		1.5		2.25	1.5		1.5	
(V_O = 9.0 or 1.0 Vdc)		10		3.0		4.50	3.0		3.0	
(V_O = 13.5 or 1.5 Vdc)		15		4.0		6.75	4.0		4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5		3.5	2.75		3.5		Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0		7.0	5.50		7.0		
(V_O = 1.5 or 13.5 Vdc)		15	11.0		11.0	8.25		11.0		
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0		-2.4	-4.2		-1.7		
(V_{OH} = 4.6 Vdc)		5.0	-0.64		-0.51	-0.88		-0.36		
(V_{OH} = 9.5 Vdc)		10	-1.6		-1.3	-2.25		-0.9		
(V_{OH} = 13.5 Vdc)		15	-4.2		-3.4	-8.8		-2.4		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64		0.51	0.88		0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.6		1.3	2.25		0.9		
(V_{OL} = 1.5 Vdc)		15	4.2		3.4	8.8		2.4		
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5		-2.1	-4.2		-1.7		
(V_{OH} = 4.6 Vdc)		5.0	-0.52		-0.44	-0.88		-0.36		
(V_{OH} = 9.5 Vdc)		10	-1.3		-1.1	-2.25		-0.9		
(V_{OH} = 13.5 Vdc)		15	-3.6		-3.0	-8.8		-2.4		
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52		0.44	0.88		0.36		mAdc
(V_{OL} = 0.5 Vdc)		10	1.3		1.1	2.25		0.9		
(V_{OL} = 1.5 Vdc)		15	3.6		3.0	8.8		2.4		
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—			5.0	7.5			pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0		0.25		0.0005	0.25		7.5	μAdc
		10		0.50		0.0010	0.50		15.0	
		15		1.00		0.0015	1.00		30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0		1.0		0.0005	1.0		7.5	μAdc
		10		2.0		0.0010	2.0		15.0	
		15		4.0		0.0015	4.0		30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/N							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/N							
		15	I_T = (0.9 μA/kHz) f + I_{DD}/N							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

6

B-SERIES GATE SWITCHING TIMES

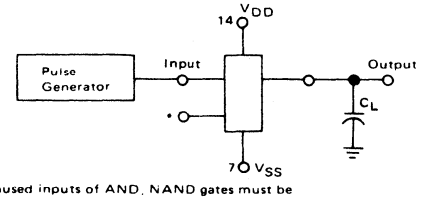
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	–	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	50	100	
8-Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	–	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	–	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	110	

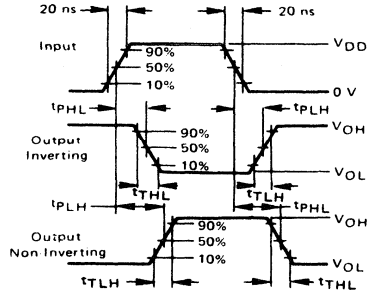
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

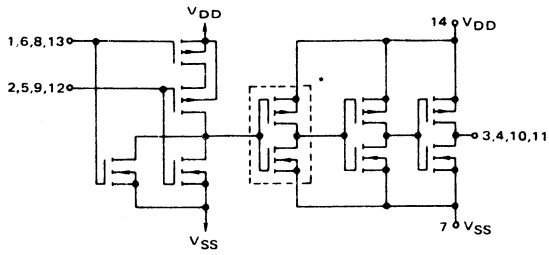


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}



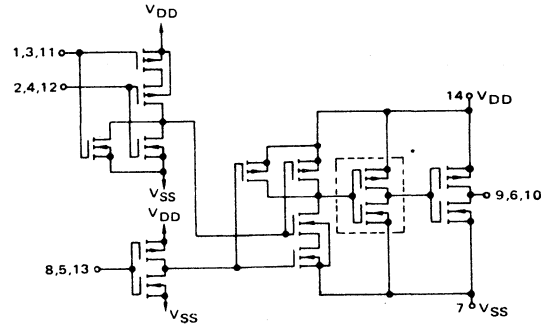
CIRCUIT SCHEMATIC
NOR, OR Gates

MC14001B
MC14071B
One of Four
Gates Shown



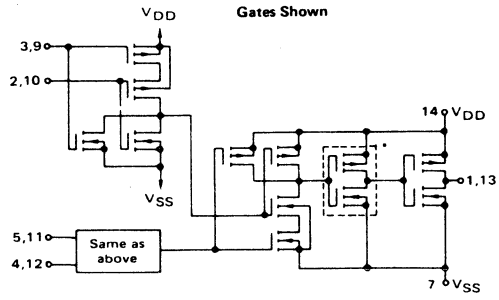
*Inverter Omitted in MC14001B

MC14025B
MC14075B
One of Three
Gates Shown



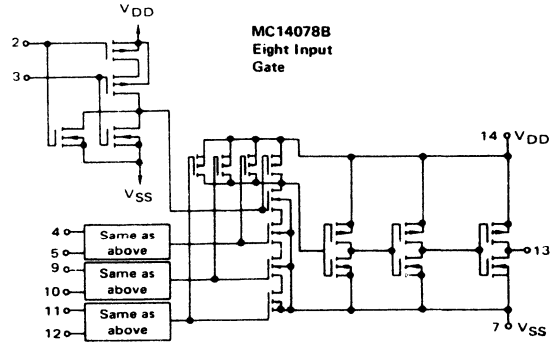
*Inverter Omitted in MC14025B

MC14002B
MC14072B
One of Two
Gates Shown



*Inverter Omitted in MC14002B

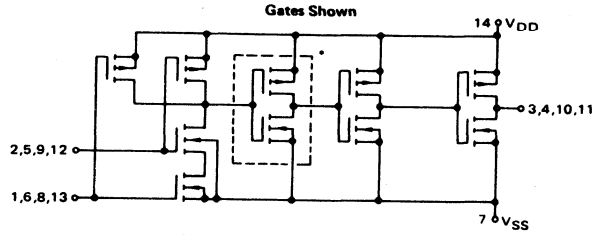
MC14078B
Eight Input
Gate



6

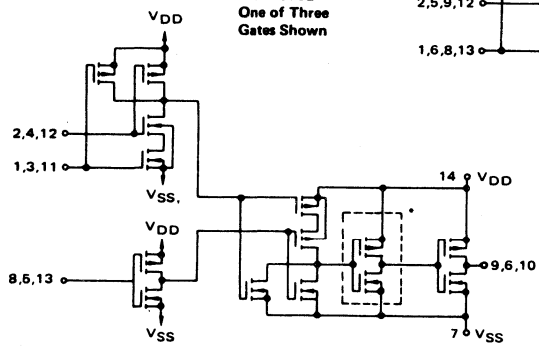
CIRCUIT SCHEMATICS
NAND, AND Gates

MC14011B
MC14081B
One of Four
Gates Shown



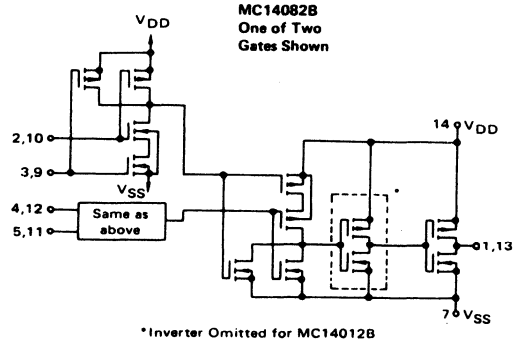
*Inverter Omitted in MC14011B

MC14023B
MC14073B
One of Three
Gates Shown



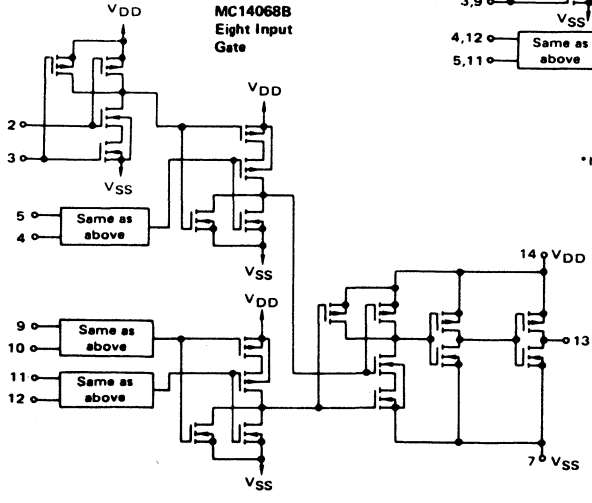
*Inverter Omitted in MC14023B

MC14012B
MC14082B
One of Two
Gates Shown



*Inverter Omitted for MC14012B

MC14068B
Eight Input
Gate



6

TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

FIGURE 2 – V_{GS} = 5.0 Vdc

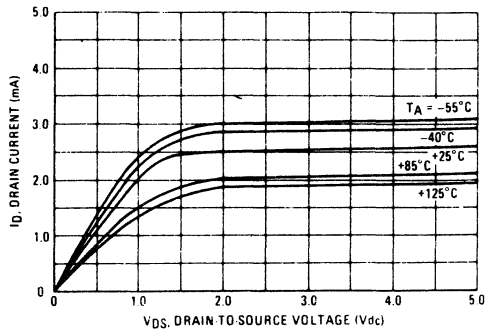


FIGURE 4 – V_{GS} = 10 Vdc

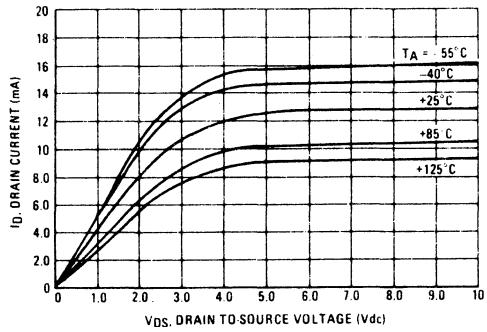
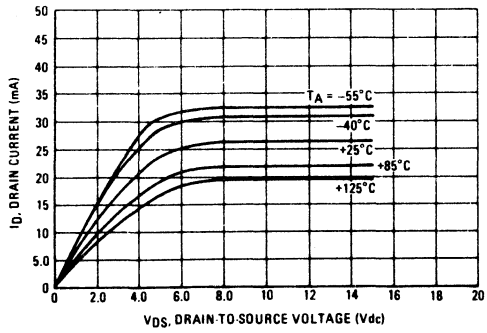


FIGURE 6 – V_{GS} = 15 Vdc



P-CHANNEL DRAIN CURRENT (SOURCE)

FIGURE 3 – V_{GS} = −5.0 Vdc

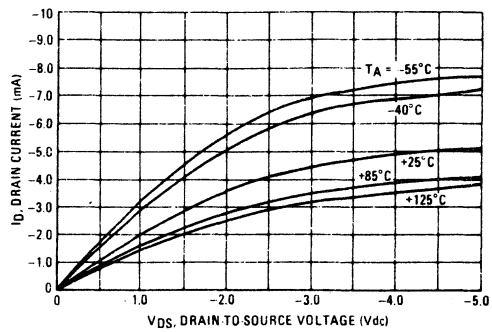


FIGURE 5 – V_{GS} = −10 Vdc

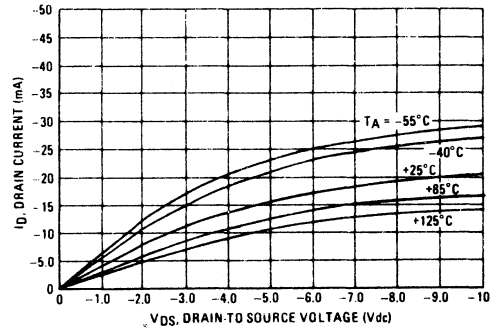
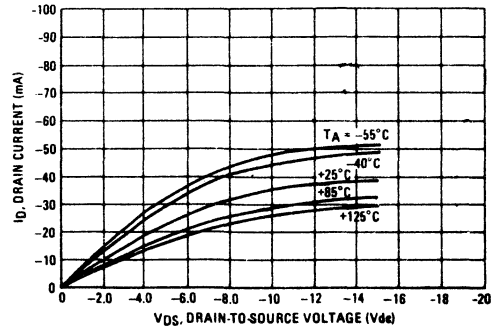


FIGURE 7 – V_{GS} = −15 Vdc



These typical curves are not guarantees, but are design aids.
Caution: The maximum rating for output current is 10 mA per pin.

TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 – V_{DD} = 5.0 Vdc

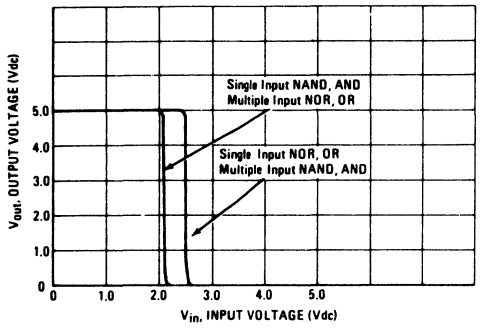


FIGURE 9 – V_{DD} = 10 Vdc

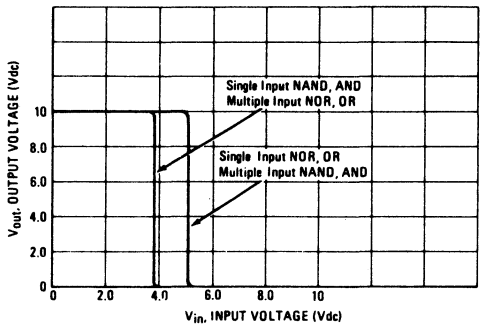
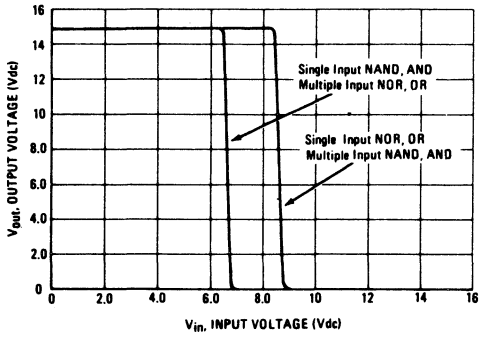


FIGURE 10 – V_{DD} = 15 Vdc



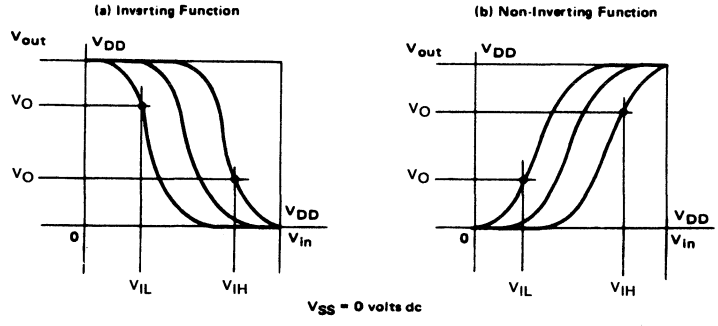
DC NOISE MARGIN

The DC noise margin is defined as the input voltage range from an ideal "1" or "0" input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the "1" and "0" levels =

1.0 V with a 5.0 V supply
2.0 V with a 10.0 V supply
2.5 V with a 15.0 V supply

FIGURE 11 – DC NOISE IMMUNITY



V_{SS} = 0 volts dc

6

MOTOROLA

MC14001UB
Quad 2-Input NOR Gate

MC14002UB
Dual 4-Input NOR Gate

MC14011UB
Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB
Triple3-Input NOR Gate

UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices

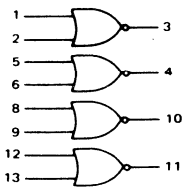
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

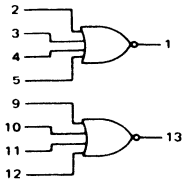
UB-SERIES GATES

LOGIC DIAGRAMS

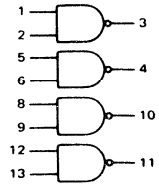
MC14001UB
Quad 2-Input NOR Gate



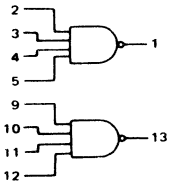
MC14002UB
Dual 4-Input NOR Gate



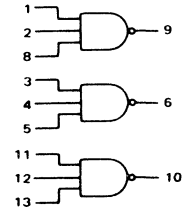
MC14011UB
Quad 2-Input NAND Gate



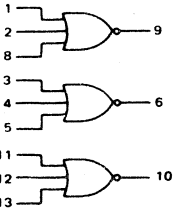
MC14012UB
Dual 4-Input NAND Gate



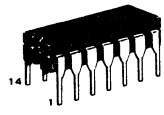
MC14023UB
Triple 3-Input NAND Gate



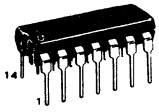
MC14025UB
Triple 3-Input NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

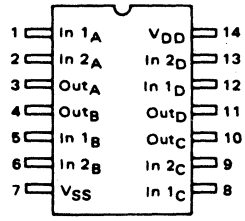
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

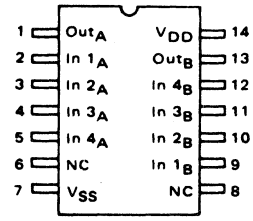
CMOS UB-SERIES GATES

PIN ASSIGNMENTS

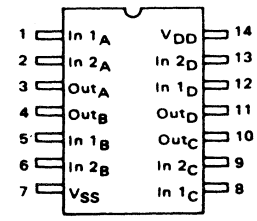
MC14001UB
Quad 2-Input NOR Gate



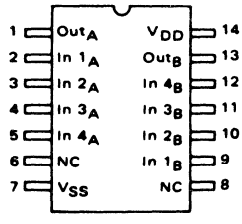
MC14002UB
Dual 4-Input NOR Gate



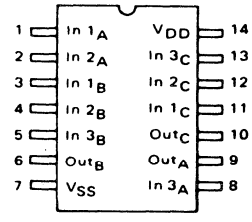
MC14011UB
Quad 2-Input NAND Gate



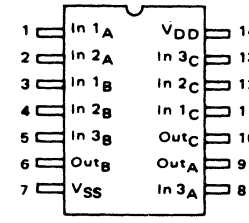
MC14012UB
Dual 4-Input NAND Gate



MC14023UB
Triple 3-Input NAND Gate



MC14025UB
Triple 3-Input NOR Gate



NC = No Connection

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}/N							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 μA/kHz) f + I_{DD}/N							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 × the number of exercised gates per package.

6

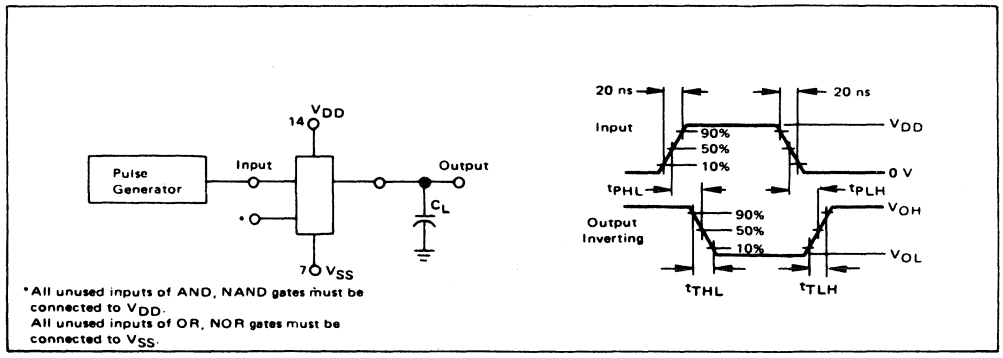
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only at 25°C.

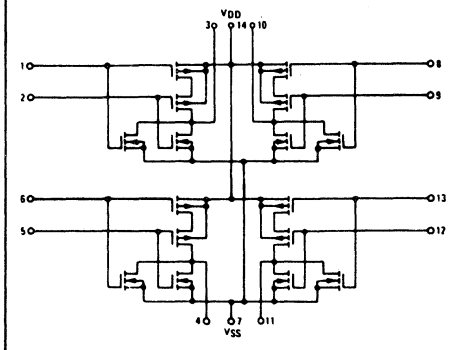
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

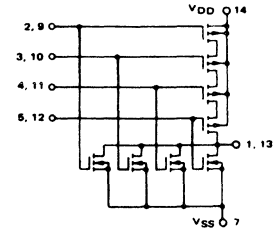


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

MC14001UB CIRCUIT SCHEMATIC

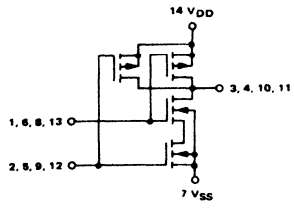


MC14002UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)

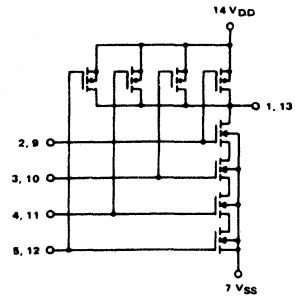


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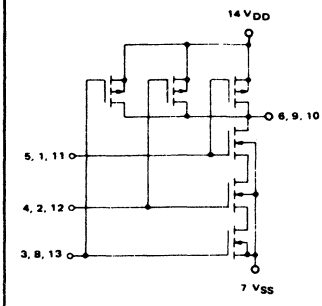
MC14011UB CIRCUIT SCHEMATIC
(1/4 of Device Shown)



MC14012UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



MC14023UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)



MC14025UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)

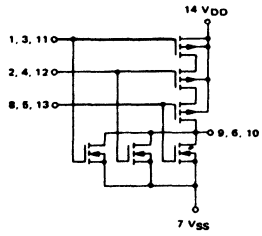


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

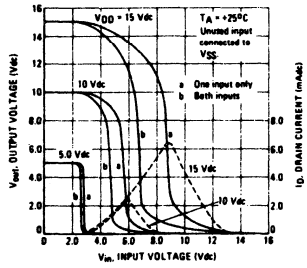


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

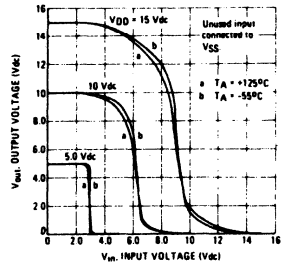


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

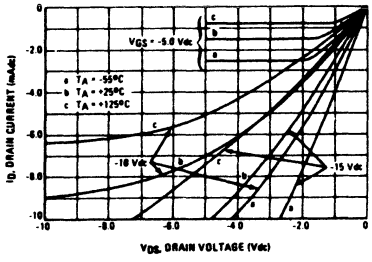
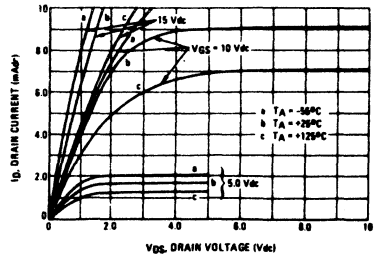


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS



6

MOTOROLA

MC14002B
MC14002UB

DUAL 4-INPUT "NOR" GATE

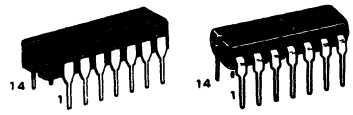
The MC14002B and MC14002UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002B and CD4002UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

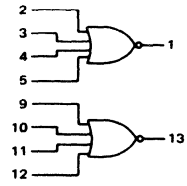
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

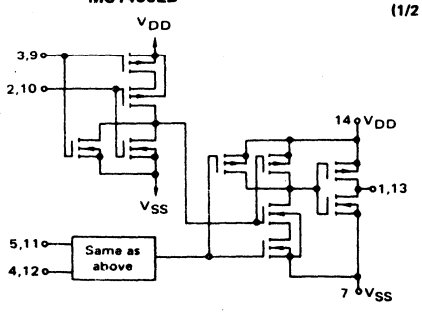
LOGIC DIAGRAM



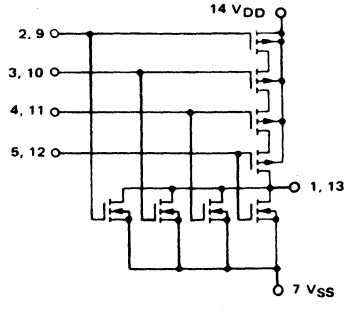
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14002B



MC14002UB



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14006B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER

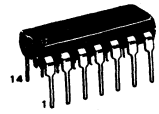
18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Fully Static Operation
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

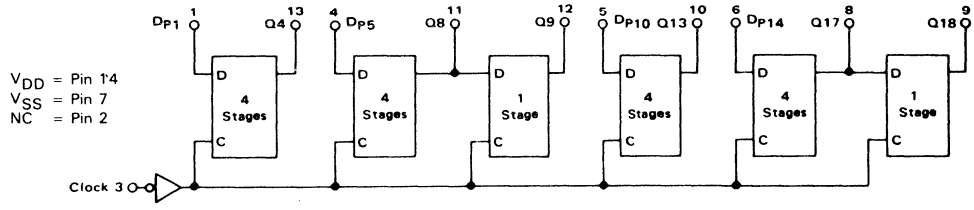
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE
(Single Stage)

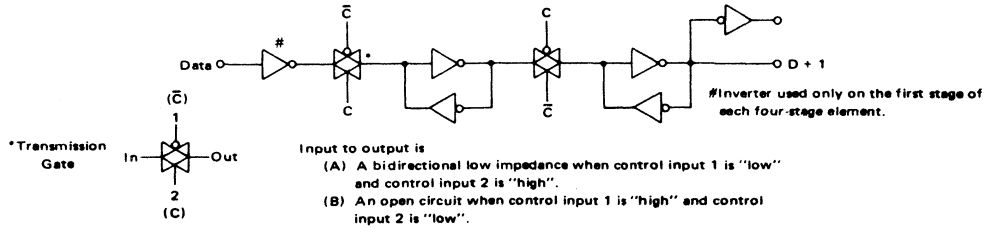
D_n	C	Q_{n+1}
0	⌒	0
1	⌒	1
X	⌒	Q_n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



#Inverter used only on the first stage of each four-stage element.

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.3 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.6 μA/kHz) f + I_{DD}							
		15	I_T = (3.9 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

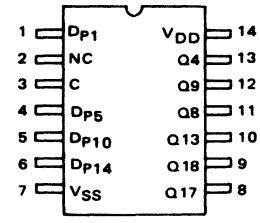
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001

PIN ASSIGNMENT



NC = No Connection

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	120	60	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	5.0	2.5	MHz
		10	–	8.3	4.2	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time**	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5	
		15	–	–	4	
Setup Time	t_{su}	5.0	0	-50	–	ns
		10	0	-15	–	
		15	0	-8.0	–	
Hold Time	t_h	5.0	180	75	–	ns
		10	90	25	–	
		15	75	20	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

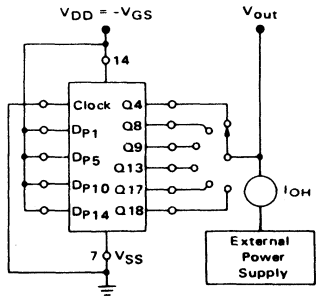
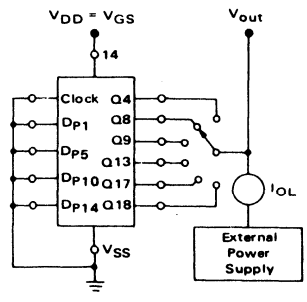


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



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FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

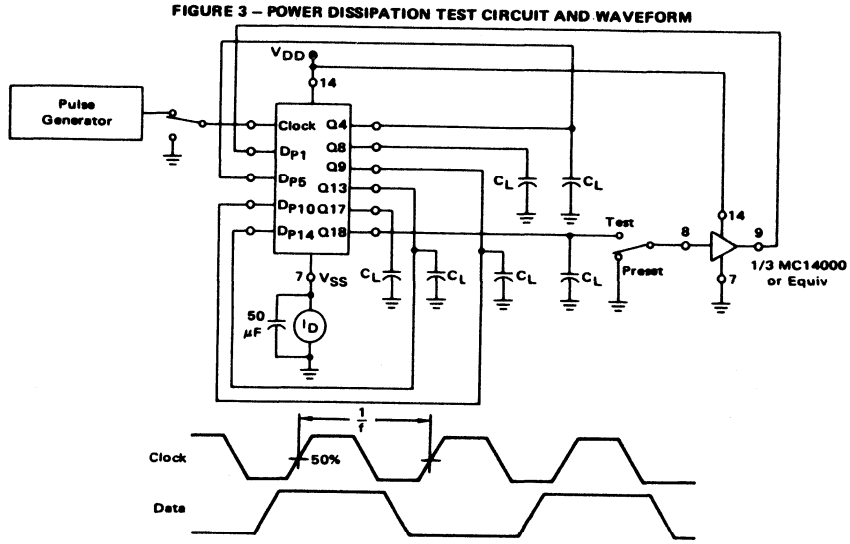
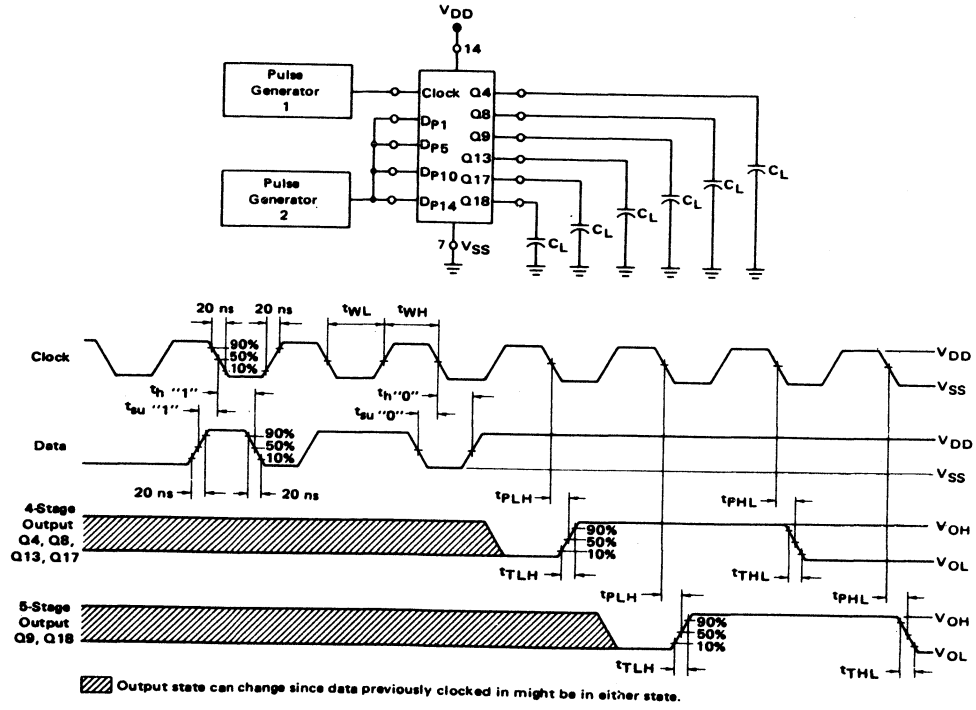


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14007UB

DUAL COMPLEMENTARY PAIR PLUS INVERTER

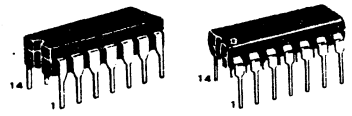
The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

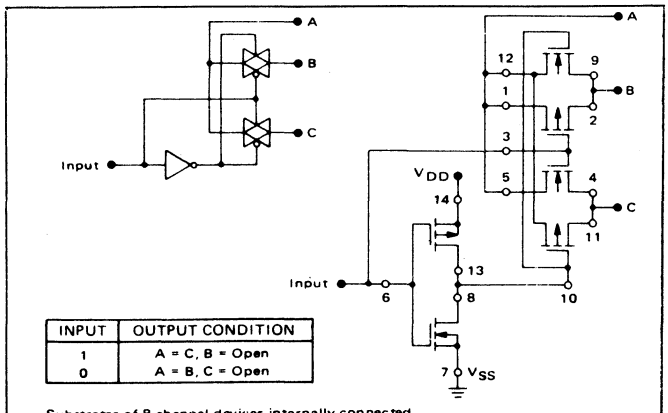
C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

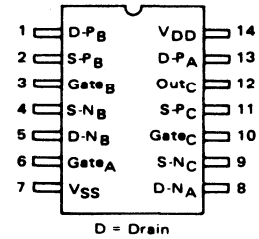
FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

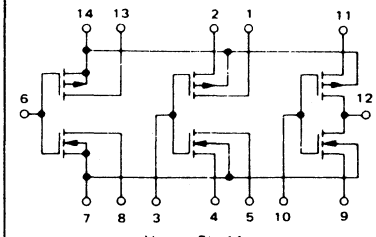
Substrates of P-channel devices internally connected to V_{DD}; substrates of N-channel devices internally connected to V_{SS}.

PIN ASSIGNMENT



D = Drain
S = Source

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

6

ELECTRICAL CHARACTERISTICS (Connected as Inverters) (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	10	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	10	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	I_T = (0.7 µA/kHz) f + I_{DD}/6							µAdc
		10	I_T = (1.4 µA/kHz) f + I_{DD}/6							
		15	I_T = (2.2 µA/kHz) f + I_{DD}/6							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

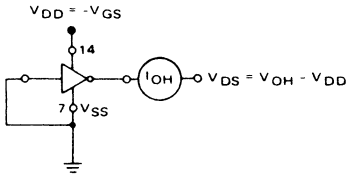
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.2 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		10	–	45	90	
t_{TLH} = (0.4 ns/pF) C_L + 15 ns		15	–	35	70	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.2 ns/pF) C_L + 15 ns		5.0	–	75	150	
t_{THL} = (0.5 ns/pF) C_L + 15 ns		10	–	40	80	
t_{THL} = (0.4 ns/pF) C_L + 10 ns		15	–	30	60	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	–	60	125	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	–	30	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	–	25	55	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	–	60	125	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	–	30	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	–	25	55	

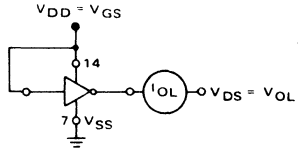
* The formulas given are for the typical characteristics only.
Switching specifications are for device connected as an inverter.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

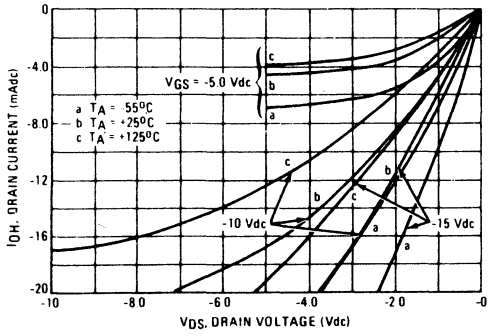


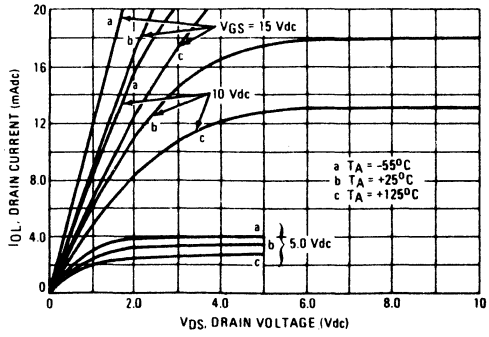
All unused inputs connected to ground.

FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS



All unused inputs connected to ground.

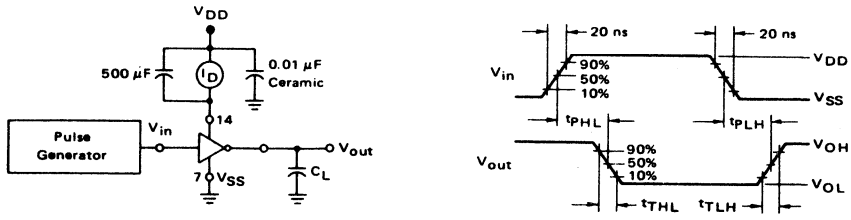




These typical curves are not guarantees, but are design aids.
Caution: The maximum current rating is 10 mA per pin.

6

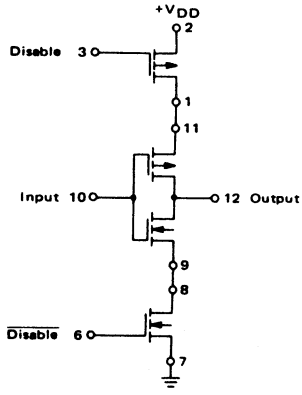
FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



APPLICATIONS

The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

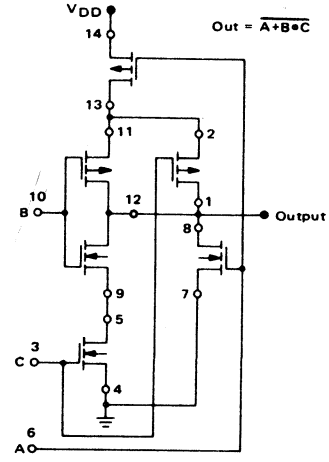
FIGURE 5 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 – AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

6

MOTOROLA

MC14008B

CMOS MSI

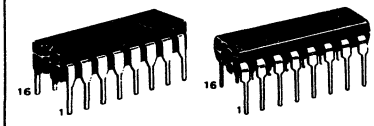
(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER

4-BIT FULL ADDER

The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

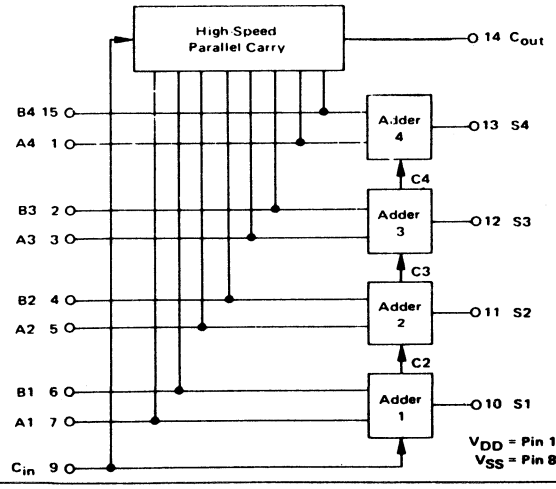
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

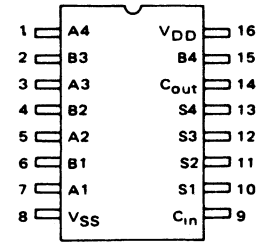
TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM



PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.4 μA/kHz) f + I_{DD}							
		15	I_T = (5.0 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	–	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

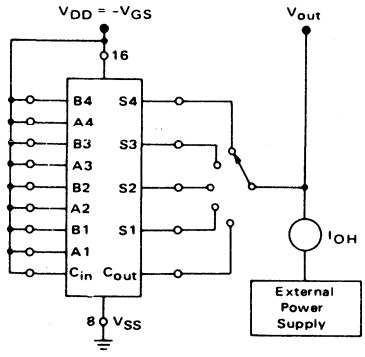
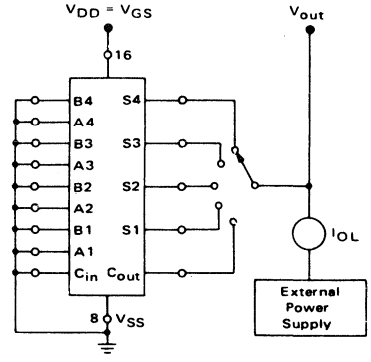


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT



6

FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

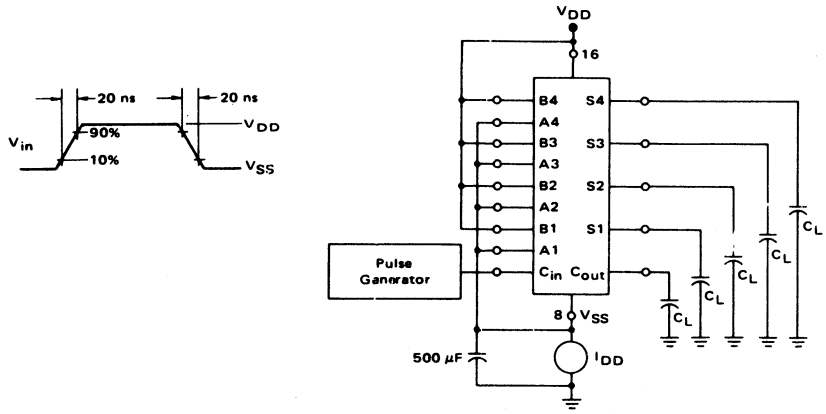


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

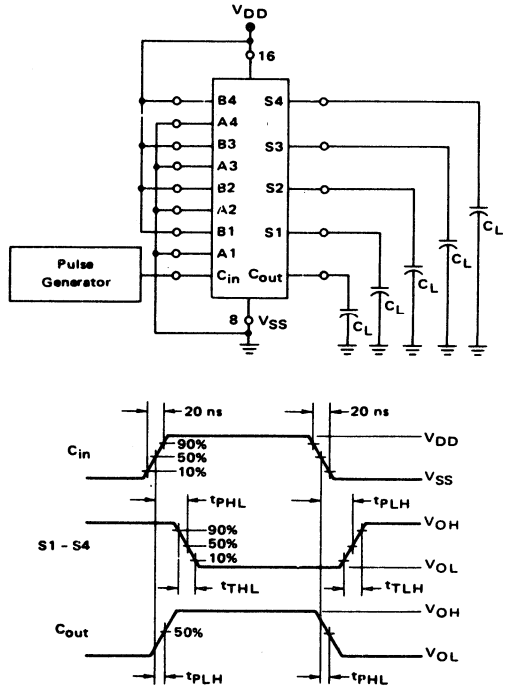
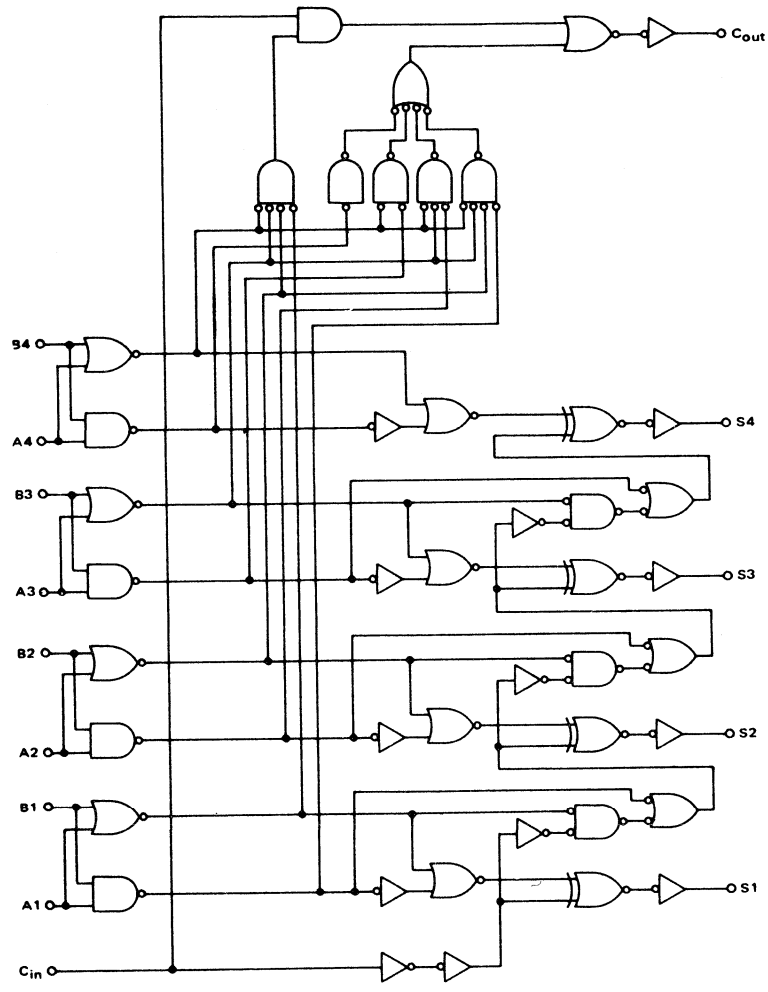
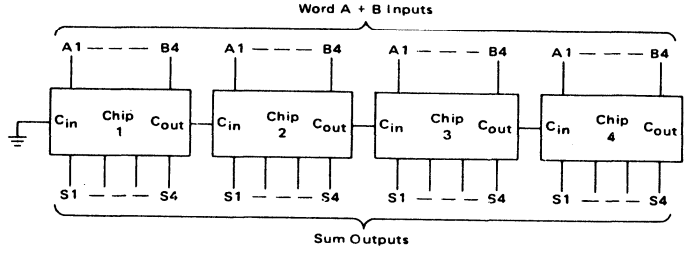


FIGURE 5 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

tp total = tp (Sum to Carry) + tp (Carry to Sum) + 2 tp (Carry to Carry)

The guaranteed 16-bit adder speed at 10 V, 25°C, C_L = 50 pF is:

t_p total = 290 + 310 + 300 = 900 ns

6

MOTOROLA

MC14011B
MC14011UB

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE

For complete data see MC14001B or MC14001UB as applicable.

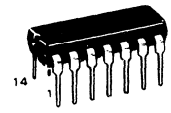
QUAD 2-INPUT "NAND" GATE

The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

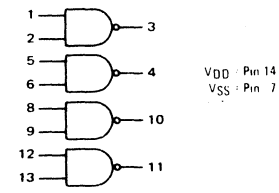
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

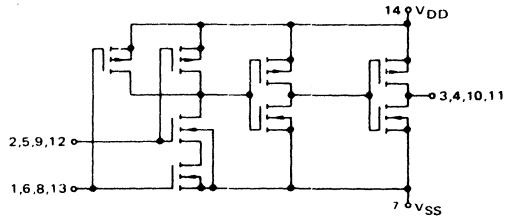
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM

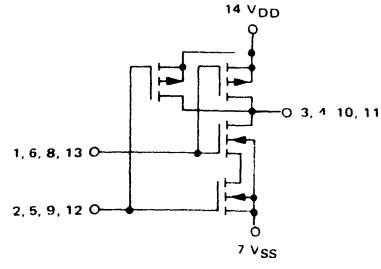


CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14011B



MC14011UB



6

MOTOROLA

MC14012B
MC14012UB

DUAL 4-INPUT "NAND" GATE

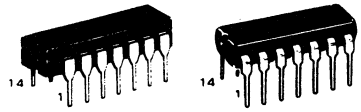
The MC14012B and MC14012UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- **Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14012B only)**
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012B and CD4012UB

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

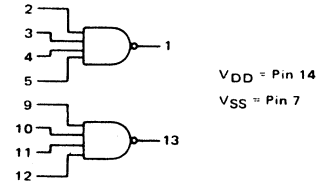
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

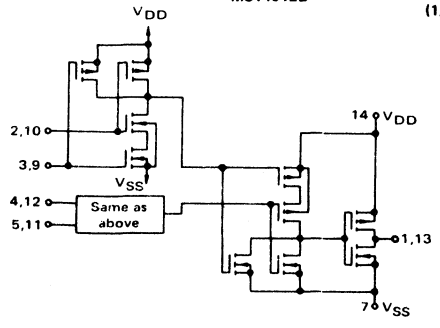
See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

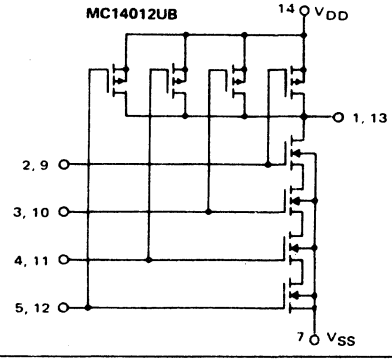


CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14012B



MC14012UB



6

MOTOROLA

MC14013B

CMOS SSI

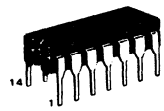
(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP

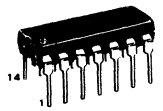
DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

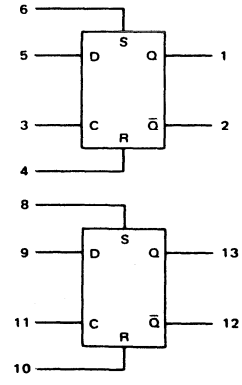
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⌐⌐	0	0	0	0	1	
⌐⌐	1	0	0	1	0	
⌐⌐	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.1	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.5 μA/kHz) f + I_{DD}							
		15	I_T = (2.3 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

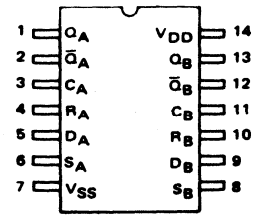
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
Clock to Q, $\overline{Q}$	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times**	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Hold Times**	t_h	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Clock Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	10	5.0	
		15	–	14	7.0	
Clock Pulse Rise and Fall Time	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Removal Times	t_{rem}					ns
Set		5	80	0	—	
		10	45	5	—	
		15	35	5	—	
Reset		5	50	−35	—	
		10	30	−10	—	
		15	25	−5	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and 70 ns with 15 V.

LOGIC DIAGRAM
(1/2 of Device Shown)

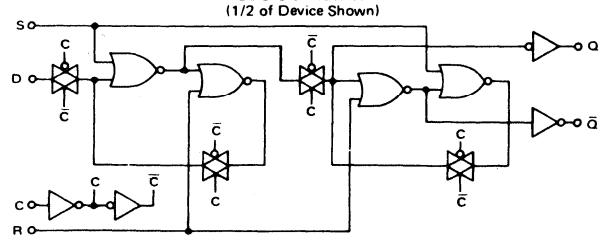
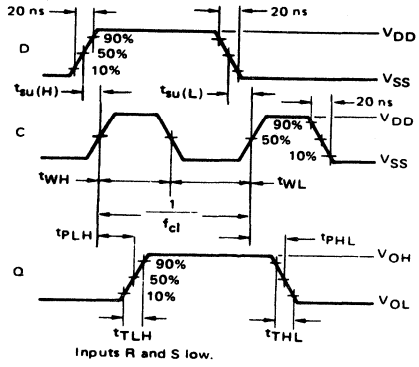
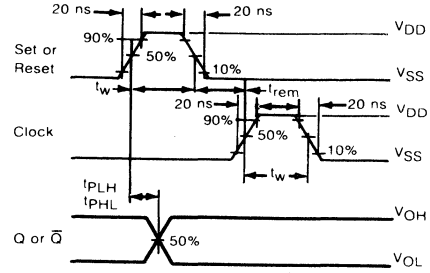


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)



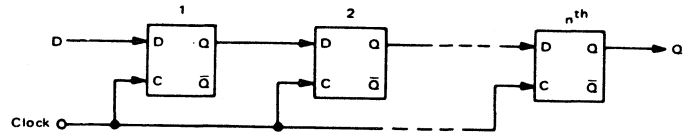
Inputs R and S low.

FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, Clock, and Output)

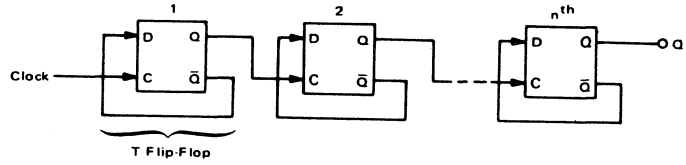


TYPICAL APPLICATIONS

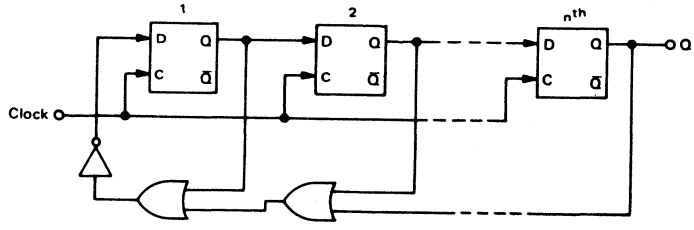
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



6

MOTOROLA

MC14014B
MC14021B

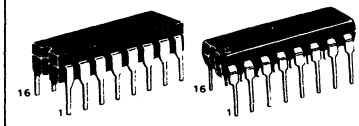
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

SERIAL OPERATION:

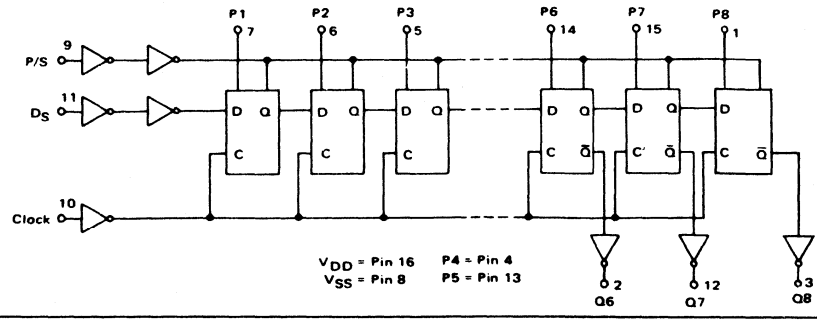
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐⌐	0	0	0	?	?
n+1	⌐⌐	1	0	1	0	?
n+2	⌐⌐	0	0	0	1	0
n+3	⌐⌐	1	0	1	0	1
·	⌐⌐	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK MC14014B	CLOCK MC14021B	D_S	P/S	P_n	$*Q_n$
⌐⌐	X	X	1	0	0
⌐⌐	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

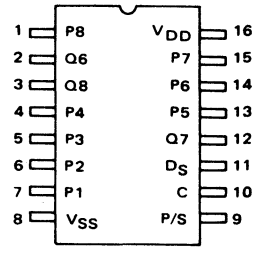
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0015.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



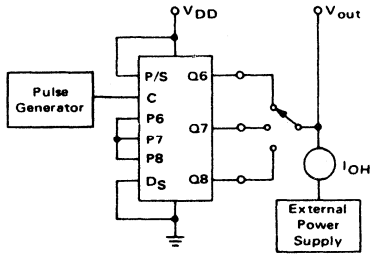
SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time (Clock to Q, P/S to Q)	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	—	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	—	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0	400	150	—	ns
		10	175	75	—	
		15	135	40	—	
Clock Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Parallel/Serial Control Pulse Width	t_{WH}	5.0	400	150	—	ns
		10	175	75	—	
		15	135	40	—	
Setup Time	t_{su}	5.0	200	100	—	ns
P/S to Clock		10	100	50	—	
		15	80	40	—	
Hold Time	t_h	5.0	20	−2.5	—	ns
Clock to P/S		10	20	−10	—	
		15	25	0	—	
Setup Time	t_{su}	5.0	350	150	—	ns
Data (Parallel or Serial) to		10	80	50	—	
Clock or P/S		15	60	30	—	
Hold Time	t_h	5.0	45	0	—	ns
Clock to D_S		10	35	0	—	
		15	35	5	—	
Hold Time	t_h	5.0	50	25	—	ns
Clock to P_n		10	45	20	—	
		15	45	20	—	
Input Clock Rise Time	$t_{r(cl)}$	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	

*The formulas given are for the typical characteristics only at 25°C.

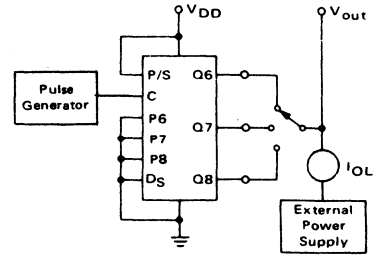
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT



Preset output under test to a logic "1" level.

FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT



6

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

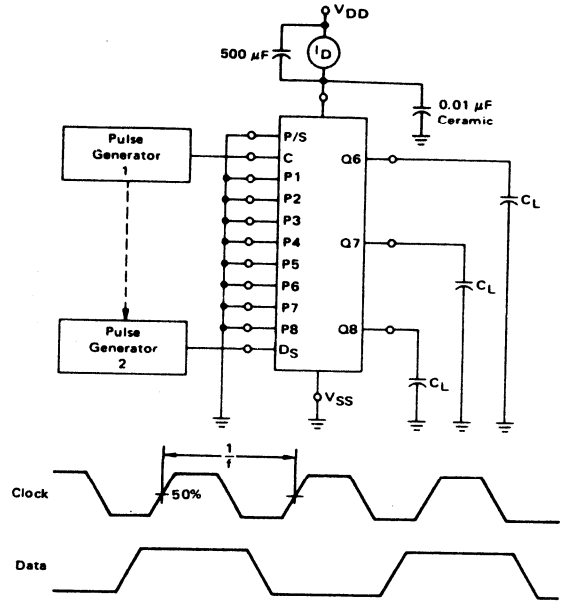
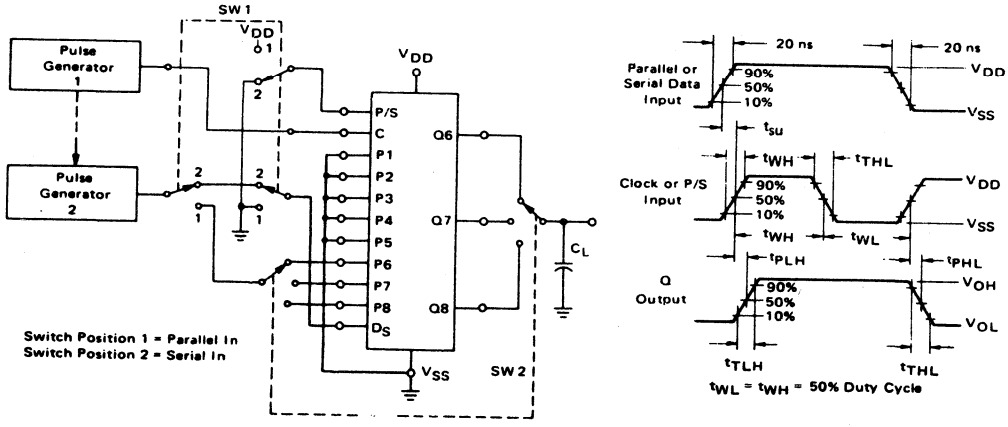


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

MOTOROLA

MC14015B

CMOS MSI

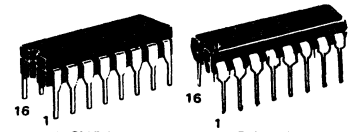
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

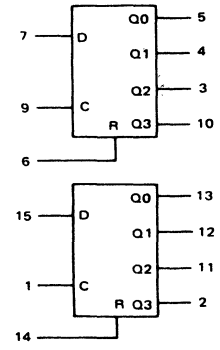
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

TRUTH TABLE

C	D	R	Q0	Q_n
⌐⌐	0	0	0	Q_{n-1}
⌐⌐	1	0	1	Q_{n-1}
⌐⌐	X	0	No Change	No Change
X	X	1	0	0

X = Don't Care
Q_n = Q0, Q1, Q2, or Q3, as applicable.
Q_{n-1} = Output of prior stage.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

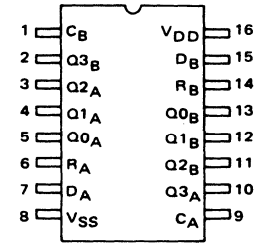
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pf, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock, Data to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 225 ns		5.0	–	310	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	170	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 375 ns		5.0	–	460	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	170	
Clock Pulse Width	t_{WH}	5.0	400	185	—	ns
		10	175	85	—	
		15	135	55	—	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	7.5	3.75	
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Reset Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	160	80	–	
		15	120	60	–	
Setup Time	t_{su}	5.0	350	100	–	ns
		10	100	50	–	
		15	75	40	–	

*The formulas given are for typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

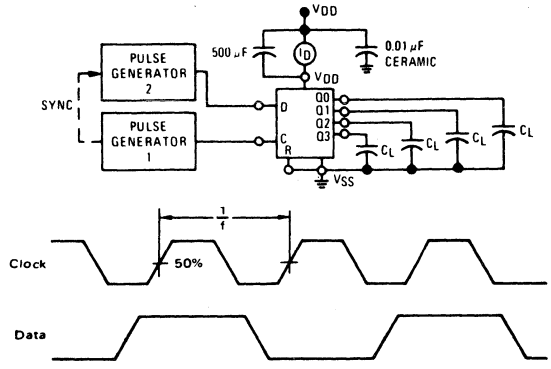


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

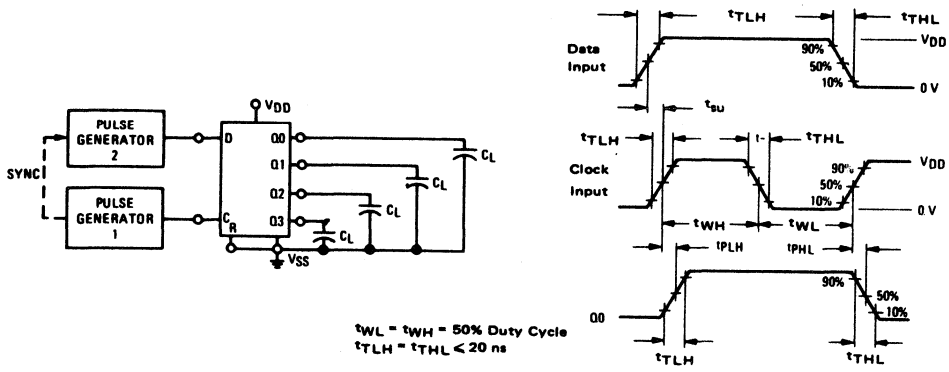
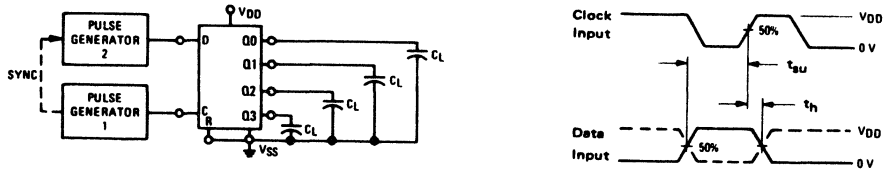
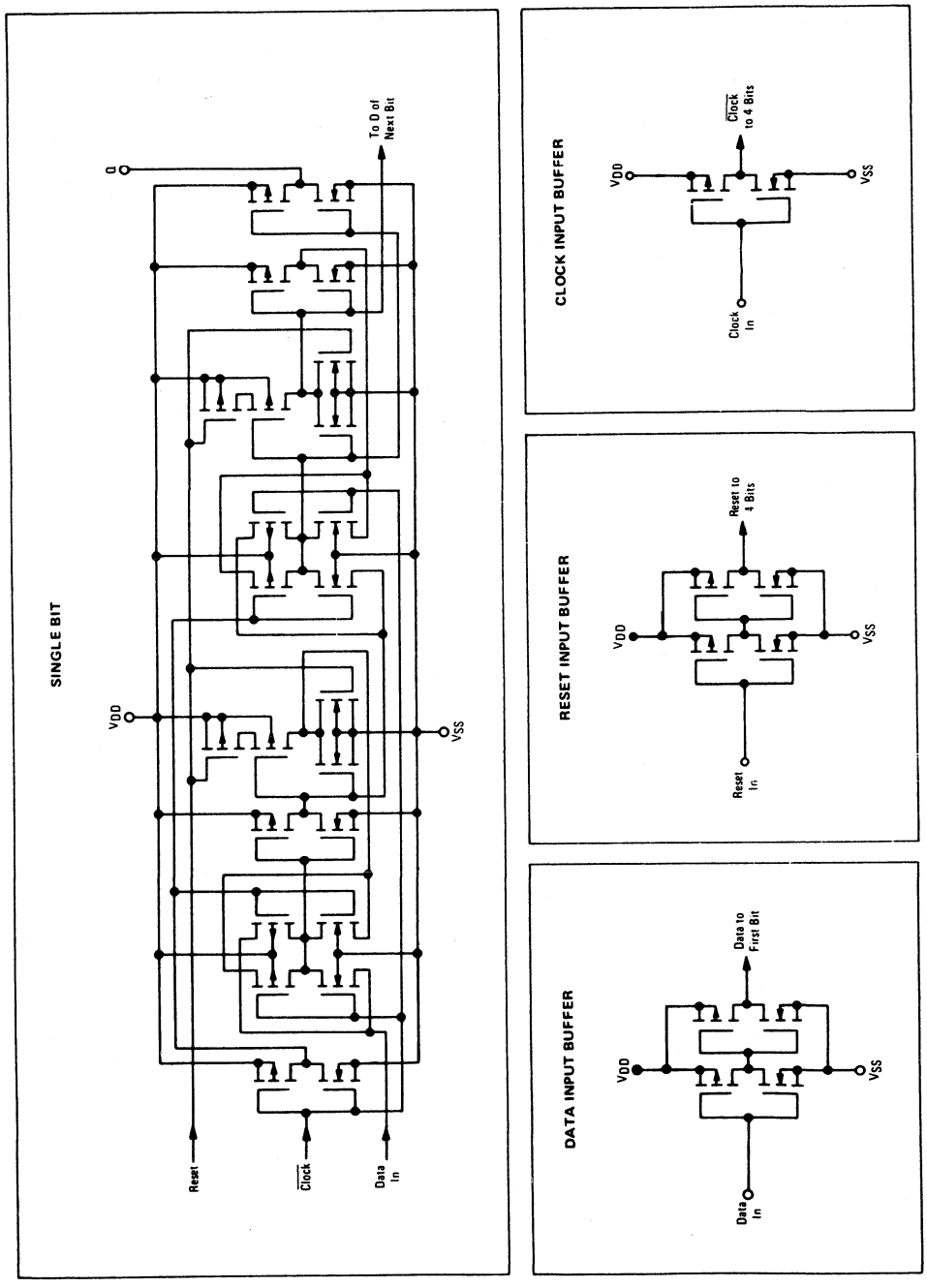


FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS

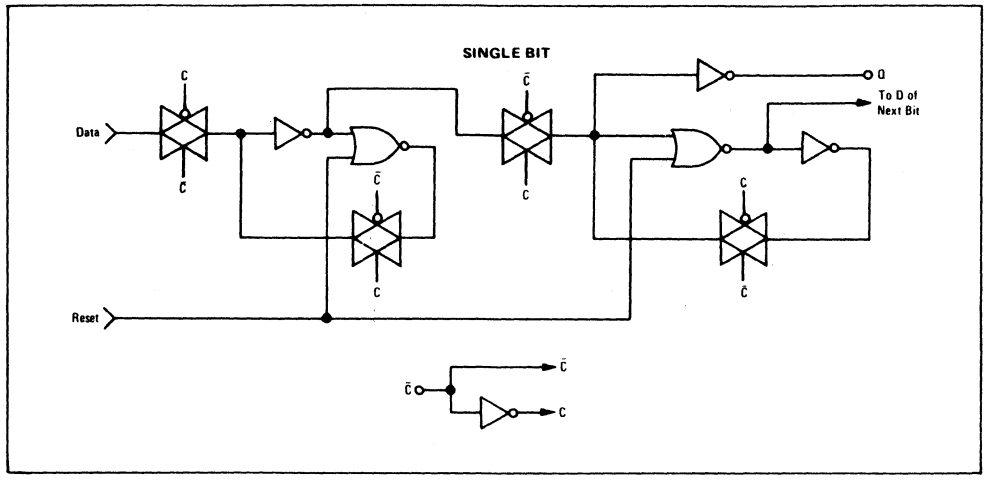


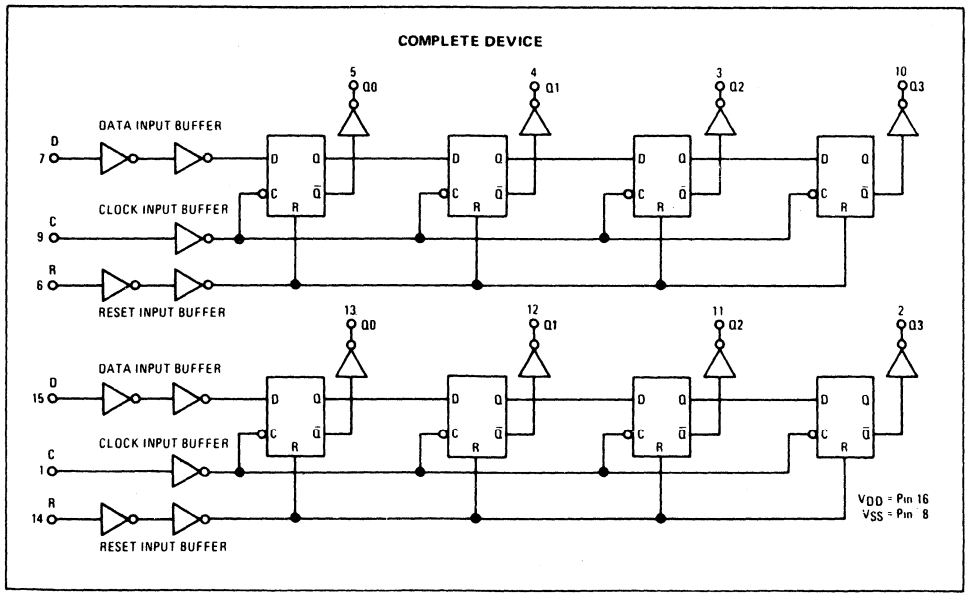
6

CIRCUIT SCHEMATICS



LOGIC DIAGRAMS





MOTOROLA

MC14016B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

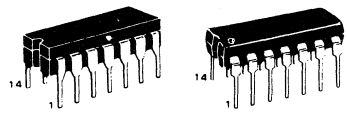
The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise – $12nV/\sqrt{Cycle}$, f≥1 kHz typical
- Pin-for-Pin Replacement for CD4016B, CD4066B
- For Lower R_{ON}, Use The HC4016 High-Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

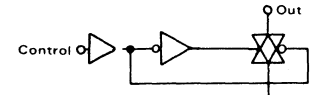
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

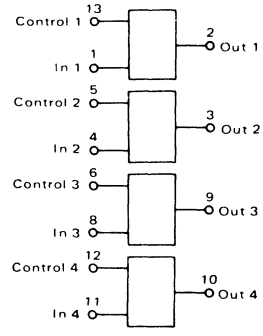
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} < V_{out} \leq V_{DD}$

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CONTROL	SWITCH
0 = V_{SS}	OFF
1 = V_{DD}	ON

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristics	Figure	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage	1	V_{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
Control Input			10	–	–	–	1.5	0.9	–	–	
			15	–	–	–	1.5	0.9	–	–	
		V_{IH}	5.0	–	–	3.0	2.0	–	–	–	Vdc
			10	–	–	8.0	6.0	–	–	–	
			15	–	–	13	11	–	–	–	
Input Current (AL Device) Control	–	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control	–	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance	–	C_{in}									pF
Control			–	–	–	–	5.0	–	–	–	
Switch Input			–	–	–	–	5.0	–	–	–	
Switch Output			–	–	–	–	5.0	–	–	–	
Feed Through			–	–	–	–	0.2	–	–	–	
Quiescent Current (AL Device)**	2,3	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)			10	–	0.50	–	0.0010	0.50	–	15	
			15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)**	2,3	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)			10	–	2.0	–	0.0010	2.0	–	15	
			15	–	4.0	–	0.0015	4.0	–	30	
"ON" Resistance (AL Device)**	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, R_L = 10 kΩ)											
(V_{in} = +5.0 Vdc)			5.0	–	600	–	300	660	–	960	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)				–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			7.5	–	360	–	240	400	–	600	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)				–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	600	–	310	660	–	960	
(V_{in} = +5.6 Vdc)				–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)				–	360	–	300	400	–	600	
"ON" Resistance (CL/CP Device)**	4,5,6	R_{ON}									Ohms
($V_C = V_{DD}$, R_L = 10 kΩ)											
(V_{in} = +5.0 Vdc)			5.0	–	610	–	300	660	–	840	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)				–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			7.5	–	370	–	240	400	–	520	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)				–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)				–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)				–	370	–	300	400	–	520	
Δ"ON" Resistance	–	ΔR_{ON}									Ohms
Between any 2 circuits in a common package											
($V_C = V_{DD}$)											
(V_{in} = ±5.0 Vdc) V_{SS} = –5 Vdc			5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc) V_{SS} = –7.5 Vdc			7.5	–	–	–	10	–	–	–	
Input/Output Leakage Current ($V_C = V_{SS}$)	–	–									µAdc
(V_{in} = +7.5, V_{out} = –7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	
(V_{in} = –7.5, V_{out} = +7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

NOTE: All unused inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc) V_{in} to V_{out} (V_C = V_{DD}, R_L = 10 kΩ)	7	t_{PLH}, t_{PHL}	5.0 10 15	– – –	15 7.0 6.0	45 15 12	ns
Control to Output (V_{in} ≤ 10 Vdc, R_L = 1.0 kΩ)	8	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	– – –	34 20 15	90 45 35	ns
Crosstalk, Control to Output (V_{SS} = 0 Vdc) (V_C = V_{DD}, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ, f = 1kHz)	9	–	5.0 10 15	– – –	30 50 100	– – –	mV
Crosstalk between any two switches (V_{SS} = 0 Vdc) (R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20 \log_{10}\frac{V_{out1}}{V_{out2}}$)	–	–	5.0	–	-80	–	dB
Noise Voltage (V_{SS} = 0 Vdc) (V_C = V_{DD}, f = 100 Hz) (V_C = V_{DD}, f = 100 kHz)	10,11	–	5.0 10 15 5.0 10 15	– – – – – –	24 25 30 12 12 15	– – – – – –	nV/√Cycle
Second Harmonic Distortion (V_{SS} = −5 Vdc) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	–	5.0	–	0.16	–	%
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = -5 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz) I_{loss} = $20 \log_{10}\frac{V_{out}}{V_{in}}$) ($R_L$ = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12	–	5.0	– – – –	 2.3 0.2 0.1 0.05	 – – – –	dB
Bandwidth (-3 dB) (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = -5 Vdc, RMS centered @ 0.0 Vdc) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	12,13	BW	5.0	– – – –	 54 40 38 37	 – – – –	MHz
OFF Channel Feedthrough Attenuation (V_{SS} = −5 Vdc) (V_C = V_{SS}, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -50 dB) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	–	–	5.0	– – – –	 1250 140 18 2.0	 – – – –	kHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

PIN ASSIGNMENT

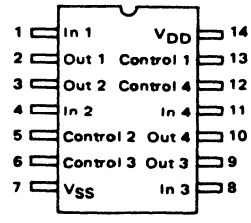
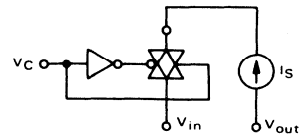


FIGURE 1 – INPUT VOLTAGE TEST CIRCUIT



V_{IL}: V_C is raised from V_{SS} until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10$ μA with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

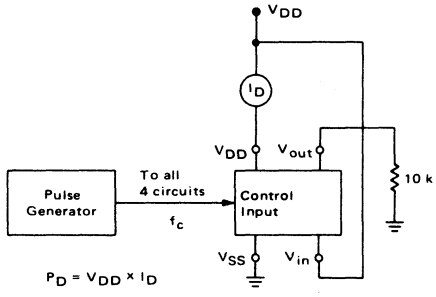
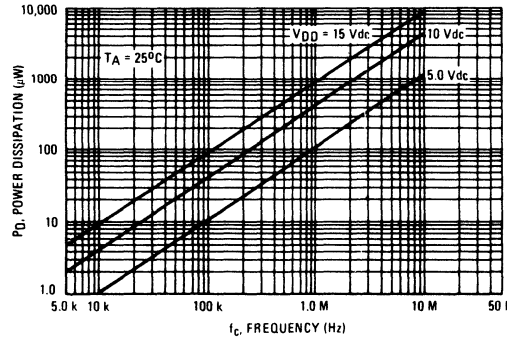


FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – V_{SS} = –5.0 V AND –7.5 V

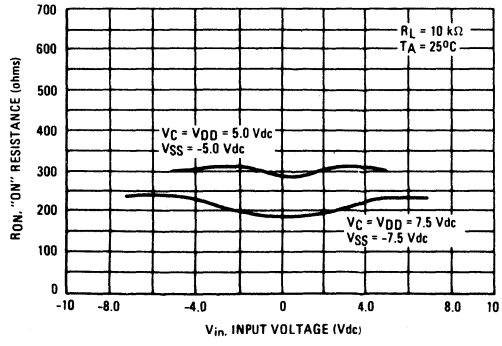
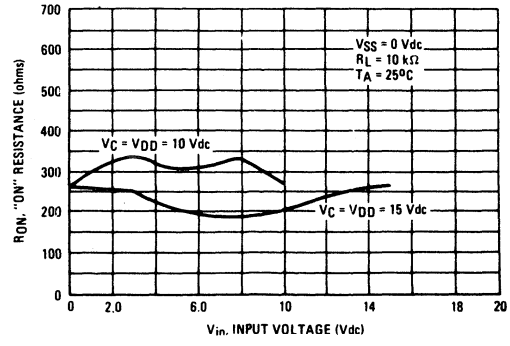


FIGURE 5 – V_{SS} = 0 V



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FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

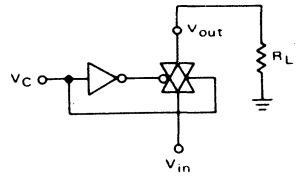


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

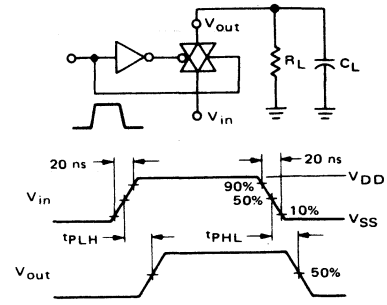


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

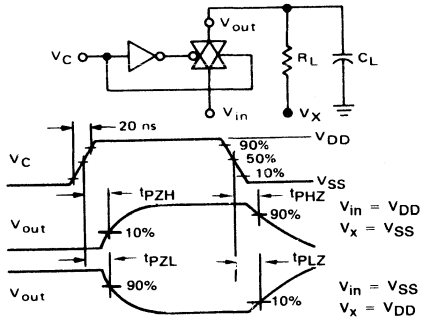


FIGURE 9 – CROSSTALK TEST CIRCUIT

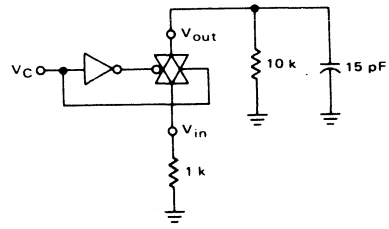


FIGURE 10 – NOISE VOLTAGE TEST CIRCUIT

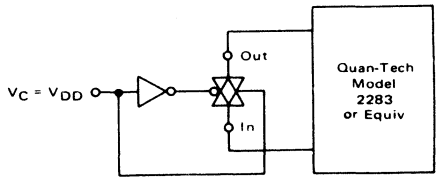
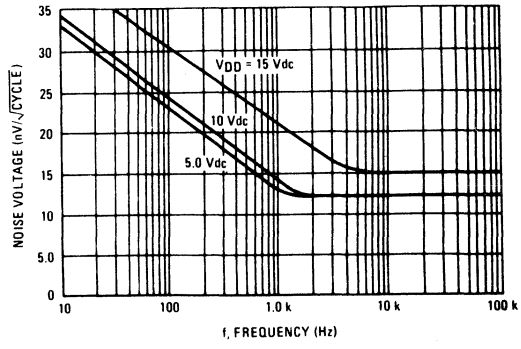


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS



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FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

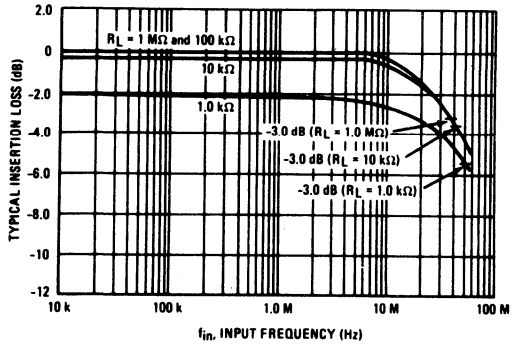


FIGURE 13 – FREQUENCY RESPONSE TEST CIRCUIT

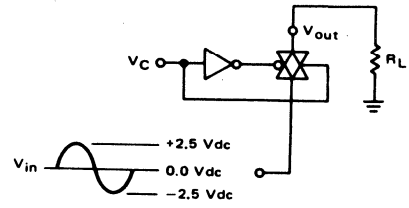
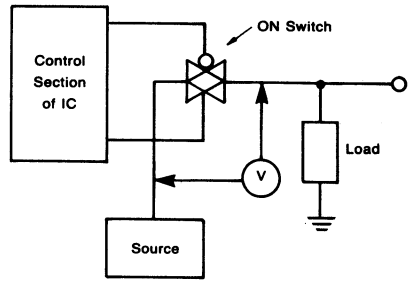


FIGURE 14 — ΔV ACROSS SWITCH



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APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5V = logic high at the control inputs; V_{SS} = GND = 0V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing neither higher than V_{DD} nor lower than V_{SS}.

The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0V. Most parameters are specified up to 15V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

FIGURE A — APPLICATION EXAMPLE

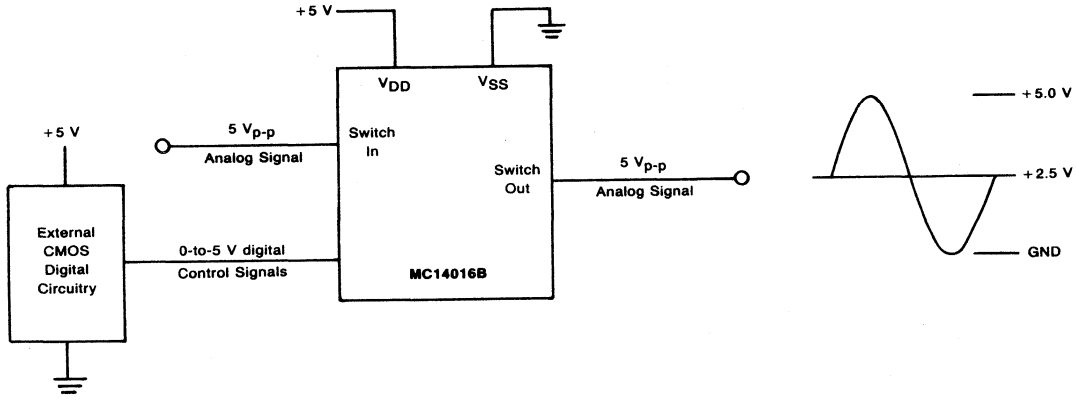
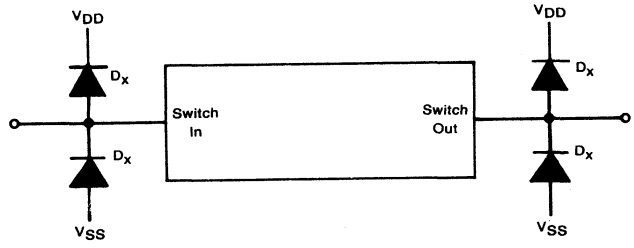


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



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MOTOROLA

MC14017B

DECADE COUNTER

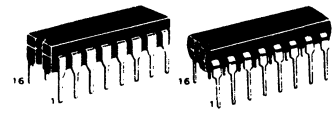
The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

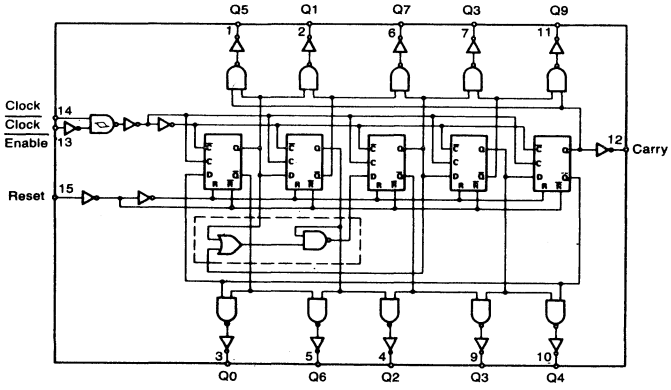
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

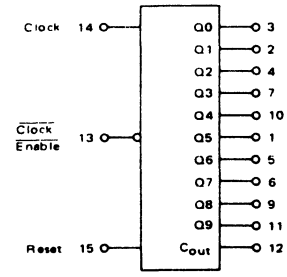
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
↓	0	0	n+1
↓	X	0	n
X	↑	0	n
1	↓	0	n+1

X = Don't Care If n < 5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15		20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.27 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.55 μA/kHz) f + I_{DD}							
		15	I_T = (0.83 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

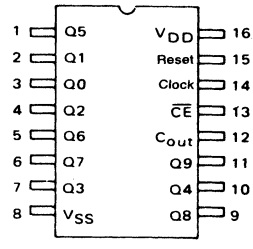
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0011.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

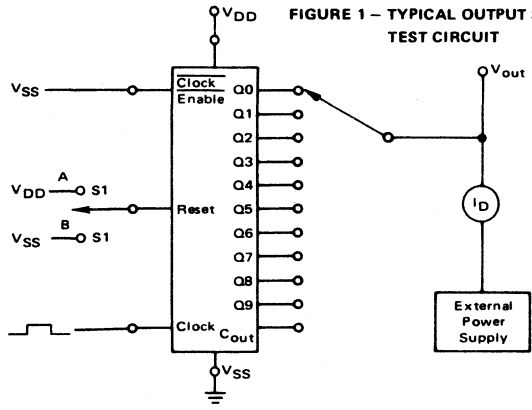
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decade Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	$t_{w(H)}$	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	$t_{w(H)}$	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH},	5.0				–
	t_{THL}	10		No Limit		
		15				
Clock Enable Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
Clock Enable Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

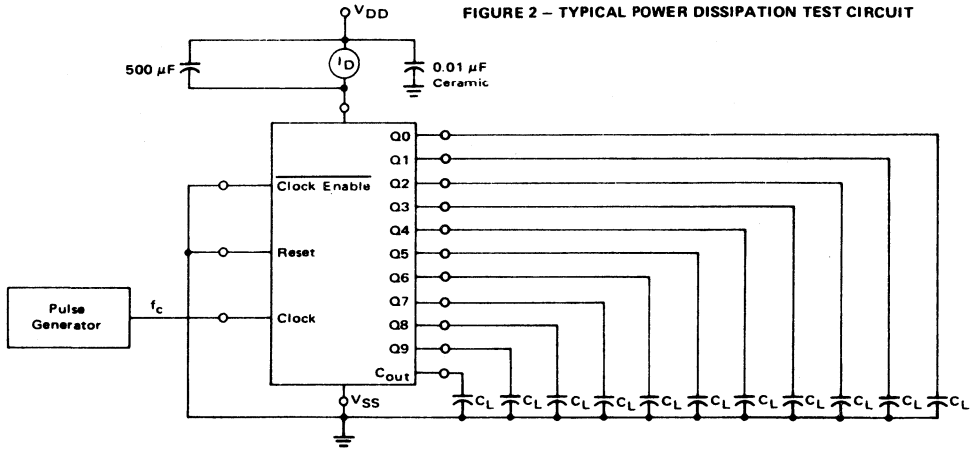
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FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

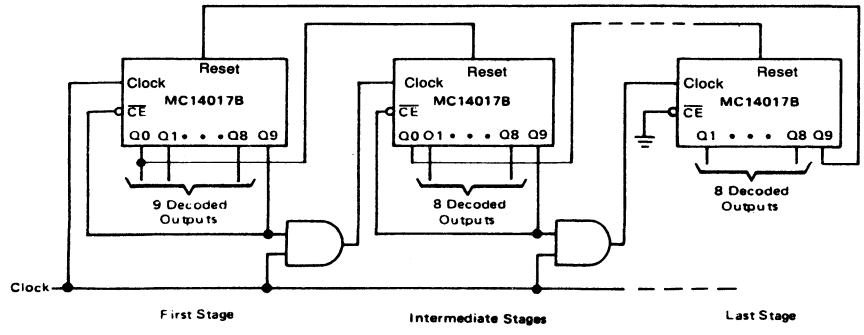
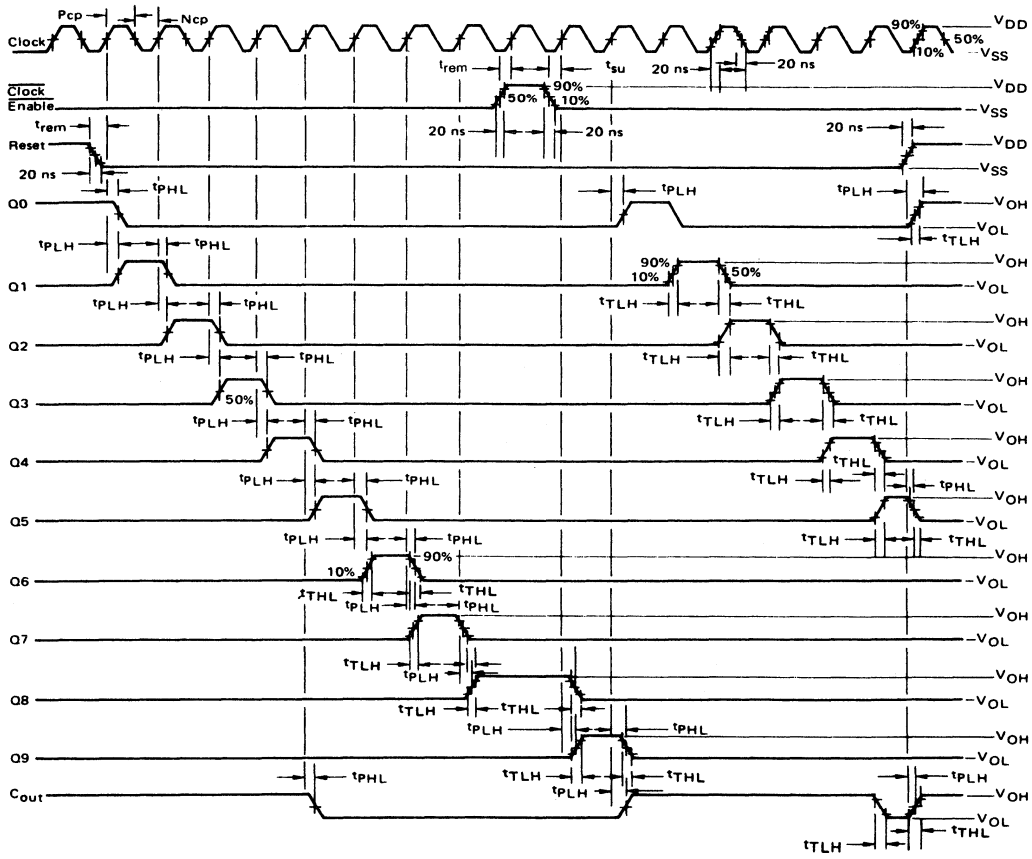


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA

MC14018B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE DIVIDE-BY-N COUNTER

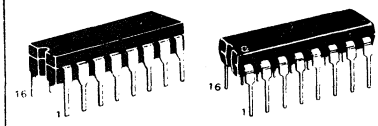
PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

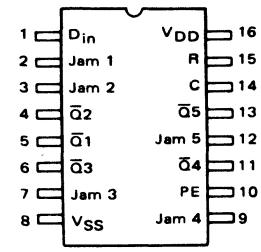
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
↓	0	0	X	$\overline{Q}n$
↑	0	0	X	$\overline{D}_n$*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5			pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10		10	–	0.010	10		300	
		15		20	–	0.015	20		600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20		150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (0.7\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

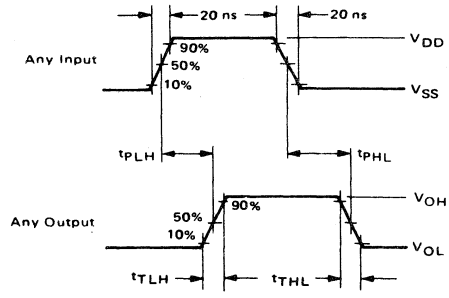
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to $\overline{Q}$						
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	–	310	620	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	–	120	240	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Setup Time	t_{su}					ns
Data (Pin 1) to Clock		5.0	200	0	–	
		10	100	0	–	
		15	80	0	–	
Jam Inputs to Preset Enable		5.0	200	0	–	ns
		10	100	0	–	
		15	80	0	–	
Data (Jam Inputs)-to-Preset Enable Hold Time	t_h	5.0	540	270	–	ns
		10	500	250	–	
		15	480	240	–	
Clock Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	200	100	–	
		15	160	80	–	
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	–	ns
		10	130	65	–	
		15	110	55	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Clock Pulse Frequency	f_{cl}					MHz
		5.0	–	2.5	1.25	
		10	–	6.5	3.25	
		15	–	8.0	4.0	

*The formulas given are for typical characteristics only at 25°C.

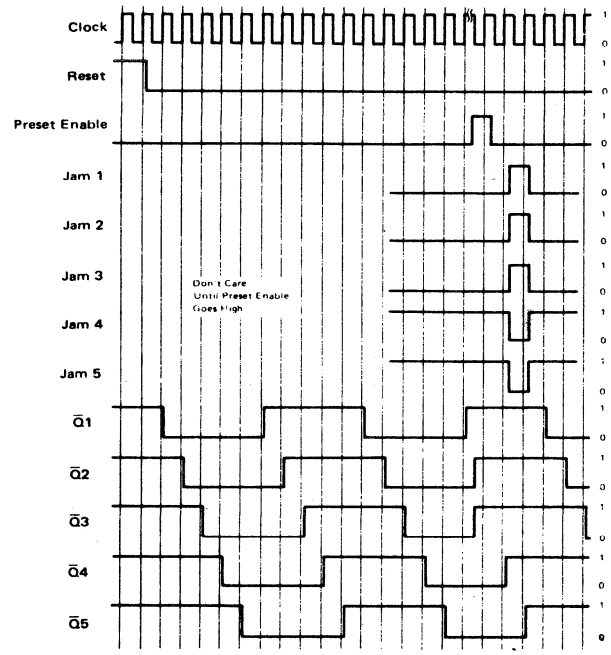
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME WAVEFORMS



6

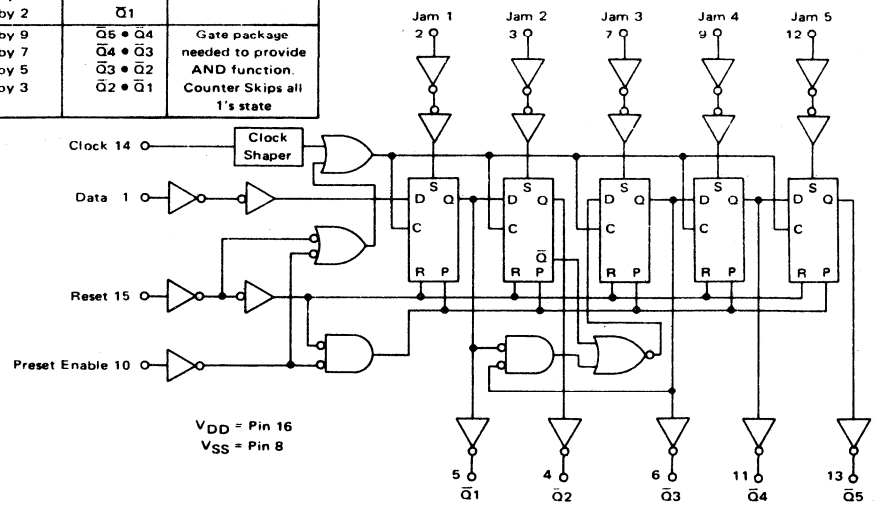
TIMING DIAGRAM
($\overline{Q}5$ Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10	$\overline{Q}5$	No external components needed.
Divide by 8	$\overline{Q}4$	
Divide by 6	$\overline{Q}3$	
Divide by 4	$\overline{Q}2$	
Divide by 2	$\overline{Q}1$	
Divide by 9	$\overline{Q}5 \bullet \overline{Q}4$	Gate package needed to provide AND function. Counter Skips all 1's state
Divide by 7	$\overline{Q}4 \bullet \overline{Q}3$	
Divide by 5	$\overline{Q}3 \bullet \overline{Q}2$	
Divide by 3	$\overline{Q}2 \bullet \overline{Q}1$	

LOGIC DIAGRAM



MOTOROLA

MC14020B

14-BIT BINARY COUNTER

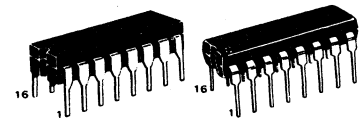
The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

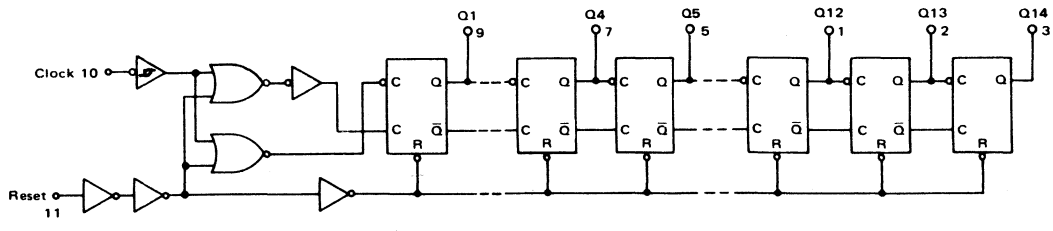
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13
Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15
V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

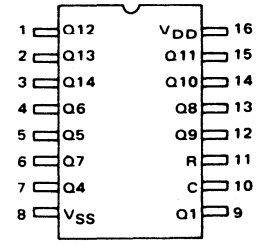
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{dc}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					
Clock to Q1	t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 175 ns		5.0	—	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 82 ns		10	—	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 55 ns		15	—	80	160	
Clock to Q14						ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 1735 ns		5.0	—	1820	3900	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 772 ns		10	—	805	1725	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 535 ns		15	—	560	1200	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 285 ns		5.0	—	370	740	
t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	—	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0	500	140	—	ns
		10	165	55	—	
		15	125	38	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.0	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			—
		10				
		15				
Reset Pulse Width	t_{WL}	5.0	3000	320	—	ns
		10	550	120	—	
		15	420	80	—	
Reset Removal Time	t_{rem}	5.0	130	65	—	ns
		10	50	25	—	
		15	30	15	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

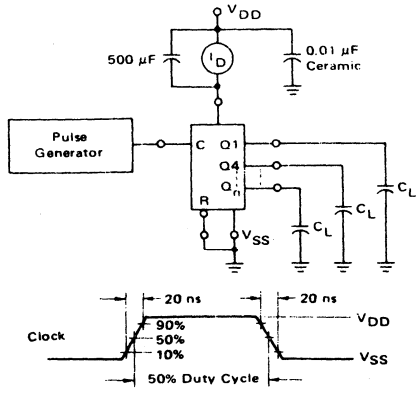
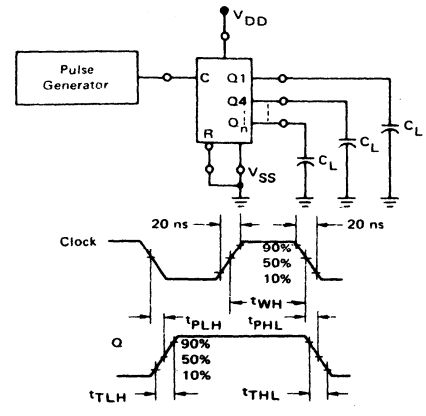
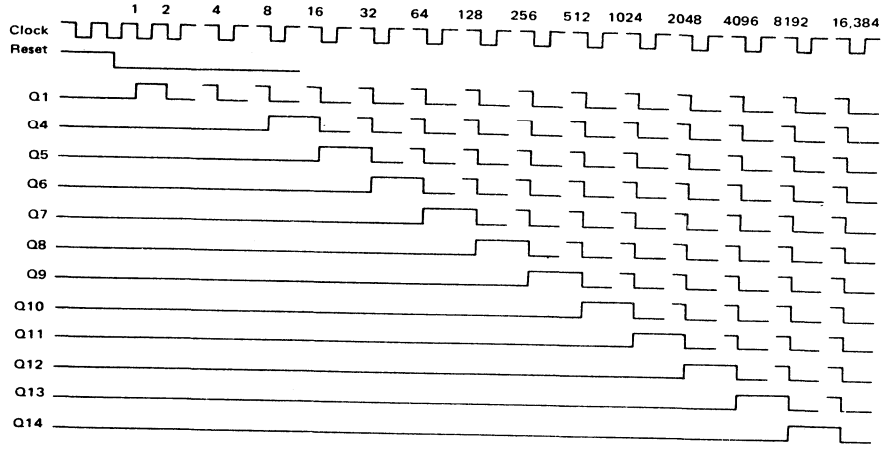


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

FIGURE 3 – TIMING DIAGRAM



MOTOROLA

MC14021B

FOR COMPLETE DATA
SEE MC14014B

CMOS MSI

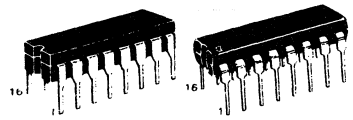
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- **Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range**
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

SERIAL OPERATION:

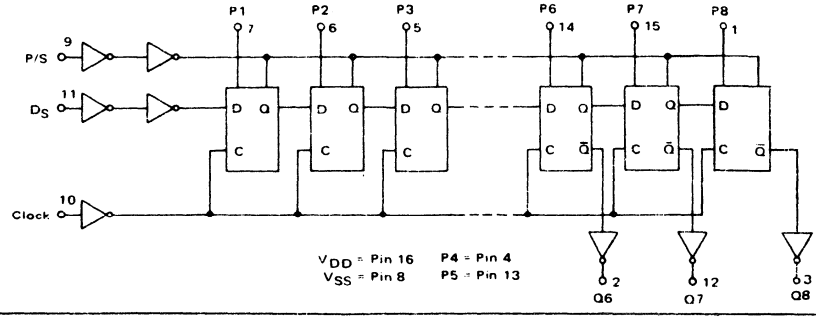
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK		D_S	P/S	P_M	$*Q_M$
MC14014B	MC14021B				
	X	X	1	0	0
	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



6

MOTOROLA

MC14022B

CMOS MSI

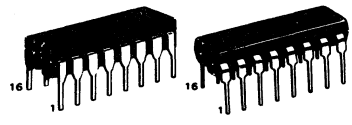
(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER

OCTAL COUNTER

The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

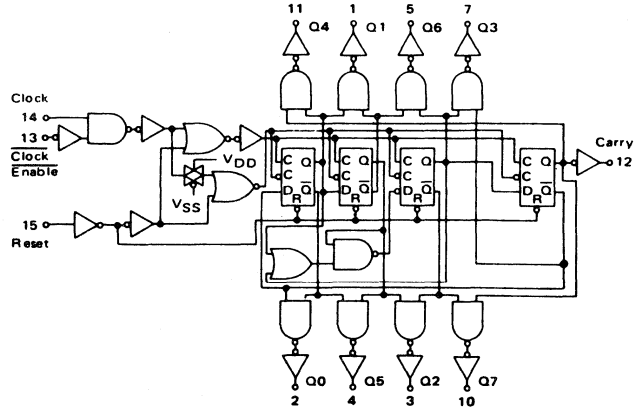
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

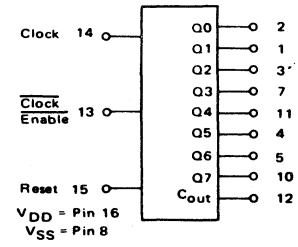
CLOCK	$\overline{\text{CLOCK}}$ $\overline{\text{ENABLE}}$	RESET	OUTPUT - n
0	X	0	n
X	1	0	n
⌐	0	0	n+1
¬	X	0	n
1	⌐	0	n+1
X	¬	0	n
X	X	1	Q0

X Don't Care If n< 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



NC = Pin 6,9

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.28 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.56 µA/kHz) f + I_{DD}							
		15	I_T = (0.85 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

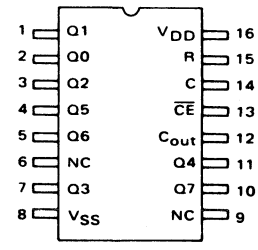
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.00125.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



NC = No Connection

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

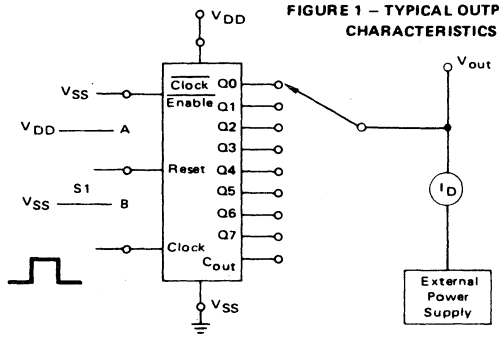
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	275	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	125	460	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 150 ns		15	–	95	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
$\overline{\text{Clock Enable}}$ Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
$\overline{\text{Clock Enable}}$ Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

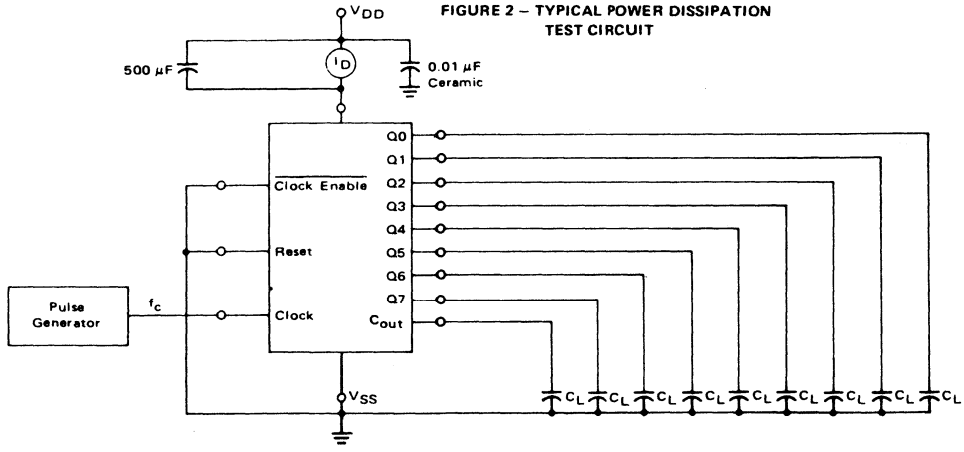
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FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	Output Sink Drive	Output Source Drive
Outputs	(S1 to A)	Clock to desired Output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

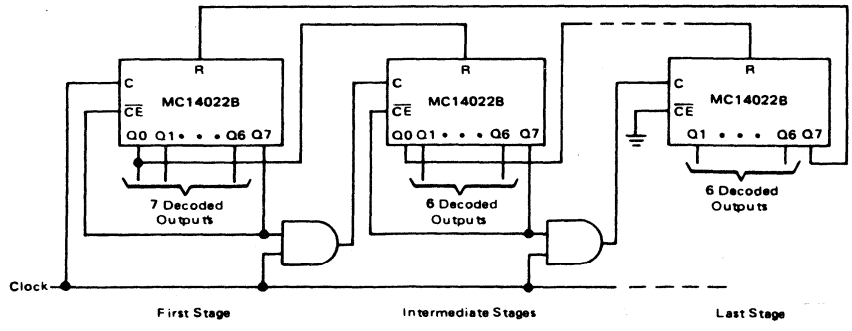
FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION



6

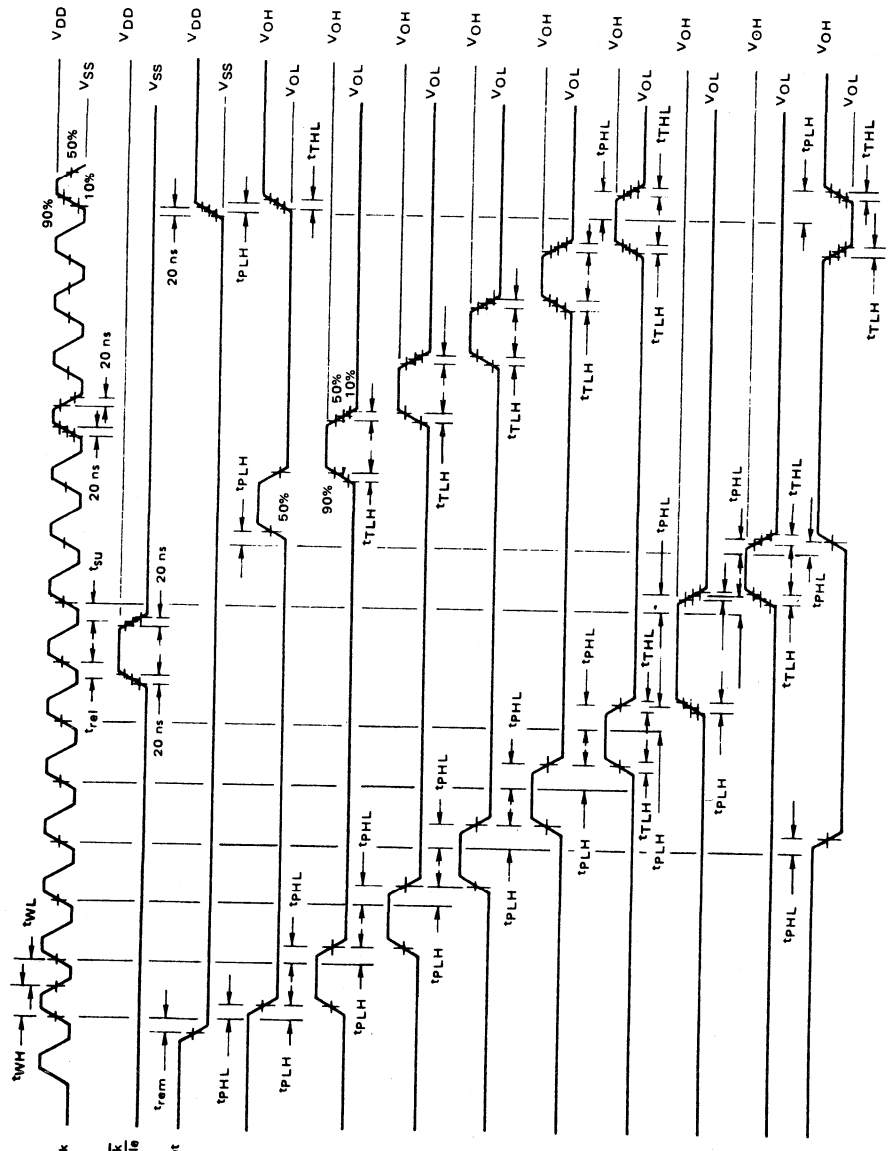


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS

MOTOROLA

MC14023B
MC14023UB

TRIPLE 3-INPUT "NAND" GATE

The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

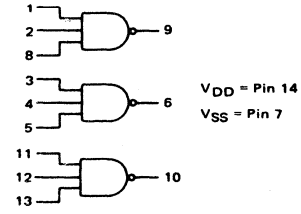
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

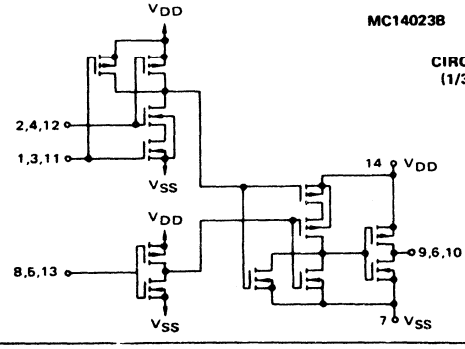
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

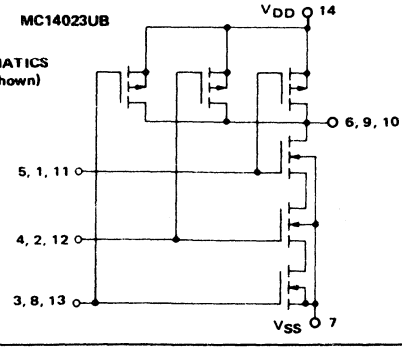


CIRCUIT SCHEMATICS
(1/3 of Device Shown)

MC14023B



MC14023UB



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14024B

CMOS SSI

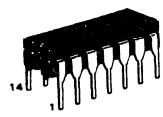
(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER

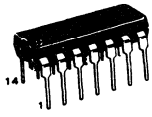
SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

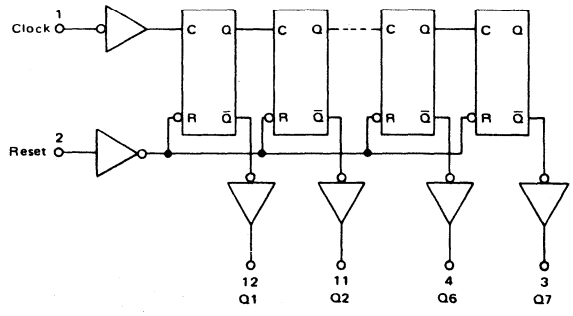
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

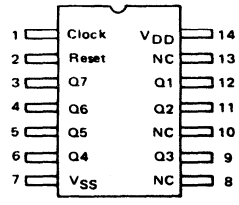
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.31 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.60 µA/kHz) f + I_{DD}							
		15	I_T = (0.89 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1,7 ns/pF) C_L + 915 ns		5.0	–	1000	2000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	–	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	–	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	–	ns
		10	165	60	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	600	375	–	ns
		10	350	200	–	
		15	260	150	–	
Reset Removal Time	t_{rem}	5.0	625	250	–	ns
		10	190	75	–	
		15	145	50	–	
Clock Input Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	1.0	s
		10	–	–	8.0	ms
		15	–	–	200	µs
Input Pulse Frequency	f_{cl}	5.0	–	2.5	1.0	MHz
		10	–	8.0	3.0	
		15	–	12	4.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

CLOCK	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
¬	0	Advance One Count
¬	1	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

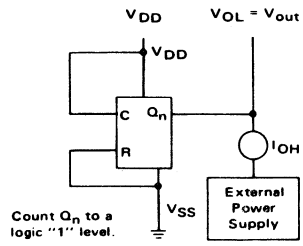


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

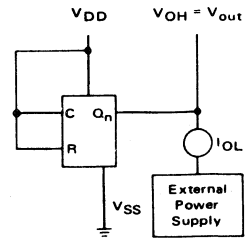
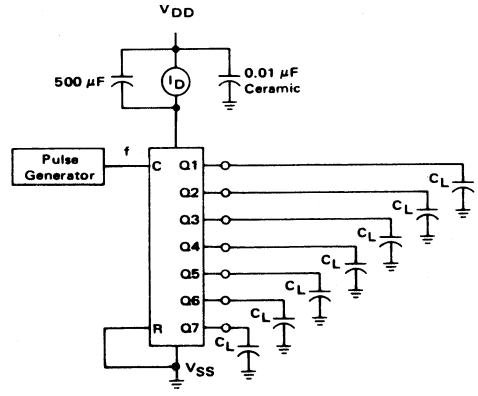


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT



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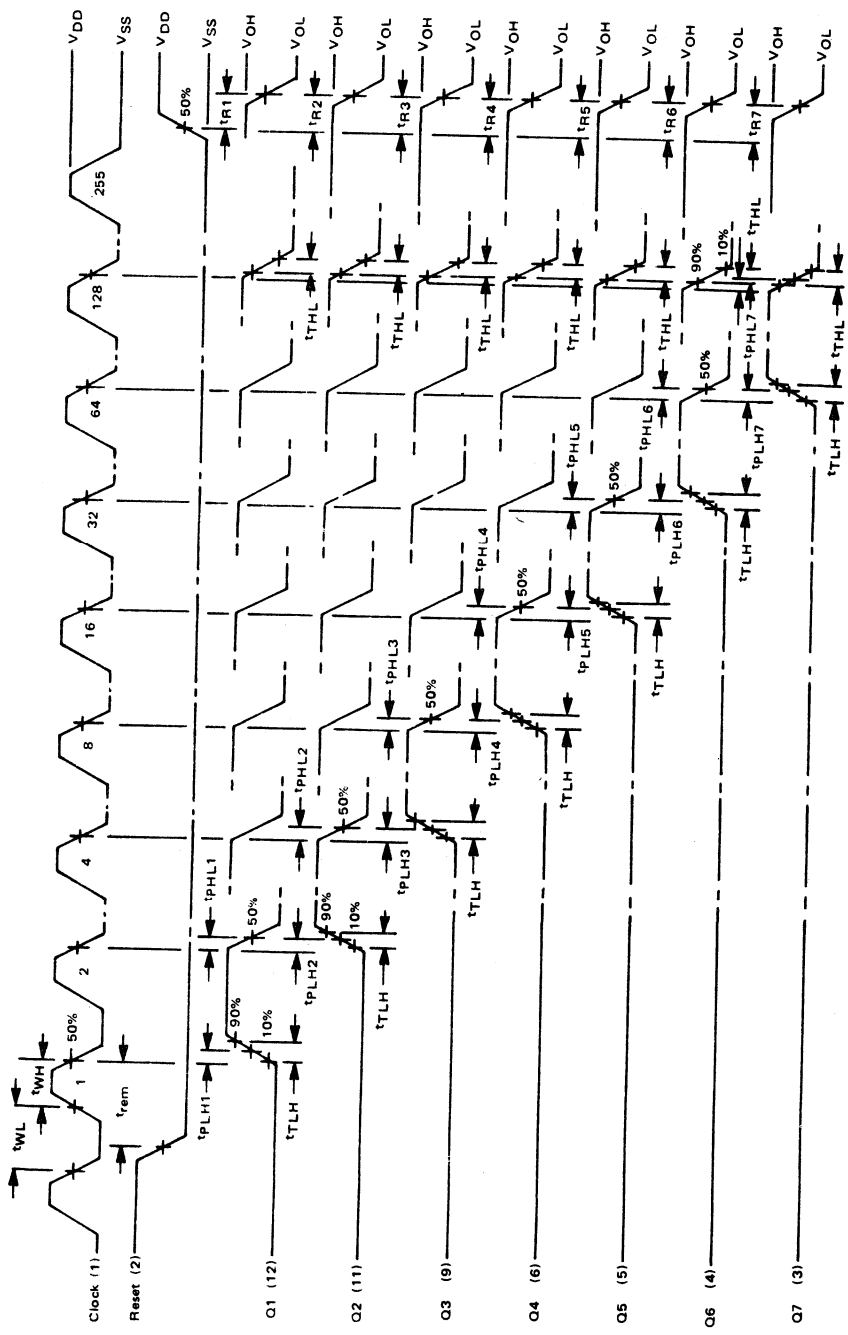


FIGURE 4 – FUNCTIONAL WAVEFORMS

6

MOTOROLA

MC14025B
MC14025UB

CMOS SSI

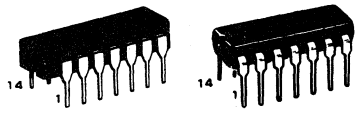
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NOR" GATE

TRIPLE 3-INPUT "NOR" GATE

The MC14025B and MC14025UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025B and CD4025UB.



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

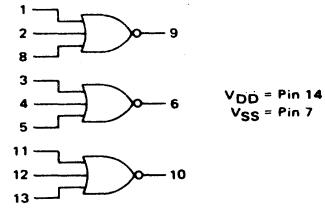
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

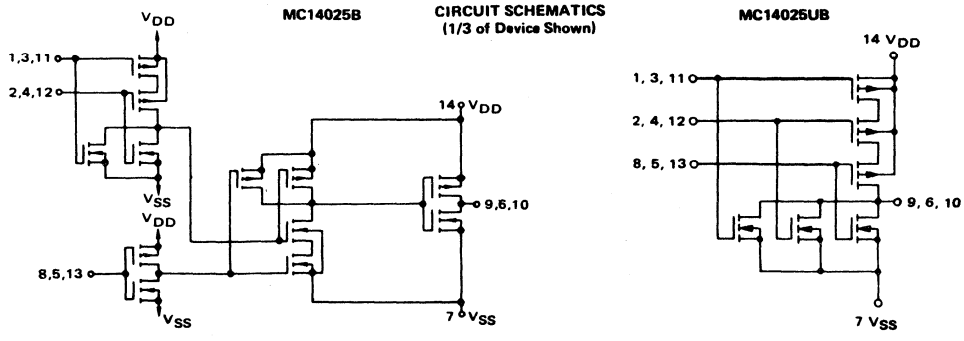
See the MC14001B data sheet for complete characteristics of the B-Series device.

See the MC14001UB data sheet for complete characteristics for the non-B device.

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14027B

CMOS SSI

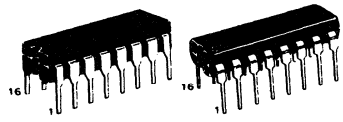
(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP

DUAL J-K FLIP-FLOP

The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to –150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: – 12mW/°C from 65°C to 85°C
Ceramic "L" Package: – 12mW/°C from 100°C to 125°C

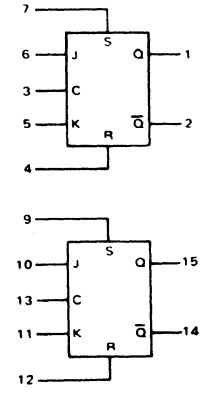
TRUTH TABLE

INPUTS						OUTPUTS*		
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$	
⌐⌐	1	X	0	0	0	1	0	
⌐⌐	X	0	0	0	1	1	0	
⌐⌐	0	X	0	0	0	0	1	
⌐⌐	X	1	0	0	1	0	1	
⌐⌐	1	1	0	0	Q_0	$\overline{Q_0}$	Q_0	
⌐⌐	X	X	0	0	X	Q_n	$\overline{Q_n}$	No Change
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.80 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.60 µA/kHz) f + I_{DD}							
		15	I_T = (2.40 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

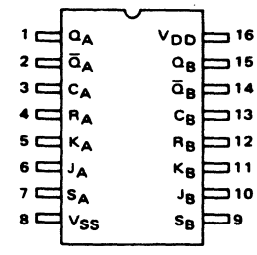
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

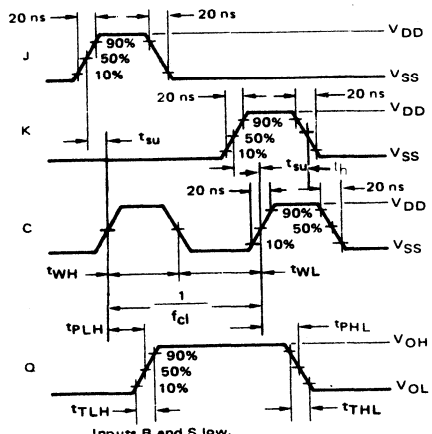
Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Times**	t_{PLH},					ns
Clock to Q, Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q, Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q, Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times	t_{su}	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Hold Times	t_h	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Clock Pulse Width	t_{WH}, t_{WL}	5.0	330	165	–	ns
		10	110	55	–	
		15	75	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	9.0	4.5	
		15	–	13	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Removal Times	t_{rem}					ns
		5	90	10	—	
		10	45	5	—	
		15	35	3	—	
Set						
		5	50	−30	—	
		10	25	−15	—	
Reset		15	20	−10	—	
Set and Reset Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

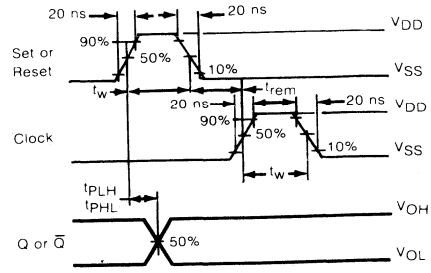
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FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)

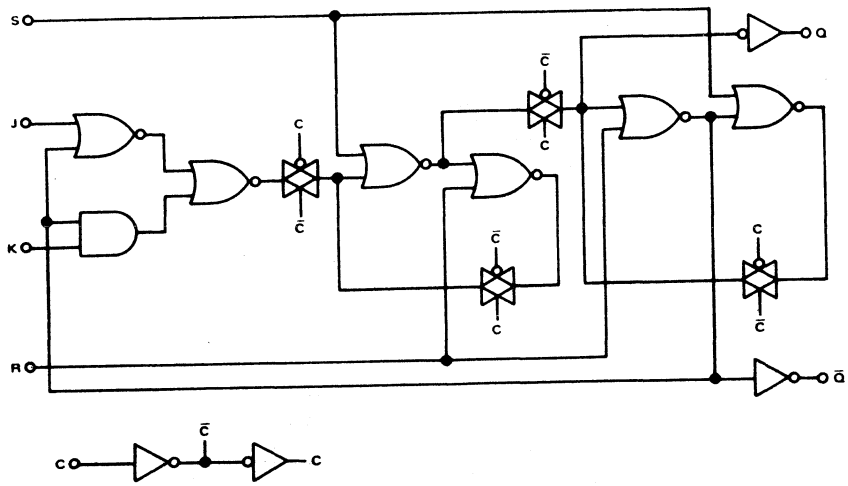


Inputs R and S low.
For the measurement of t_{WH}, $1/f_{cl}$, and P_D the inputs J and K are kept high.

FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, Clock, and Output)



LOGIC DIAGRAM
(1/2 of Device Shown)



MOTOROLA

MC14028B

CMOS MSI

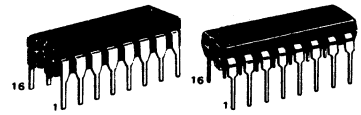
(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

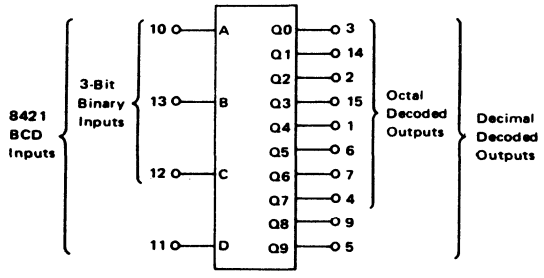
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4		
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C

†To calculate total supply current at loads other than 50 pF:

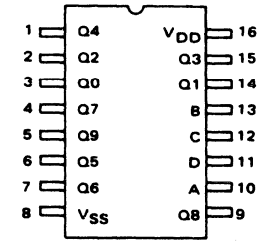
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

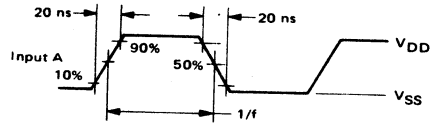
Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

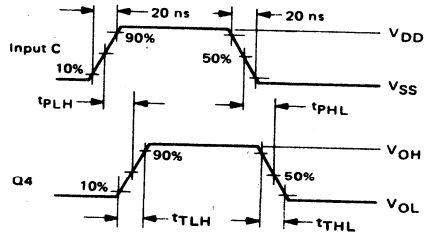
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

Inputs B, C, and D switching in respect to a BCD code.



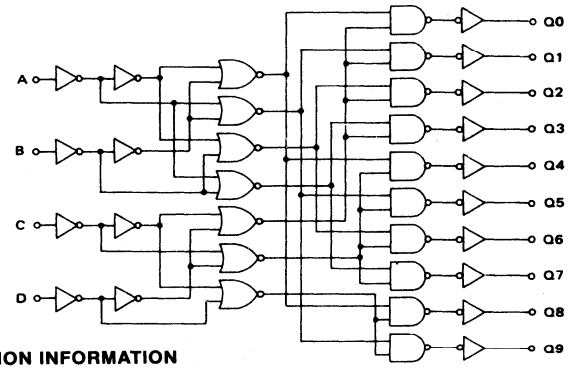
All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.



6

LOGIC DIAGRAM

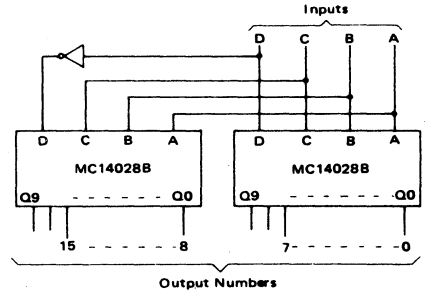


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS														CODE AND REDEFINED OUTPUT NUMBERS					
																		Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

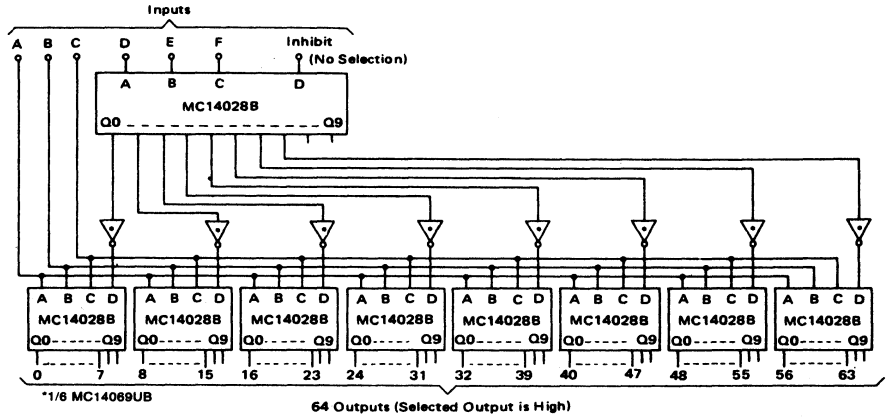
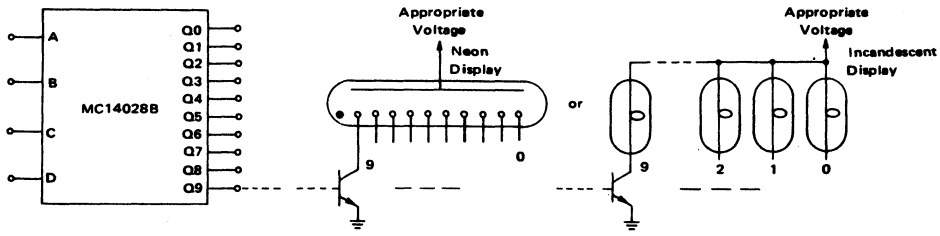


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



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MOTOROLA

MC14029B

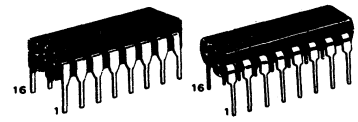
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

BINARY/DECADE UP/DOWN COUNTER

BINARY/DECADE UP/DOWN COUNTER

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

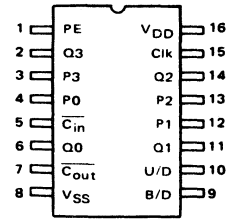
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clk to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	90	180	
Clk to C_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	85	190	
C_{in} to C_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns	t_{PHL}	5.0	–	175	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	50	120	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	50	100	
PE to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	–	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
PE to C_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	–	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0	180	90	—	ns
		10	80	40	—	
		15	60	30	—	
Clock Pulse Frequency	f_{cl}	5.0	—	4.0	2.0	MHz
		10	—	8.0	4.0	
		15	—	10	5.0	
Preset Removal Time	t_{rem}	5.0	160	80	—	ns
The Preset Signal must be low prior to a positive-going transition of the clock.		10	80	40	—	
		15	60	30	—	
Clock Rise and Fall Time	$t_{r(cl)}$	5.0	–	–	15	μs
	$t_{f(cl)}$	10	–	–	5	
		15	–	–	4	
$\overline{Carry}$ In Setup Time	t_{su}	5.0	150	75	–	ns
		10	60	30	–	
		15	40	20	–	
Up/Down Setup Time		5.0	340	170	–	ns
		10	140	70	–	
		15	100	50	–	
Binary/Decade Setup Time		5.0	320	160	–	ns
		10	140	70	–	
		15	100	50	–	
Preset Enable Pulse Width	t_W	5.0	130	65	–	ns
		10	70	35	–	
		15	50	25	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

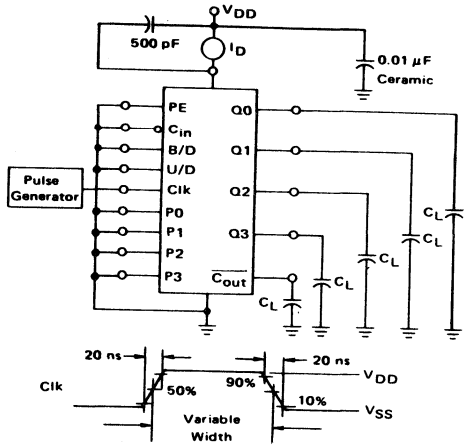
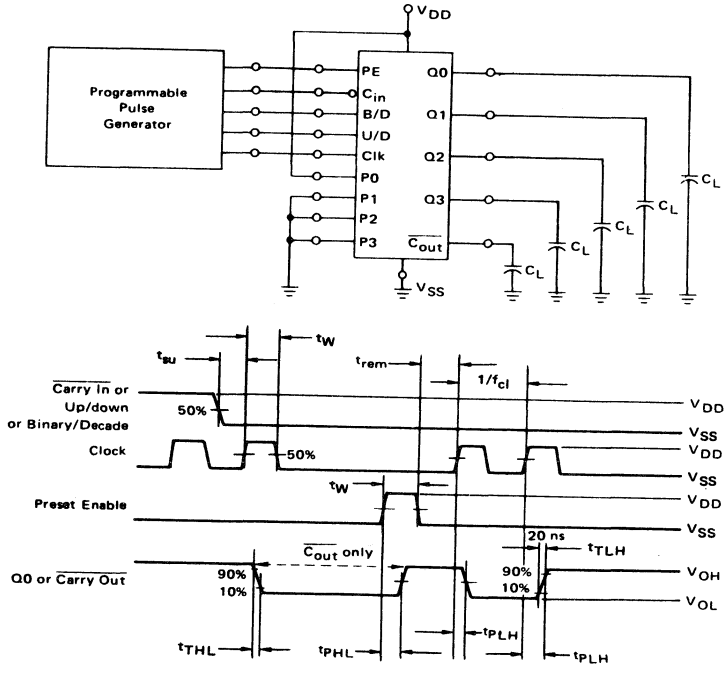


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM

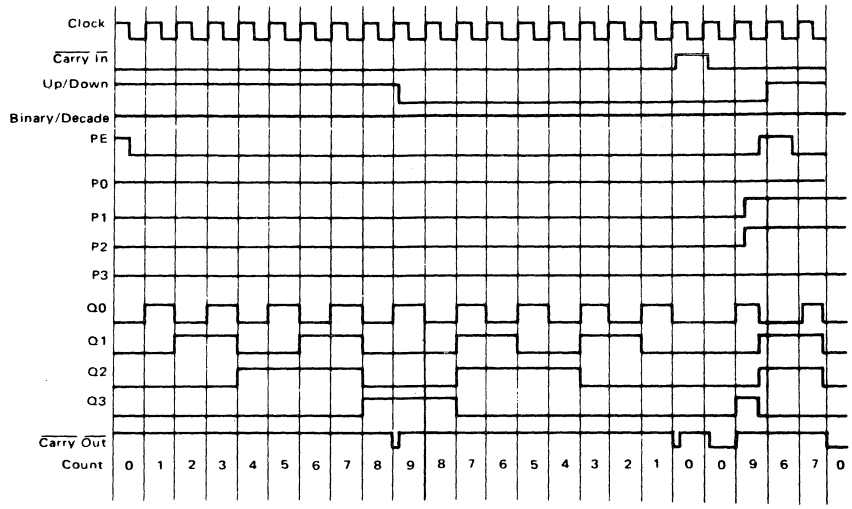
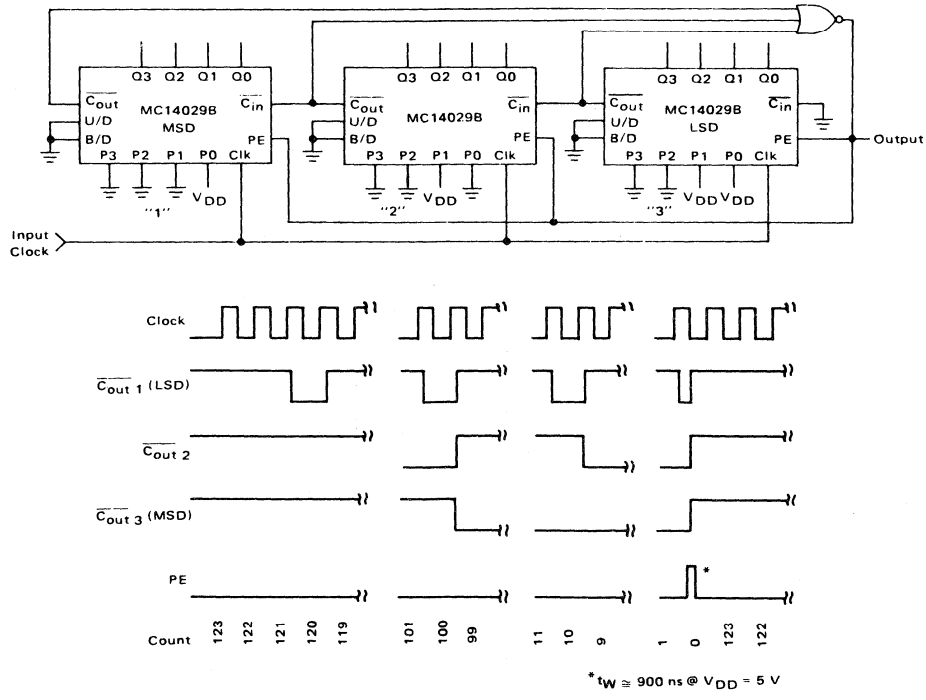
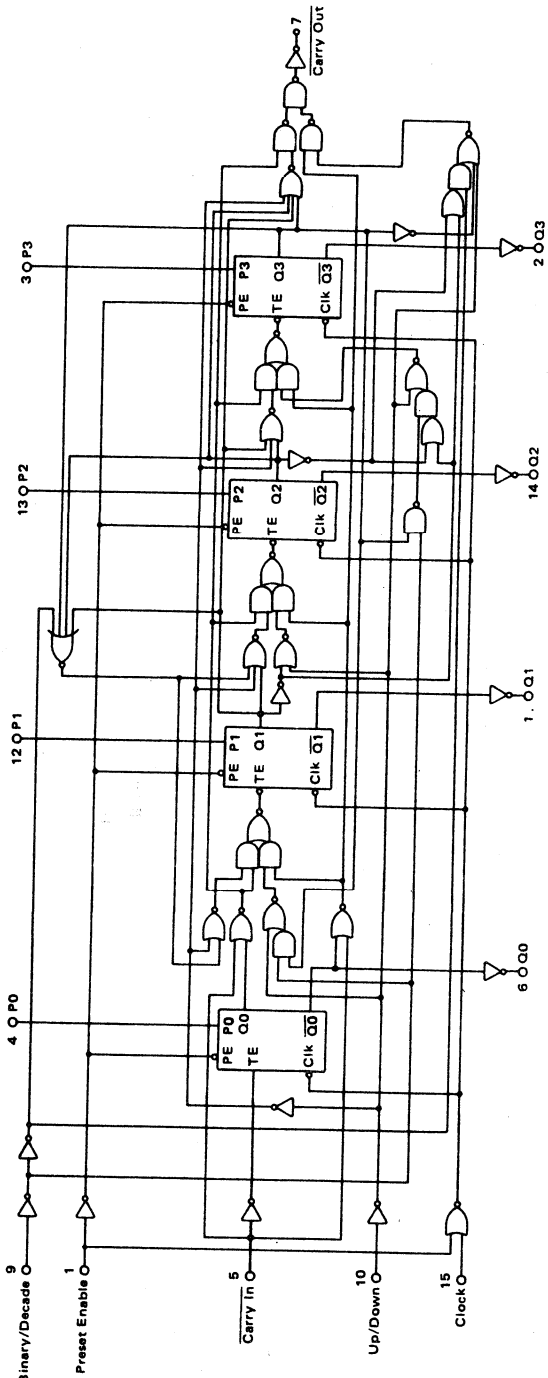


FIGURE 3 – DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM
(Shown for N = 123)



LOGIC DIAGRAM



MOTOROLA

MC14032B
MC14038B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

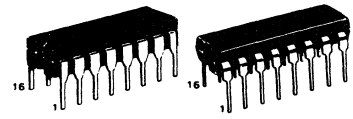
TRIPLE SERIAL ADDERS

Positive Logic – MC14032B
Negative Logic – MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Buffered Outputs
- Single-Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

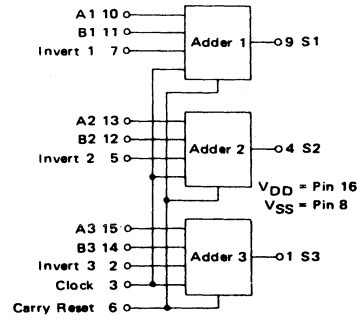
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

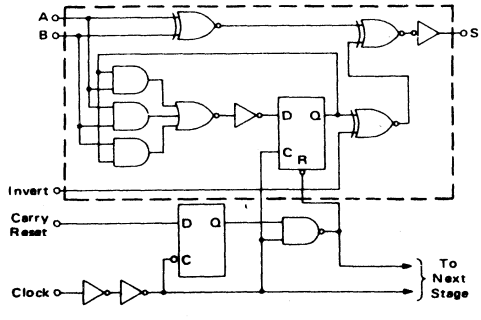
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM

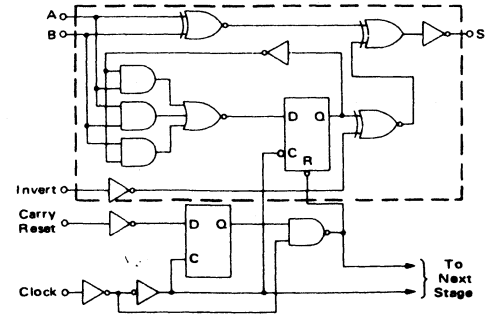


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.96 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.93 µA/kHz) f + I_{DD}							
		15	I_T = (2.8 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

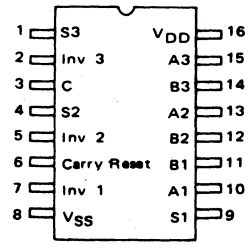
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

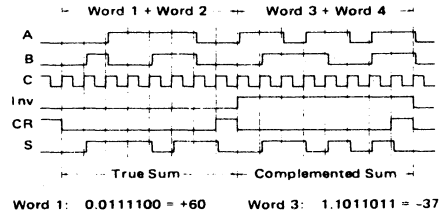
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A, B or Invert to Sum	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	1400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	230	
Clock to Sum						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	2400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 110 ns		15	–	135	450	
Input Setup Time	t_{su}	5.0	10	-10	–	ns
		10	10	0	–	
		15	10	0	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	1.0	MHz
		10	–	10	2.5	
		15	–	12	4.0	
Clock Rise and Fall Times	t_{THL}, t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

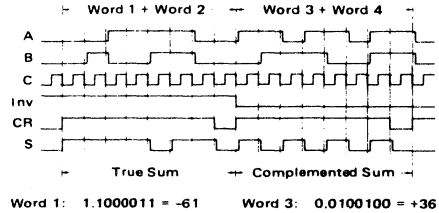
TIMING DIAGRAMS

MC14032B



Word 1: 0.0111100 = +60 Word 3: 1.1011011 = -37
Word 2: 0.0110010 = +50 Word 4: 1.1001110 = -50
0.1101110 = +110 1.0101001 = -87

MC14038B



Word 1: 1.1000011 = -61 Word 3: 0.0100100 = +36
Word 2: 1.1001101 = -51 Word 4: 0.0110001 = +49
1.0010000 = -112 0.1010101 = +85

Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

6

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

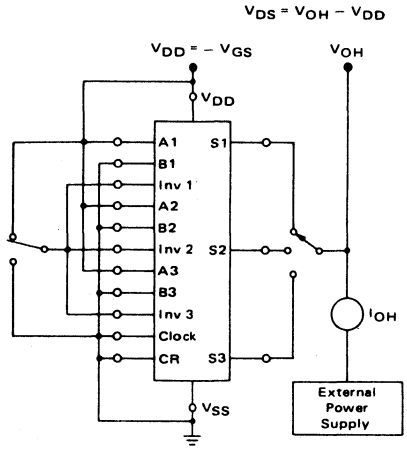


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

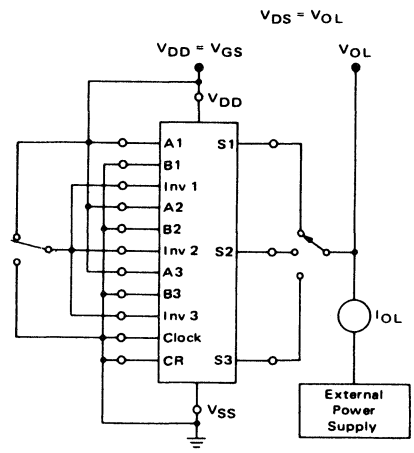
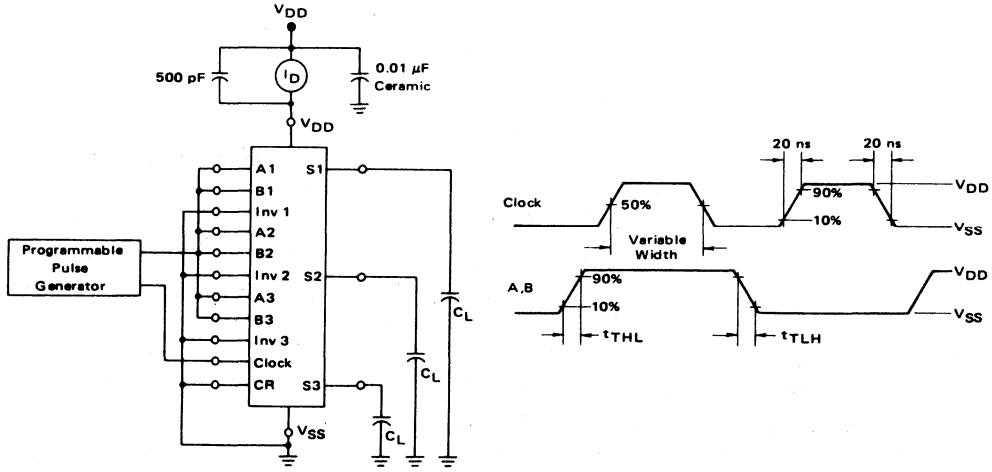
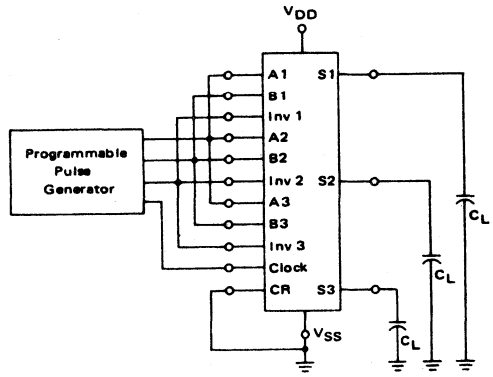


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

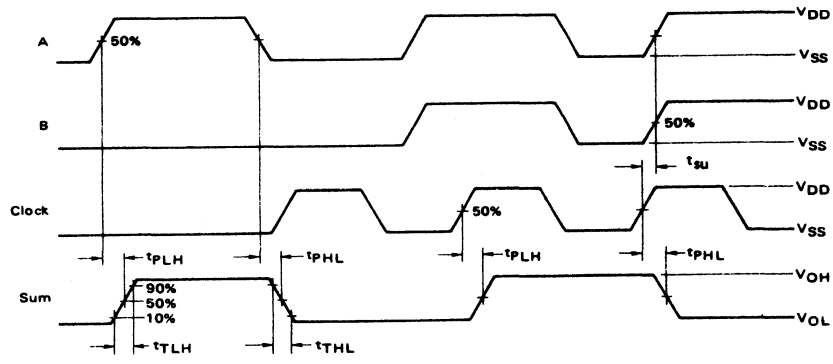


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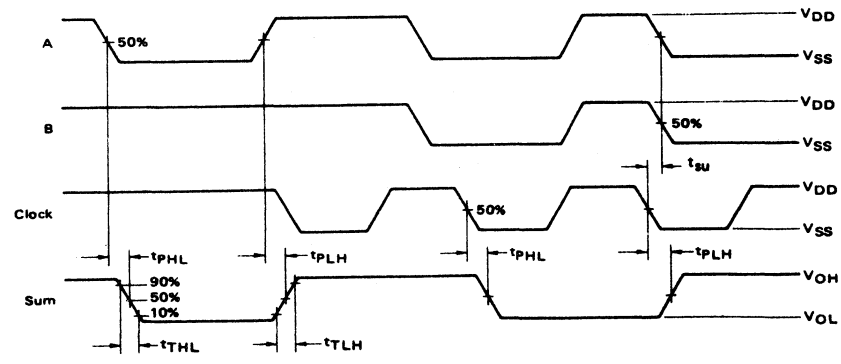
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14032B



MC14038B



6

MOTOROLA

MC14034B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

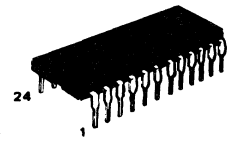
8-BIT UNIVERSAL BUS REGISTER

8-BIT UNIVERSAL BUS REGISTER

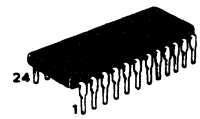
The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

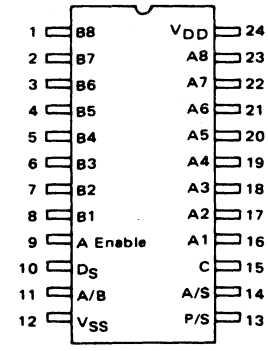
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (4.4 μA/kHz) f + I_{DD}							
		15	I_T = (6.6 μA/kHz) f + I_{DD}							
3-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc
			–		–			–		
3-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	μAdc
			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time A or B	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time A or B	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time						
A (B) Synchronous Parallel Data Input,	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 440 ns		5.0	–	525	1050	
t_{PHL}, t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	410	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 120 ns		15	–	145	290	
Propagation Delay Time						
A (B) Asynchronous Parallel Data Input	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1010	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Clock Pulse Width	t_{WH}	5.0	340	170	–	ns
		10	140	70	–	
		15	110	55	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.2	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock Pulse Rise	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
A, B Input Setup Time	t_{su}	5.0	100	35	–	ns
		10	45	15	–	
		15	35	12	–	
High Level SE, P/S, A/S Pulse Width	t_{WH}	5.0	600	200	–	ns
		10	270	90	–	
		15	200	80	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

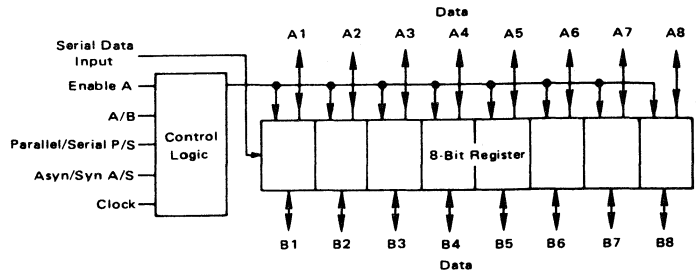
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM

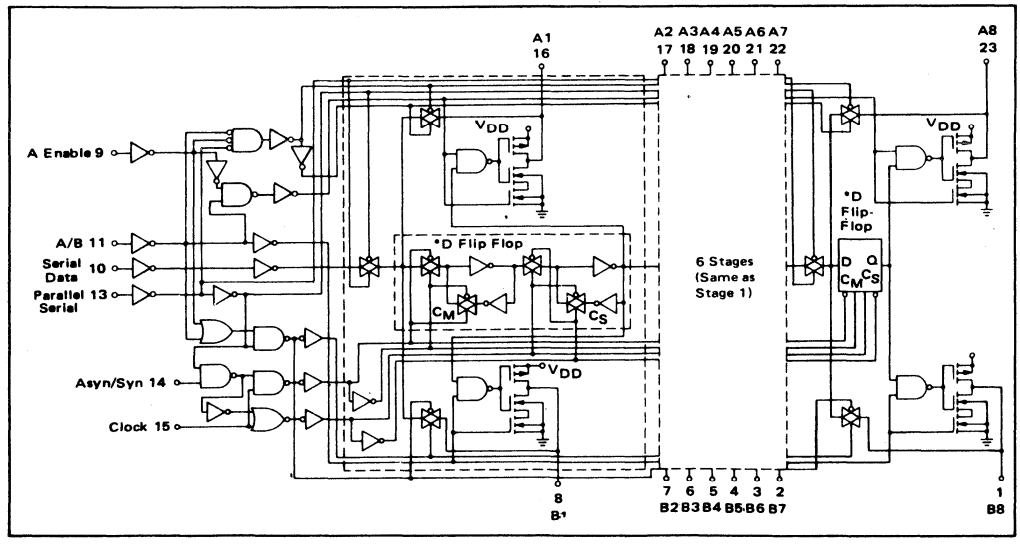
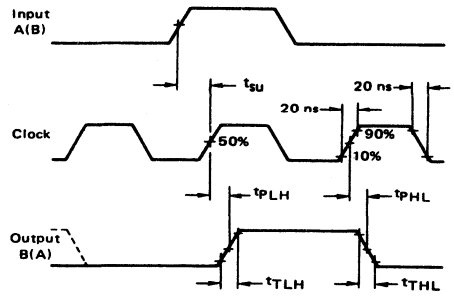


FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

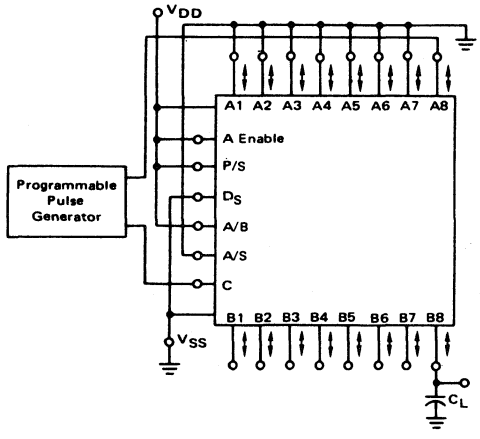
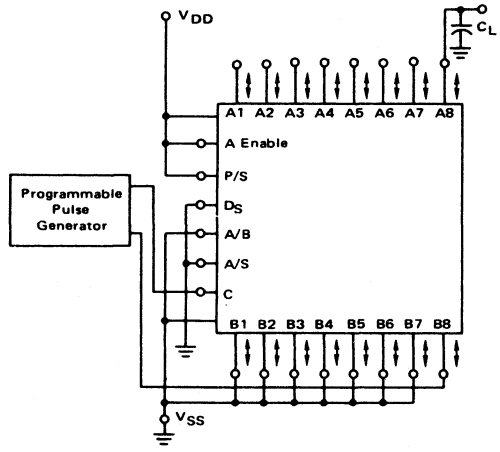


FIGURE 3 — B SYNCHRONOUS DATA INPUT, A PARALLEL DATA OUTPUT AND SETUP TIME



6

FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

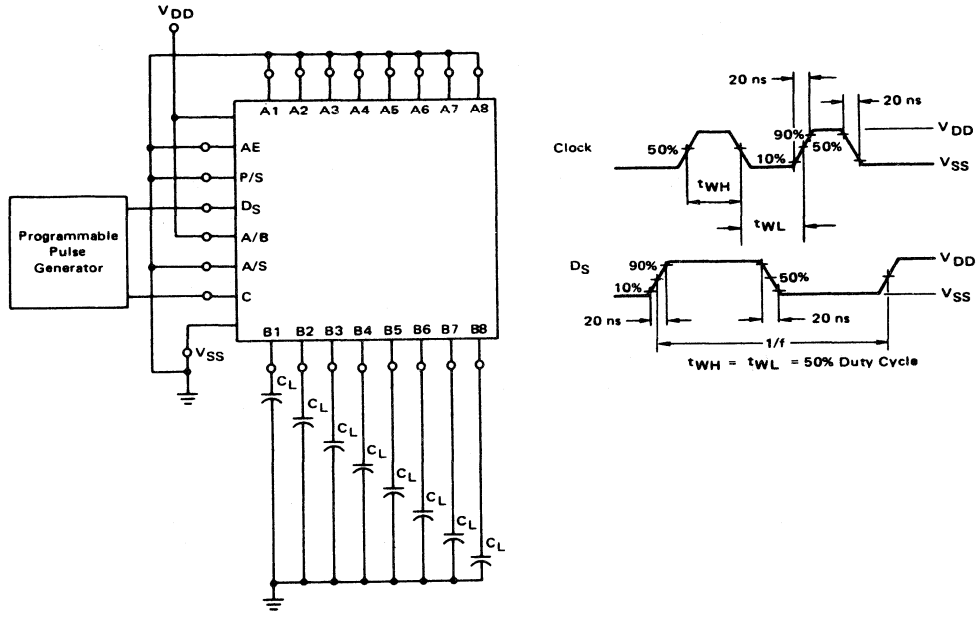


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

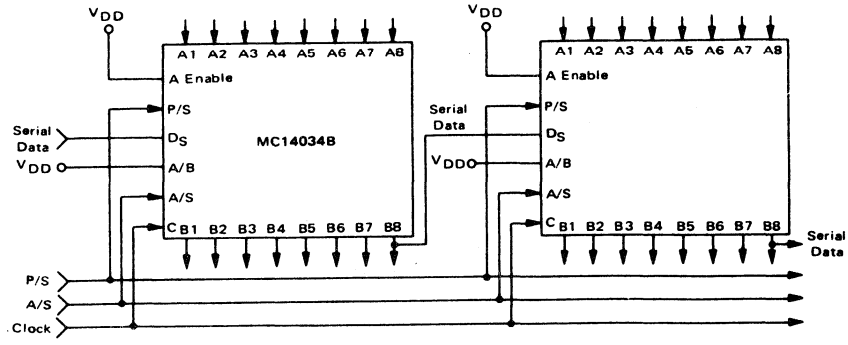
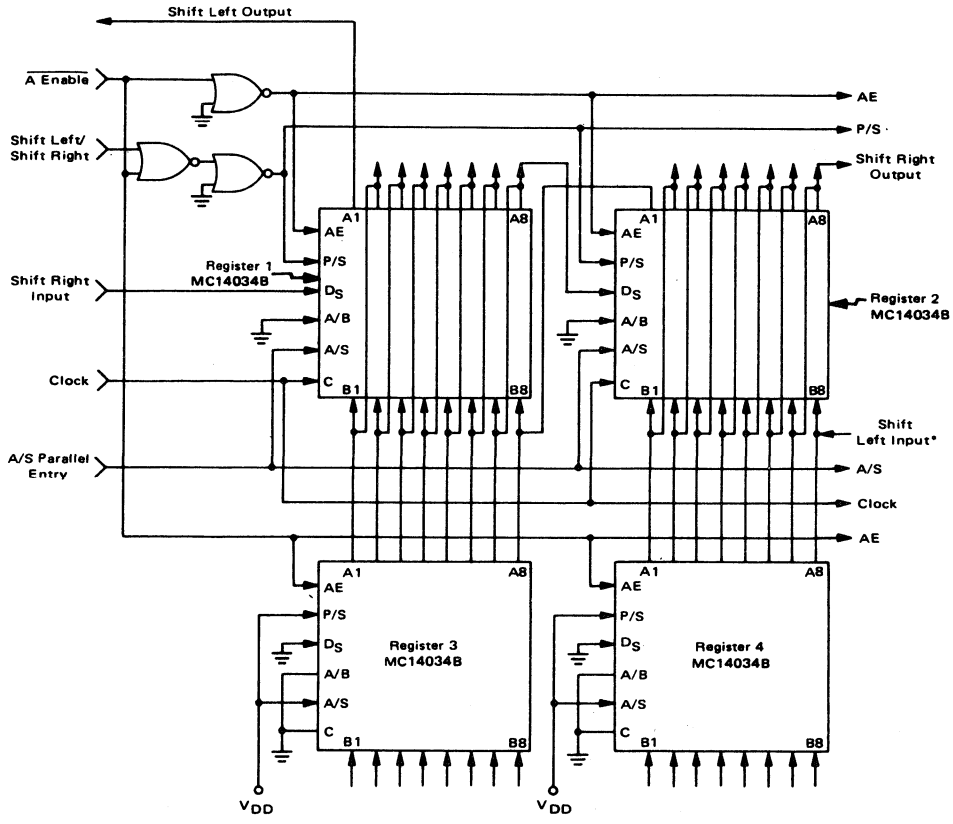


FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

MOTOROLA

MC14035B

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

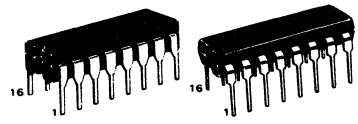
INPUTS C	J	$\overline{K}$	R	t_n OUTPUT Q0
⎍	0	0	0	0
⎍	0	1	0	Q0 (n − 1)
⎍	1	0	0	$\overline{Q0}$ (n − 1)
⎍	1	1	0	1
⎎	x	x	0	Q0 (n − 1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

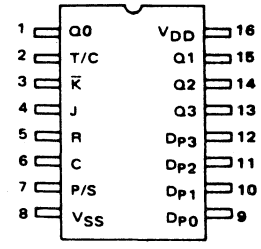
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	µAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	µAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

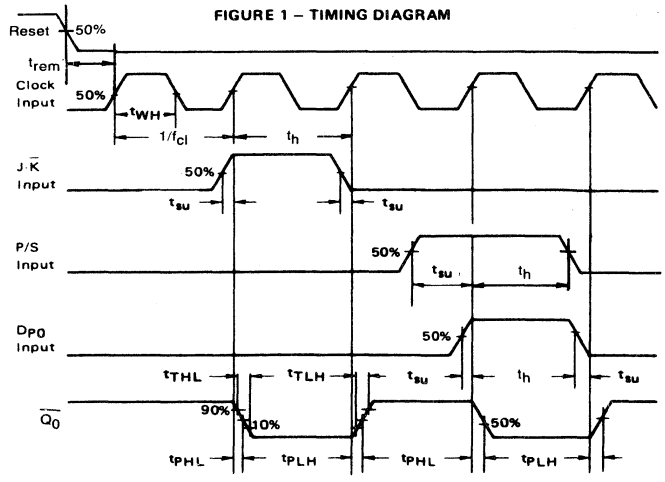
SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, See Figure 1)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
T_{TLH}, $T_{THL} = (1.5$ ns/pF) $C_L + 25$ ns	t_{THL}	5.0	—	100	200	
T_{TLH}, $T_{THL} = (0.75$ ns/pF) $C_L + 12.5$ ns		10	—	50	100	
T_{TLH}, $T_{THL} = (0.55$ ns/pF) $C_L + 12.5$ ns		15	—	40	80	
Propagation Delay Time, Clock or Reset to Q	t_{PLH},					ns
T_{PLH}, $T_{PHL} = (1.75$ ns/pF) $C_L + 223$ ns	t_{PHL}	5.0	—	300	600	
T_{PLH}, $T_{PHL} = (0.70$ ns/pF) $C_L + 89$ ns		10	—	130	260	
T_{PLH}, $T_{PHL} = (0.53$ ns/pF) $C_L + 67$ ns		15	—	95	190	
Clock Pulse Width	t_{WH}	5.0	335	135	—	ns
		10	165	45	—	
		15	125	40	—	
Reset Pulse Width	t_{WH}	5.0	400	80	—	ns
		10	175	40	—	
		15	130	35	—	
Reset Removal Time	t_{rem}	5.0	80	40	—	ns
		10	30	15	—	
		15	25	10	—	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			—
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	—	2.5	1.2	MHz
		10	—	6.0	2.0	
		15	—	10	3.0	
J-$\overline{K}$ to Clock Setup Time	t_{su}	5.0	500	120	—	ns
		10	200	50	—	
		15	150	30	—	
Clock to J-$\overline{K}$ Hold Time	t_h	5.0	40	−40	—	ns
		10	30	−5	—	
		15	25	0	—	
P/S to Clock Setup Time	t_{su}	5.0	500	25	—	ns
		10	200	10	—	
		15	150	7.5	—	
Clock to P/S Hold Time	t_h	5.0	30	−70	—	ns
		10	20	−20	—	
		15	20	−10	—	
D_P to Clock Setup Time	t_{su}	5.0	500	90	—	ns
		10	200	20	—	
		15	150	15	—	
Clock to D_P Hold Time	t_h	5.0	90	−25	—	ns
		10	40	0	—	
		15	40	5	—	

*The formulas given are for the typical characteristics only at 25°C.

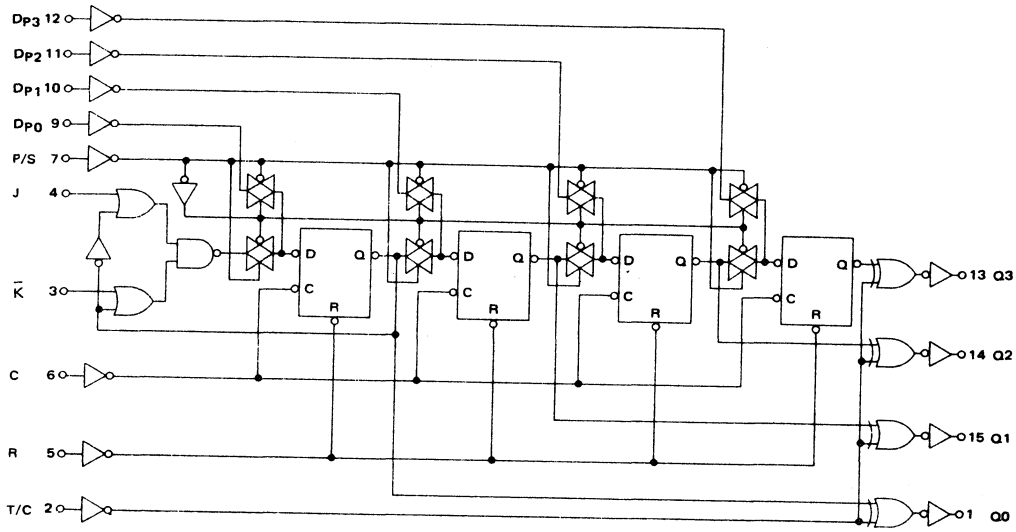
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TIMING DIAGRAM

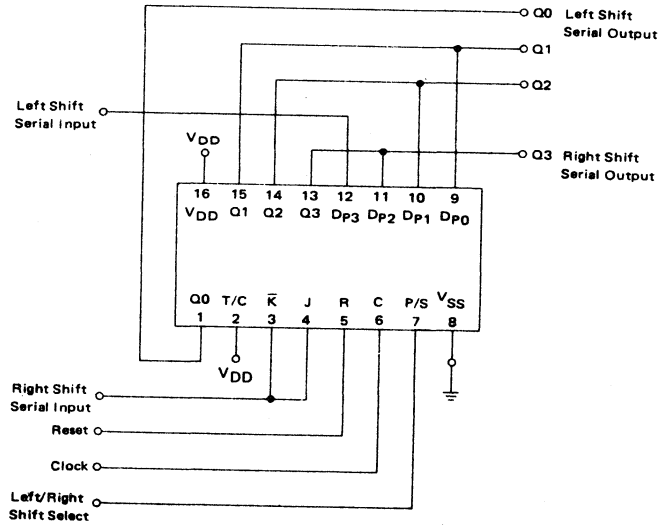


T/C Input Low

LOGIC DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



MOTOROLA

MC14038B

FOR COMPLETE DATA
SEE MC14032B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

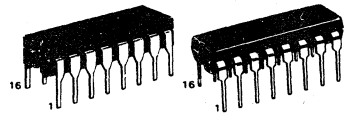
TRIPLE SERIAL ADDERS

Positive Logic – MC14032B
Negative Logic – MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Buffered Outputs
- Single-Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

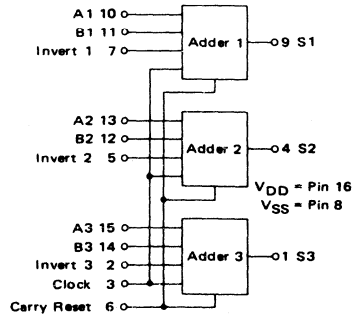
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

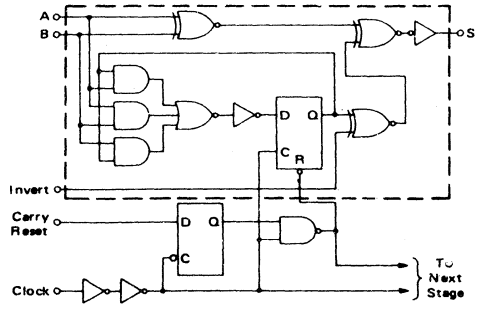
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM

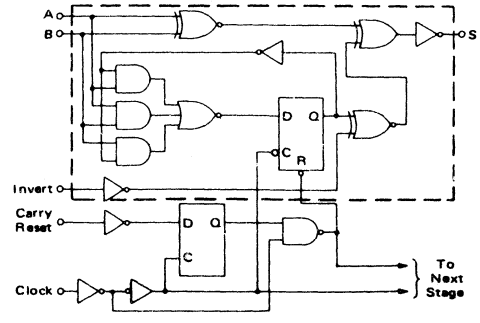


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



6

MOTOROLA

MC14040B

12-BIT BINARY COUNTER

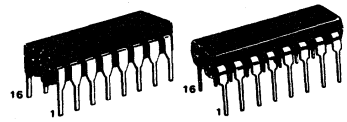
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line
- Pin-for-Pin Replacement for CD4040B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

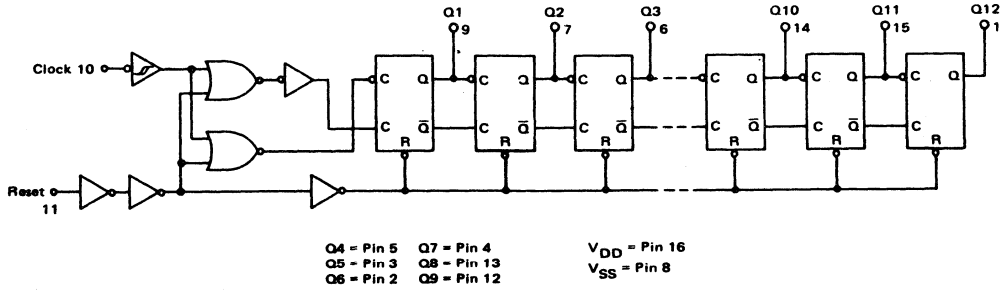
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.85 μA/kHz) f + I_{DD}							
		15	I_T = (1.43 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

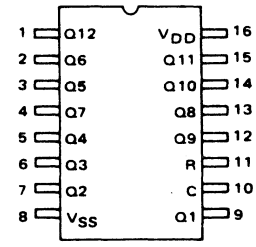
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{dc}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					
Clock to Q1	t_{PHL}					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	—	260	520	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	—	115	230	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	—	80	160	
Clock to Q12						ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns		5.0	—	1625	3250	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns		10	—	720	1440	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 ns		15	—	500	1000	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 485 ns		5.0	—	370	740	
t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	—	155	310	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	—	115	230	
Clock Pulse Width	t_{WH}	5.0	385	140	—	ns
		10	150	55	—	
		15	115	38	—	
Clock Pulse Frequency	f_{cl}	5.0	—	2.1	1.5	MHz
		10	—	7.0	3.5	
		15	—	10.0	4.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Reset Pulse Width	t_{WH}	5.0	960	320	—	ns
		10	360	120	—	
		15	270	80	—	
Reset Removal Time	t_{rem}	5.0	130	65	—	ns
		10	50	25	—	
		15	30	15	—	

"The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

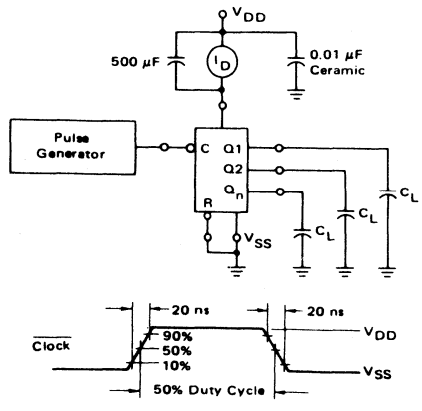


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

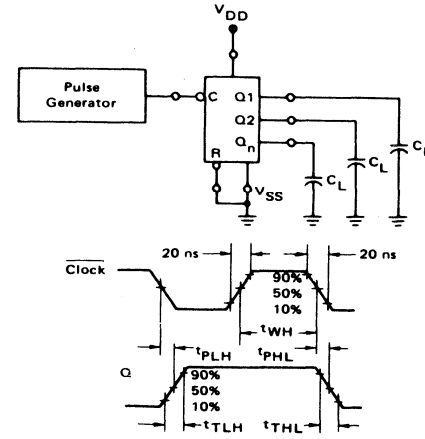
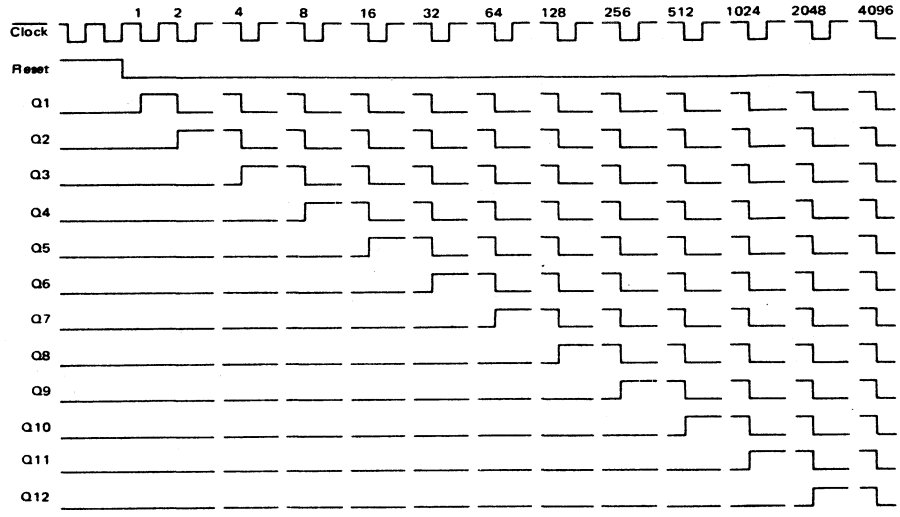


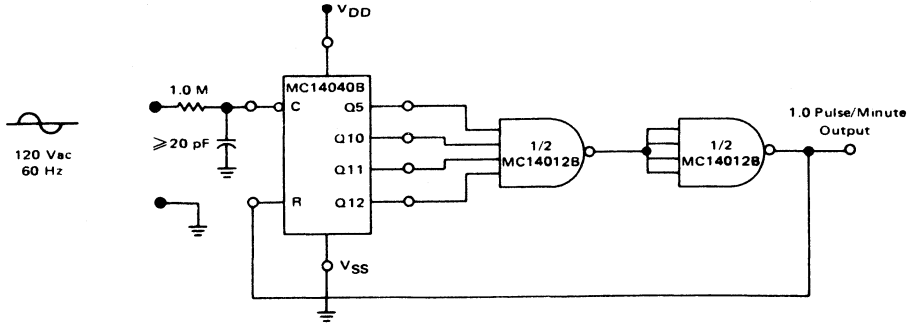
FIGURE 3 – TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MOTOROLA

MC14042B

QUAD TRANSPARENT LATCH

The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

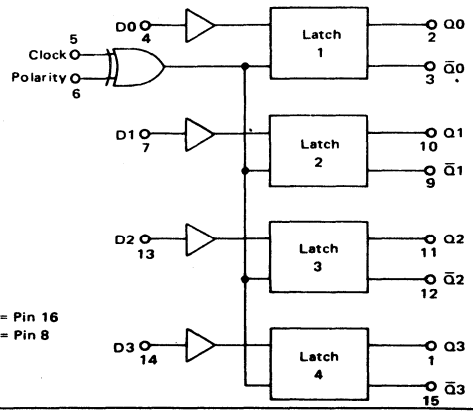
- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

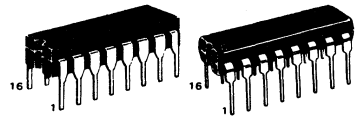
LOGIC DIAGRAM



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD
TRANSPARENT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

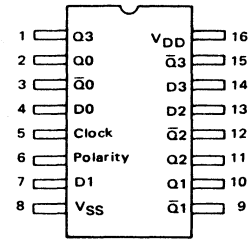
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.0 μA/kHz) f + I_{DD}							
		15	I_T = (3.0 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

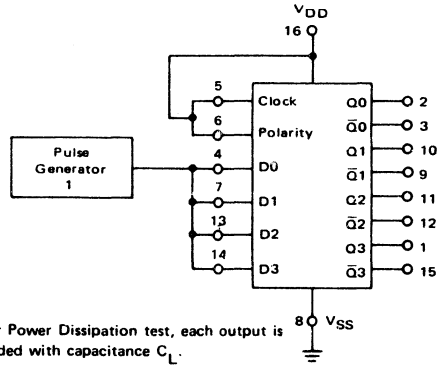
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, D to Q, $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Propagation Delay Time, Clock to Q, $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		25	–	60	120	
Clock Pulse Width	t_{WH}					ns
		5.0	300	150	–	
		10	100	50	–	
		15	80	40	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}					µs
		5.0	—	—	15	
		10	—	—	5.0	
		15	—	—	4.0	
Hold Time	t_h					ns
		5.0	100	50	–	
		10	50	25	–	
		15	40	20	–	
Setup Time	t_{su}					ns
		5.0	50	0	–	
		10	30	0	–	
		15	25	0	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM
(Data to Output)



For Power Dissipation test, each output is loaded with capacitance C_L.

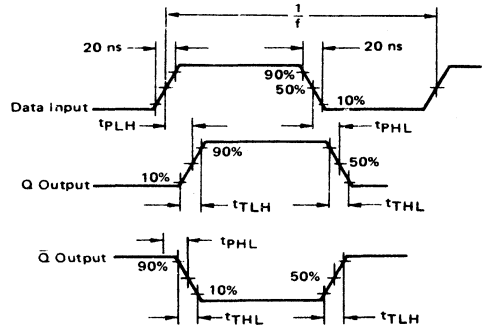
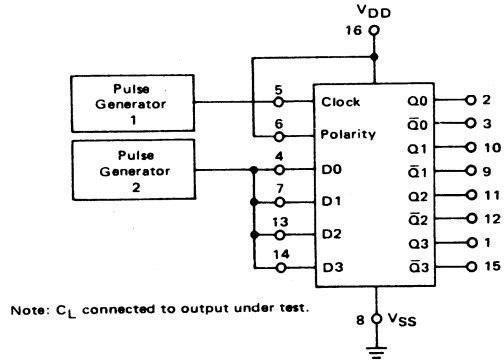
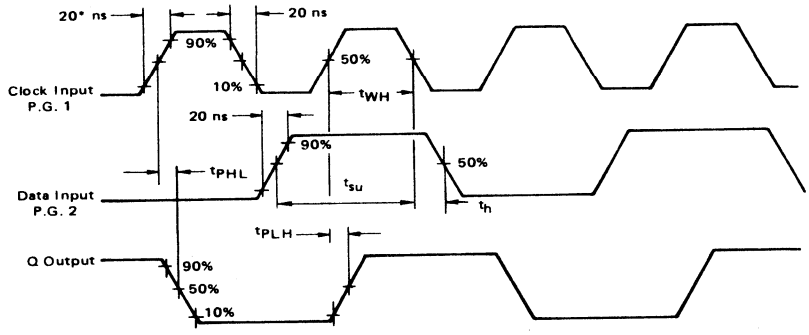


FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)



Note: C_L connected to output under test.



*Input clock rise time is 20 ns except for maximum rise time test.

6

MOTOROLA

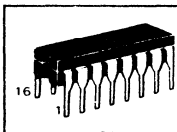
MC14043B
QUAD "NOR" R-S LATCH

MC14044B
QUAD "NAND" R-S LATCH

CMOS MSI
QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620



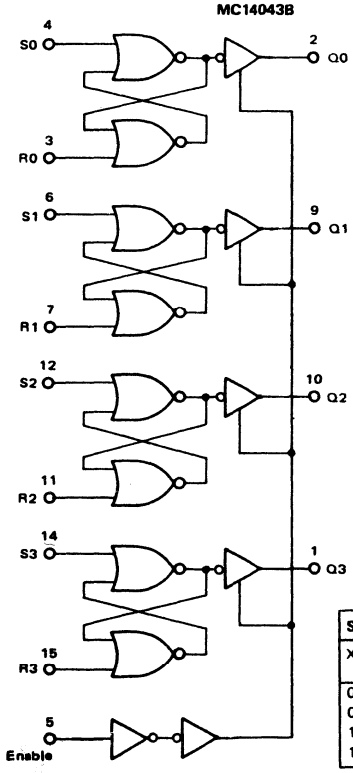
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MC14043B



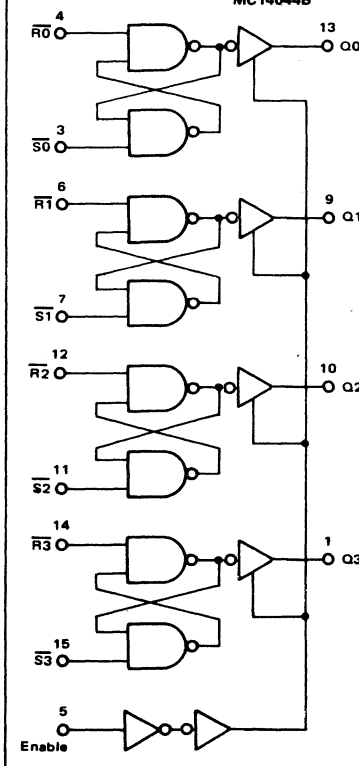
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

MC14044B



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all outputs switching)	I_T	5.0	$I_T = (0.58\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.15\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.73\ \mu A/kHz)\ f + I_{DD}$							
Three-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
Three-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	–	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
t_{PHL} = (0.90 ns/pF) C_L + 130 ns	t_{PHL}	5.0	–	175	350	ns
t_{PHL} = (0.90 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
Set, $\overline{\text{Set}}$ Pulse Width	t_W	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Reset, $\overline{\text{Reset}}$ Pulse Width	t_W	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Three-State Enable/Disable Delay	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5.0	–	150	300	ns
		10	–	80	160	
		15	–	55	110	

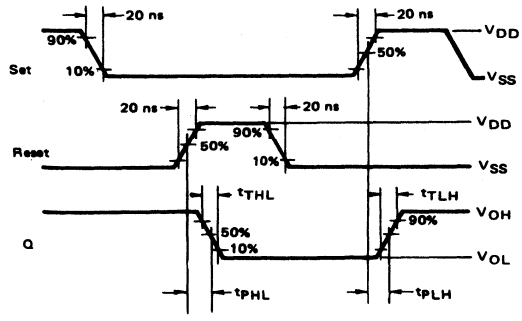
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

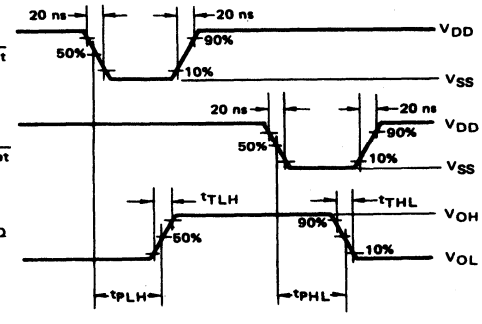
6

AC WAVEFORMS

MC14043B



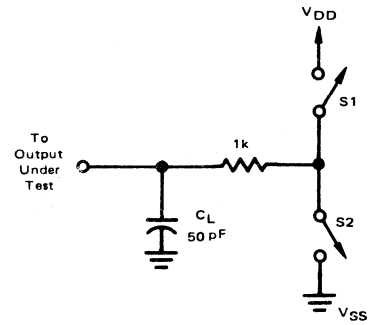
MC14044B

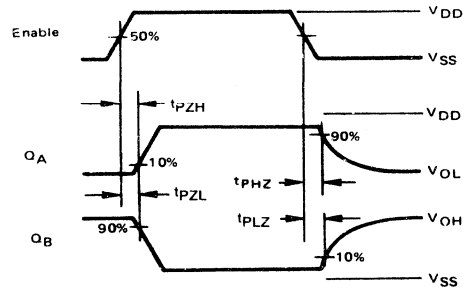


THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3-State Tests.

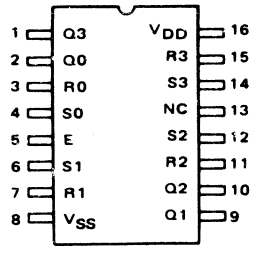
TEST	ENABLE	S1	S2	Q	MC14043B S	MC14043B R	MC14044B $\overline{S}$	MC14044B $\overline{R}$
t_{PZH}	⌐	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PZL}	⌐	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}
t_{PHZ}	¬	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PLZ}	¬	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}



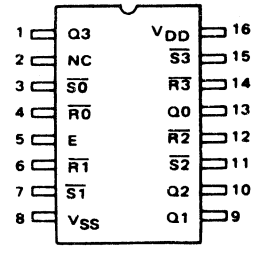


PIN ASSIGNMENT

MC14043B



MC14044B



NC = No Connection

6

MOTOROLA

MC14049UB
MC14050B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

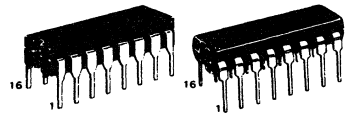
HEX BUFFERS

Inverting – MC14049UB
Noninverting – MC14050B

HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B non-inverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{DD}. The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications—MC14049UB
  Meets JEDEC B Specification—MC14050B
- V_{IN} can exceed V_{DD}



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

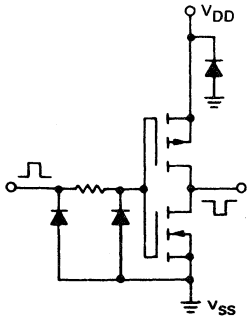
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}	Input Voltage (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	+45	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

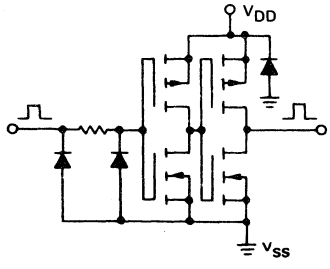
*Maximum Ratings are those values beyond which damage to the device may occur.

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14049UB

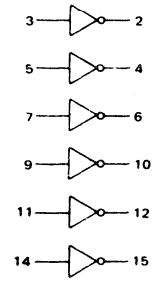


MC14050B



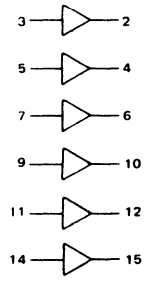
LOGIC DIAGRAMS

MC14049UB



NC = Pin 13, 16
V_{SS} = Pin 8
V_{DD} = Pin 1

MC14050B



NC = Pin 13, 16
V_{SS} = Pin 8
V_{DD} = Pin 1

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage MC14049UB	"0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)			5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)			10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)			15	–	2.5	–	6.75	2.5	–	2.5	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)			5.0	4.0	–	4.0	2.75	–	4.0	–	
(V_O = 1.0 Vdc)			10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)			15	12.5	–	12.5	8.25	–	12.5	–	
Input Voltage MC14050B	"0" Level	V_{IL}									Vdc
(V_O = 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 13.5 Vdc)			15	11	–	11	8.25	–	11	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.6	–	-1.25	−2.5	–	-0.9	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	−2.6	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.7	–	-3.75	−10	–	-2.7	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.2	–	mAdc
(V_{OL} = 0.5 Vdc)			10	10	–	8.0	16	–	5.6	–	
(V_{OL} = 1.5 Vdc)			15	30	–	24	40	–	17.0	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.5	–	−1.25	−2.5	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	-1.5	–	−1.3	−2.6	–	-1.0	–	
(V_{OH} = 13.5 Vdc)			15	-4.5	–	−3.75	−10	–	-3.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.6	–	3.2	6.0	–	2.6	–	mAdc
(V_{OL} = 0.5 Vdc)			10	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)			15	28	–	24	40	–	19	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)			10	–	8.0	–	0.004	8.0	–	60	
			15	–	16	–	0.006	16	–	120	
Total Supply Current**†		I_T	5.0	I_T = (1.8 µA/kHz)f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package)			10	I_T = (3.5 µA/kHz)f + I_{DD}							
(C_L 50 pF on all outputs, all buffers switching)			15	I_T = (5.3 µA/kHz)f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

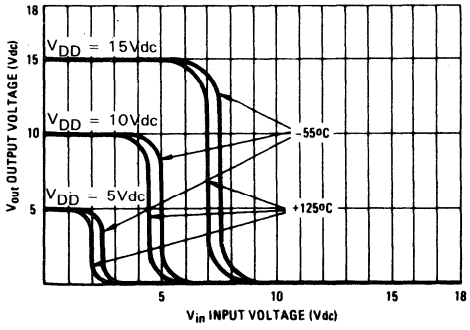
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
MC14049UB						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/pF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	
MC14050B						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.7 ns/pF) C_L + 65 ns		5.0	–	100	160	
t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns		10	–	50	80	
t_{TLH} = (0.2 ns/pF) C_L + 30 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	60	
t_{THL} = (0.06 ns/pF) C_L +17 ns		10	–	20	40	
t_{THL} = (0.04 ns/pF) C_L + 13 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	–	80	140	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	–	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	–	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	–	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	–	15	30	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049UB



MC14050B

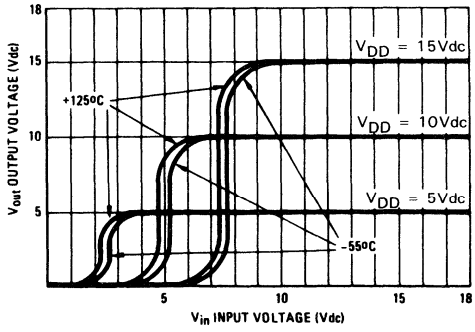


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

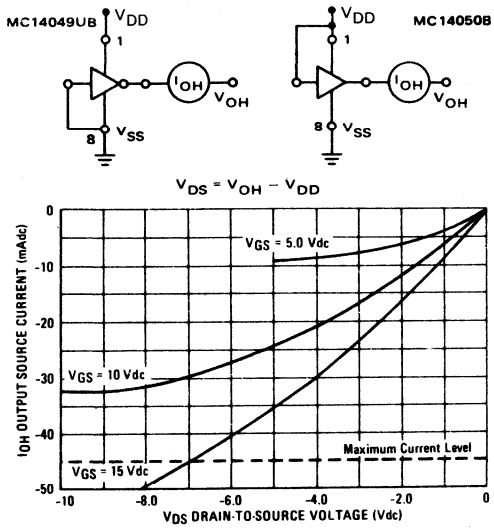


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

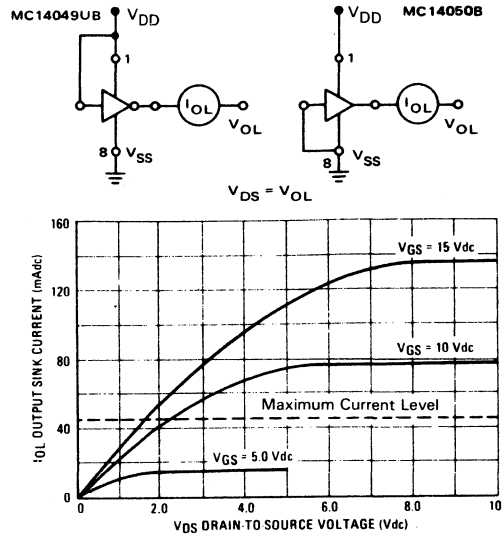


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

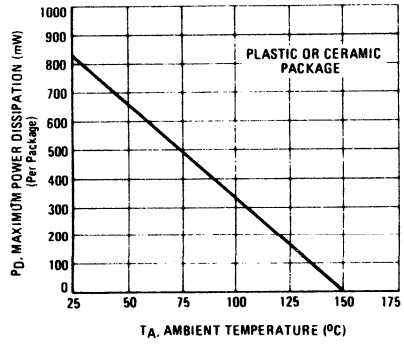
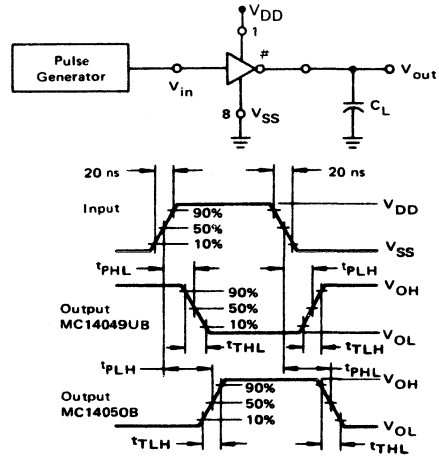


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

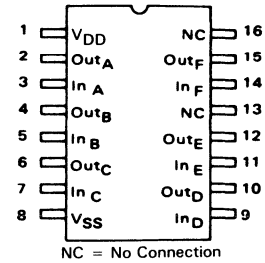


#Invert on MC14049UB only

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the V_{SS} pin, only.** Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



NC = No Connection

6

MOTOROLA

MC14051B
MC14052B
MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

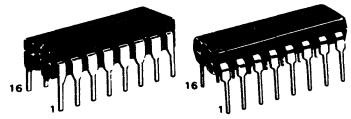
The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low-Noise — 12 $nV/\sqrt{Cycle}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON}, Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

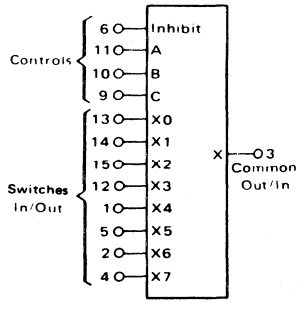
MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

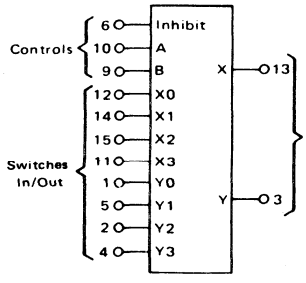
6

MC14051B
8-Channel Analog Multiplexer/Demultiplexer



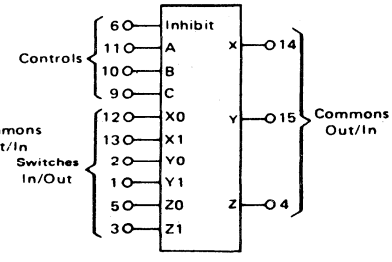
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052B
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14053B
Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3 \geq V_{SS} \geq V_{EE}$	3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	5	—	0.005	5	—	150	μA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	10	—	0.010	10	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	20	—	0.015	20	—	600	
Quiescent Current Per Package (CL/CP Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	20	—	0.005	20	—	150	μA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	40	—	0.010	40	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	80	—	0.015	80	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	$T_A = 25°C$ only	Typical			(0.07 μA/kHz)f + I_{DD}				μA
		10	(The channel component,				(0.20 μA/kHz)f + I_{DD}				
		15	$(V_{in} - V_{out})/R_{on}$, is not included.)				(0.36 μA/kHz)f + I_{DD}				
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5	R_{on} = per spec,	—	1.5	—	2.25	1.5	—	1.5	V
		10	I_{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5	R_{on} = per spec,	3.5	—	3.5	2.75	—	3.5	—	V
		10	I_{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Leakage Current (CL/CP Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN - X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	$V_{in} = 0$ V, No load	—	—	—	10	—	—	—	μV
ON Resistance (AL Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	800	—	250	1050	—	1300	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	400	—	120	500	—	550	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	880	—	250	1050	—	1200	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	450	—	120	500	—	520	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5		—	**70**	—	25	**70**	—	**135**	Ω
		10		—	**50**	—	10	**50**	—	**95**	
		15		—	**45**	—	10	**45**	—	**65**	
Off-Channel Leakage Current (AL Device) **(Figure 10)**	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) **(Figure 10)**	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14051B)	—	—	—	60	—	—	—	pF
			(MC14052B)				32				
			(MC14053B)				17				
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

* T_{low} = −55°C for AL Device, −40° for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

6

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	V_{DD}-V_{EE} Vdc	Typ # All Types	Max	Unit
Propagation Delay Times (Figure 6)	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 10 kΩ)					
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ, V_{EE} = V_{SS})	t_{PHZ}, t_{PLZ},				ns
Output "1" or "0" to High Impedance, or	t_{PZH}, t_{PZL}				
High Impedance to "1" or "0" Level					
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ, V_{EE} = V_{SS})	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	360	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Second Harmonic Distortion (R_L = 10KΩ, f = 1kHz) V_{in} = 5 V_{PP}	–	10	0.07	–	%
Bandwidth (Figure 7) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}-V_{EE}) p-p, C_L = 50pF 20 Log $\frac{V_{out}}{V_{in}}$ = −3 dB)	BW	10	17	—	MHz
Off Channel Feedthrough Attenuation (Figure 7) R_L = 1KΩ, V_{in} = 1/2 (V_{DD} − V_{EE}) p-p f_{in} = 4.5 MHz — MC14051B f_{in} = 30 MHz — MC14052B f_{in} = 55 MHz — MC14053B	–	10	−50	—	dB
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}-V_{EE}) p-p, f_{in} = 3.0 MHz	–	10	−50	–	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_1 = 1 kΩ, R_L = 10 kΩ Control t_{TLH} = t_{THL} = 20 ns, Inhibit = V_{SS})	–	10	75	–	mV

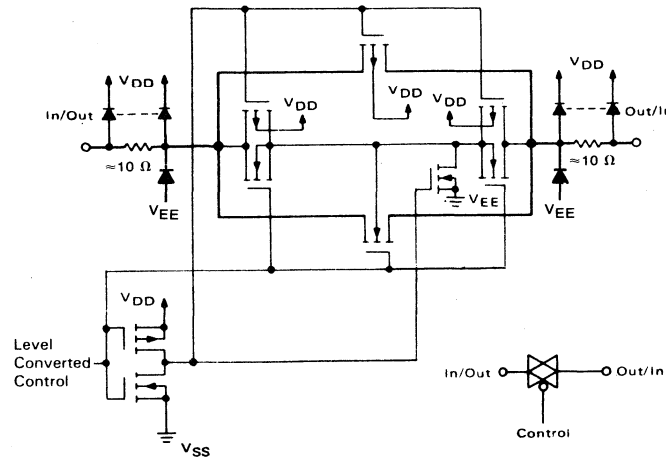
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC



TRUTH TABLE

Control Inputs				ON Switches					
	Select								
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM

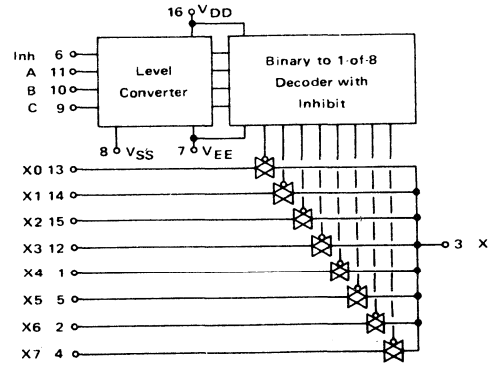


FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

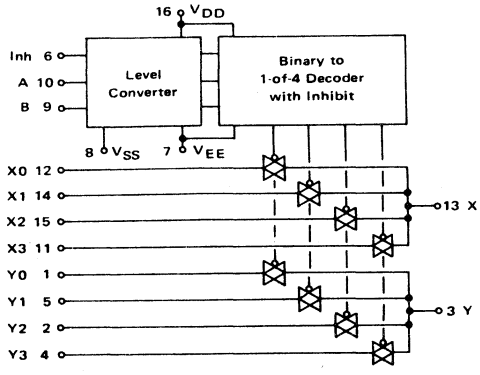
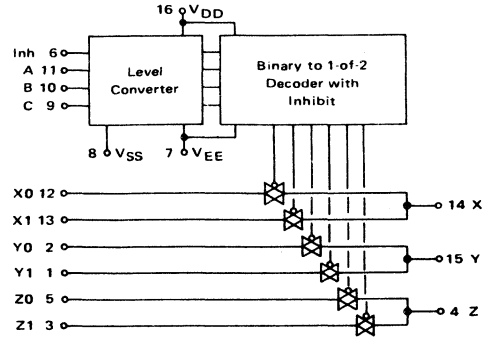


FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



6

TEST CIRCUITS

FIGURE 5 — ΔV ACROSS SWITCH

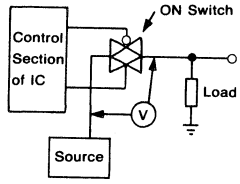


FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

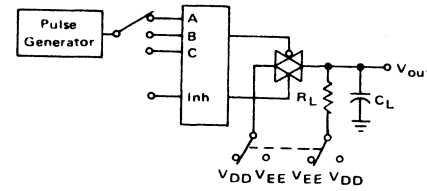


FIGURE 7 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

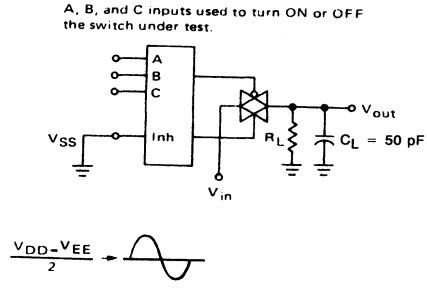


FIGURE 8 — CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

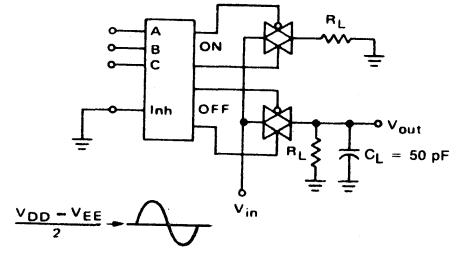


FIGURE 9 — CROSSTALK, CONTROL INPUT TO COMMON O/I

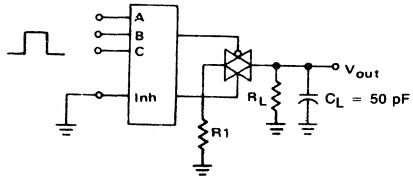


FIGURE 10 — OFF CHANNEL LEAKAGE

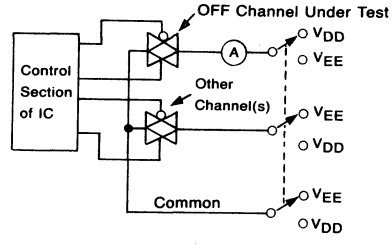
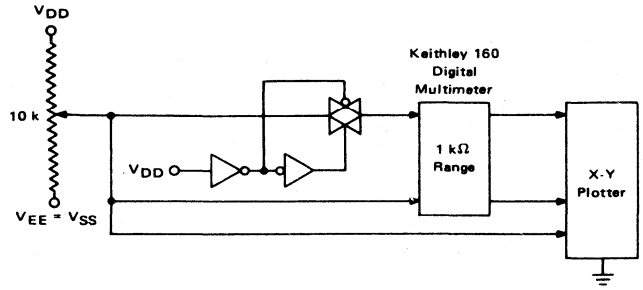


FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – V_{DD} = 7.5 V, V_{EE} = -7.5 V

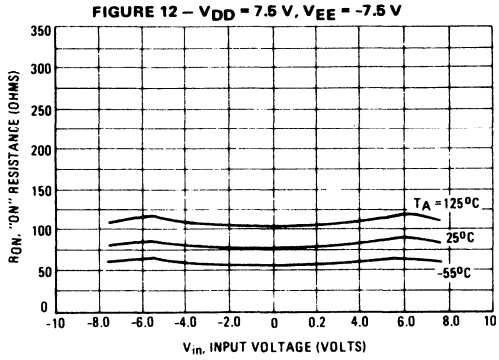


FIGURE 13 – V_{DD} = 5.0 V, V_{EE} = -5.0 V

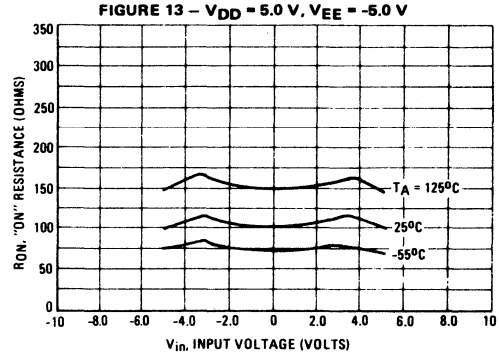


FIGURE 14 – V_{DD} = 2.5 V, V_{EE} = -2.5 V

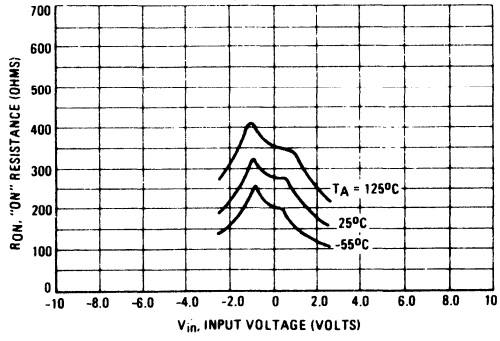
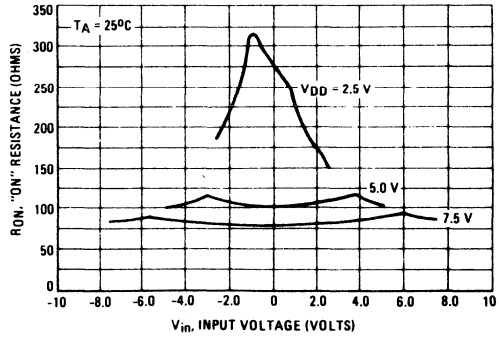
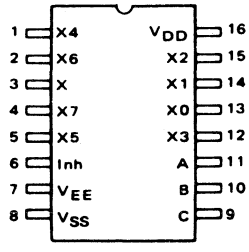


FIGURE 15 – COMPARISON AT 25°C, V_{DD} = -V_{EE}

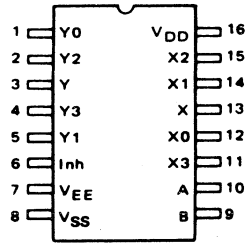


PIN ASSIGNMENT

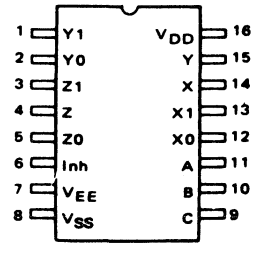
MC14051B



MC14052B



MC14053B



6

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} − V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} − V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a ½ volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 V, V_{SS} = +5 V, and V_{EE} = −3 V is acceptable. See the Table below.

FIGURE A — APPLICATION EXAMPLE

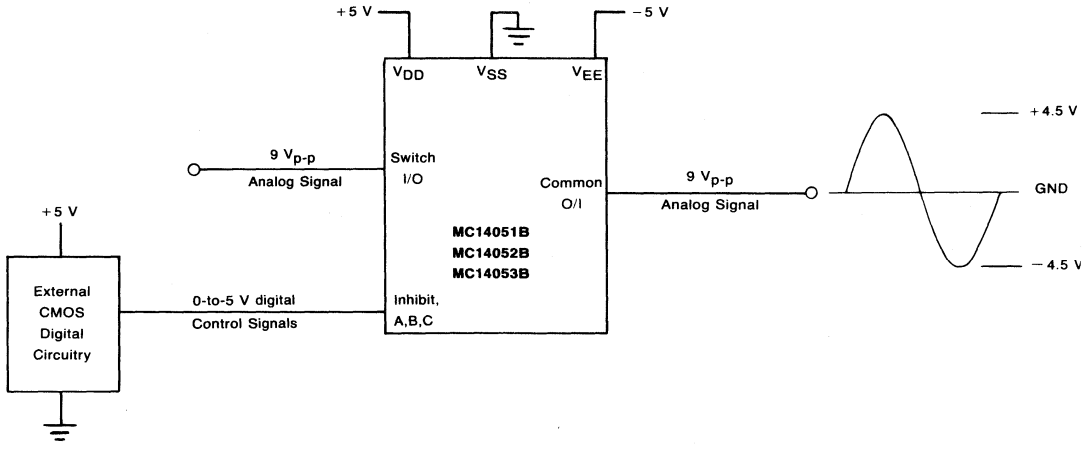
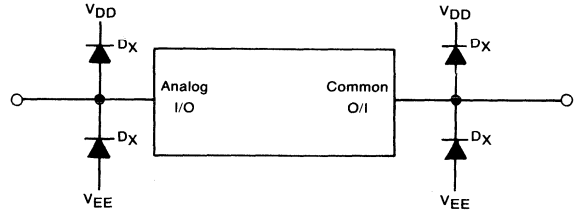


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V_{DD} in Volts	V_{SS} in Volts	V_{EE} in Volts	Control Inputs Logic High/Logic Low in Volts	Maximum Analog Signal Range in Volts
+8	0	−8	+8/0	+8 to −8 = 16 V_{p-p}
+5	0	−12	+5/0	+5 to −12 = 17 V_{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V_{p-p}
+5	0	−5	+5/0	+5 to −5 = 10 V_{p-p}
+10	+5	−5	+10/+5	+10 to −5 = 15 V_{p-p}

MOTOROLA

MC14060B

CMOS MSI

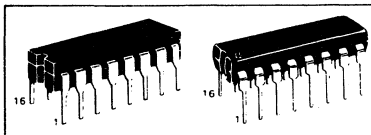
(LOW POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER AND OSCILLATOR

14-BIT BINARY COUNTER AND OSCILLATOR

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4060B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

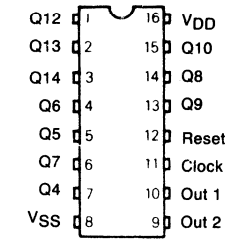
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

TRUTH TABLE

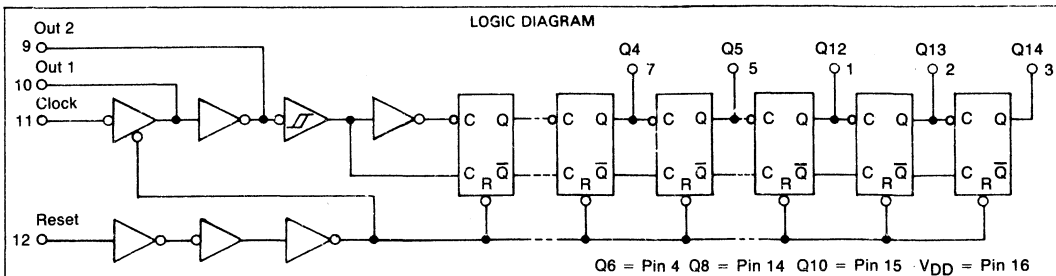
Clock	RESET	Output State
⌒	L	No Change
⌣	L	Advance to next state
X	H	All Outputs are low

X = Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



Q6 = Pin 4 Q8 = Pin 14 Q10 = Pin 15 V_{DD} = Pin 16
Q7 = Pin 6 Q9 = Pin 13 V_{SS} = Pin 8

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level										
$V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level										
$V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level										
(V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level										
(V_O = 0.5 or 4.5 V)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)										
(V_{OH} = 2.5 V) (Except Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V) Pins 9 and 10)	I_{OH}	5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	mA
(V_{OH} = 9.5 V)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink		5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)	I_{OL}	10	1.6	–	1.3	2.25	–	0.9	–	mA
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)										
(V_{OH} = 2.5 V) (Except Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V) Pins 9 and 10)	I_{OH}	5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	mA
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)	I_{OL}	10	1.3	–	1.1	2.25	–	0.9	–	mA
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)		5.0	–	5.0	–	0.005	5.0	–	150	
(Per Package)	I_{DD}	10	–	10	–	0.010	10	–	300	µA
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		5.0	–	20	–	0.005	20	–	150	
(Per Package)	I_{DD}	10	–	40	–	0.010	40	–	300	µA
		15	–	80	–	0.015	80	–	600	
Total Supply Current** (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.25\ \mu A/kHz)\ f + I_{DD}$							µA
		10	$I_T = (0.54\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}	5.0	–	40	200	ns
		10	–	25	100	
		15	–	20	80	
Output Fall Time (Counter Outputs)	t_{THL}	5.0	–	50	200	ns
		10	–	30	100	
		15	–	20	80	
Propagation Delay Time Clock to Q4	t_{PLH} t_{PHL}	5.0	–	415	740	ns
		10	–	175	300	
		15	–	125	200	
Clock to Q14		5.0	–	1.5	2.7	μs
		10	–	0.7	1.3	
		15	–	0.4	1.0	
Clock Pulse Width	t_{WH}	5.0	100	65	–	ns
		10	40	30	–	
		15	30	20	–	
Clock Pulse Frequency	f_ϕ	5.0	–	5	3.5	MHz
		10	–	14	8	
		15	–	17	12	
Clock Rise and Fall Time	t_{TLH} t_{THL}	5.0	No Limit			ns
		10				
		15				
Reset Pulse Width	t_W	5.0	120	40	–	ns
		10	60	15	–	
		15	40	10	–	
Propagation Delay Time Reset to Qn	t_{PHL}	5.0	–	170	360	ns
		10	–	80	160	
		15	–	60	100	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

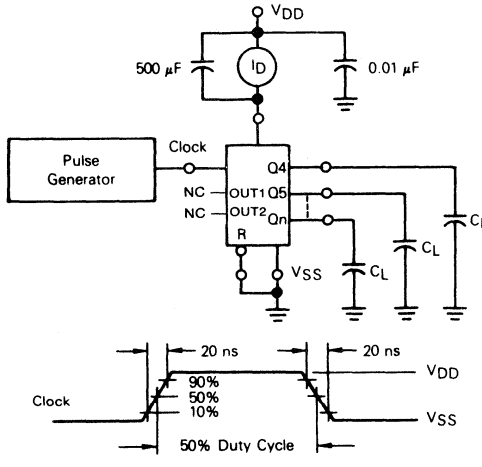
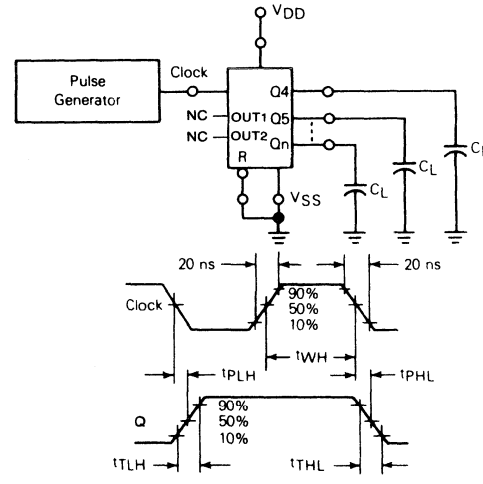
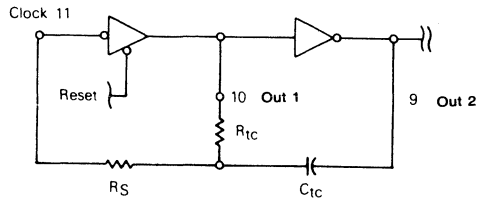


FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



$$f \approx \frac{1}{2.3\,R_{tc}C_{tc}}$$

if 1kHz ≤ f ≤ 100 kHz
and $2R_{tc} < R_s < 10R_{tc}$
(f in Hz, R in ohms, C in farads)

The formual may vary for other frequencies. Recommend maximum value for the resistors is 1 MΩ.

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

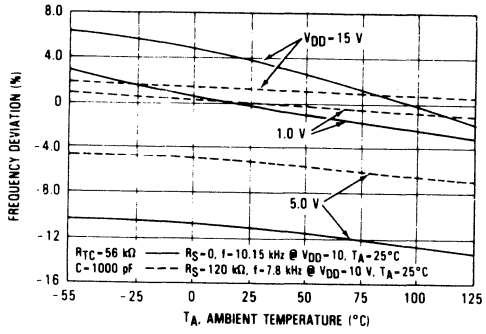


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

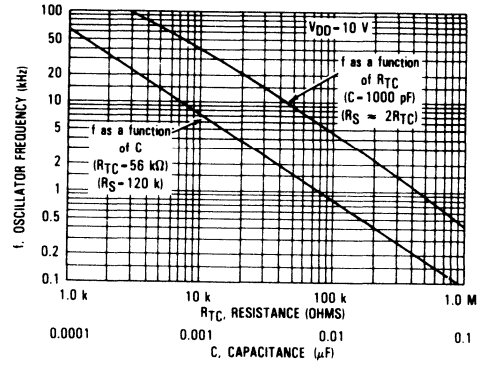


FIGURE 6 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT

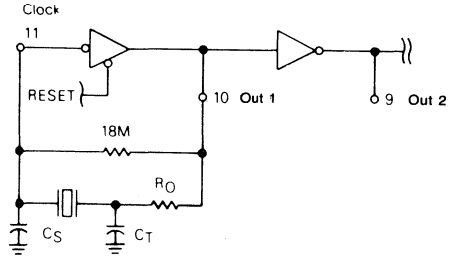


FIGURE 7 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	32	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_O	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Changes as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from −55°C to +25°C Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C Complete Oscillator*	−160	−560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

6

MOTOROLA

MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

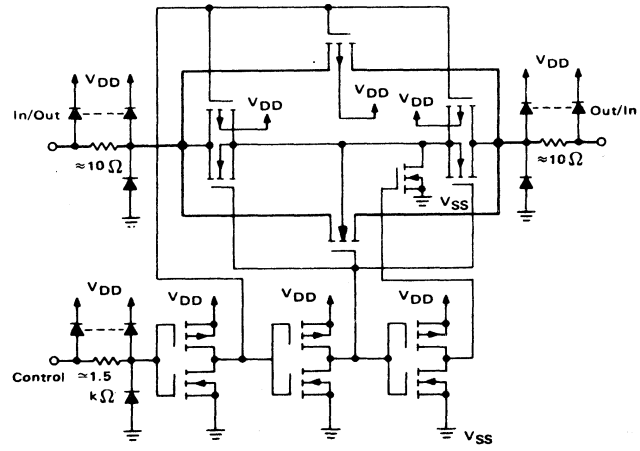
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016B
- For Lower R_{ON}, Use The HC4066 High-Speed CMOS Device

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

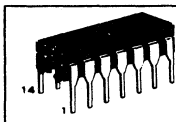
CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



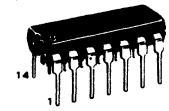
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632

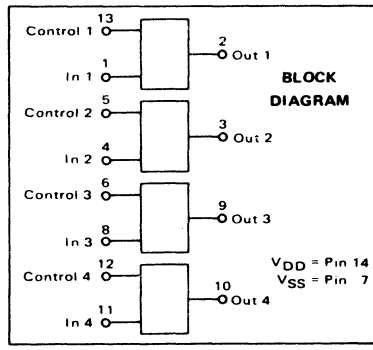


P SUFFIX
PLASTIC PACKAGE
CASE 646

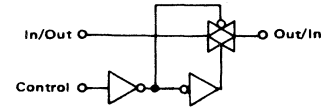
ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

6

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	—		3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	0.25	—	0.005	0.25	—	7.5	μA
		10	Switch I/O: $V_{SS} \leq V_{I/O} \leq V_{DD}$,	—	0.50	—	0.010	0.50	—	15	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	1.00	—	0.015	1.00	—	30	
Quiescent Current Per Package (CL/CP Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	1.0	—	0.005	1.0	—	7.5	μA
		10	Switch I/O: $V_{SS} \leq V_{I/O} \leq V_{DD}$,	—	2.0	—	0.010	2.0	—	15	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	4.0	—	0.015	4.0	—	30	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	T_A = 25°C only	Typical: (0.07 μA/kHz)f + I_{DD}							μA
		10	(The channel component,	Typical: (0.20 μA/kHz)f + I_{DD}							
		15	$(V_{in} - V_{out})/R_{on}$, is not included.)	Typical: (0.36 μA/kHz)f + I_{DD}							
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5	R_{on} = per spec,	—	1.5	—	2.25	1.5	—	1.5	V
		10	I_{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5	R_{on} = per spec,	3.5	—	3.5	2.75	—	3.5	—	V
		10	I_{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Leakage Current (CL/CP Device)	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (Figure 1)**	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No load	—	—	—	10	—	—	—	μV
ON Resistance (AL Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	800	—	250	1050	—	1300	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	400	—	120	500	—	550	
		15	and V_{in} = 0 to V_{DD} (Switch)	—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	880	—	250	1050	—	1200	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	450	—	120	500	—	520	
		15	and V_{in} = 0 to V_{DD} (Switch)	—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (AL Device) (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	—		—	—	—	0.47	—	—	—	pF

* T_{low} = −55°C for AL Device, −40° for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

6

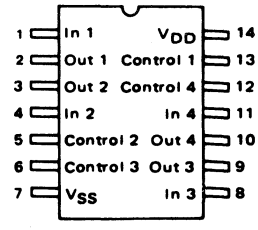
ELECTRICAL CHARACTERISTICS* ($C_L = 50$ pF, $T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Times $V_{SS} = 0$ Vdc						
Input to Output ($R_L = 10$ kΩ)	t_{PLH}, t_{PHL}					ns
t_{PLH}, $t_{PHL} = (0.17$ ns/pF$)\ C_L + 15.5$ ns		5.0	—	20	40	
t_{PLH}, $t_{PHL} = (0.08$ ns/pF$)\ C_L + 6.0$ ns		10	—	10	20	
t_{PLH}, $t_{PHL} = (0.06$ ns/pF$)\ C_L + 4.0$ ns		15	—	7.0	15	
Control to Output ($R_L = 1$ kΩ) (Figure 2)						
Output "1" to High Impedance	t_{PHZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
Second Harmonic Distortion $V_{SS} = -5$ Vdc ($V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ kΩ, f = 1.0 kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) $V_{SS} = -5$ Vdc ($R_L = 1$ kΩ, $20 \log \frac{V_{out}}{V_{in}} = -3$ dB, $C_L = 50$ pF, $V_{in} = 5\ V_{p-p}$)	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) $V_{SS} = -5$ Vdc ($V_{in} = 5\ V_{p-p}$, $R_L = 1$ kΩ, $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	−50	—	dB
Channel Separation (Figure 4) $V_{SS} = -5$ Vdc ($V_{in} = 5\ V_{p-p}$, $R_L = 1$ kΩ, $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	−50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) $V_{SS} = -5$ Vdc ($R_1 = 1$ kΩ, $R_L = 10$ kΩ, Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV_{p-p}

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

TEST CIRCUITS

FIGURE 1 — ΔV ACROSS SWITCH

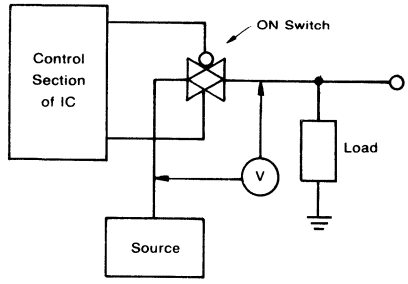


FIGURE 2 — TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

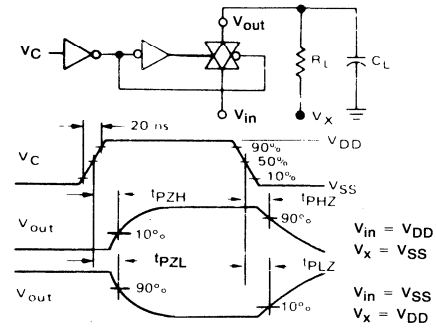


FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

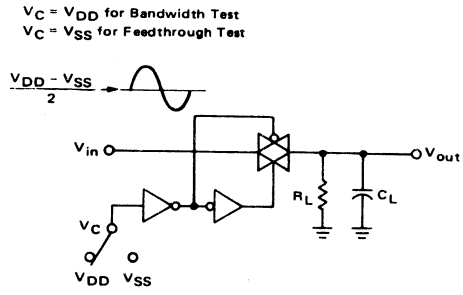


FIGURE 4 — CHANNEL SEPARATION

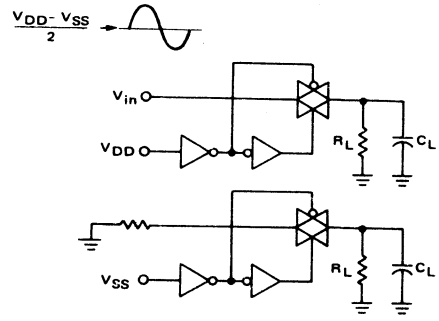


FIGURE 5 – CROSSTALK, CONTROL TO OUTPUT

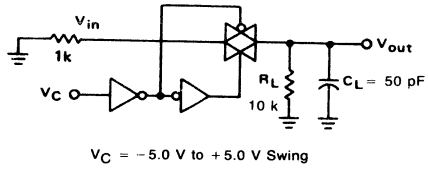


FIGURE 6 — OFF CHANNEL LEAKAGE

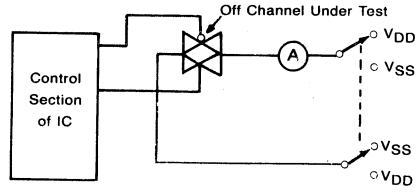
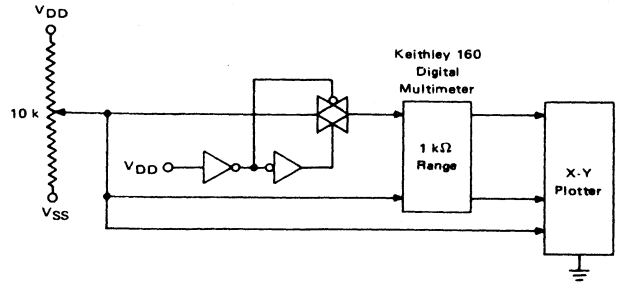


FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V

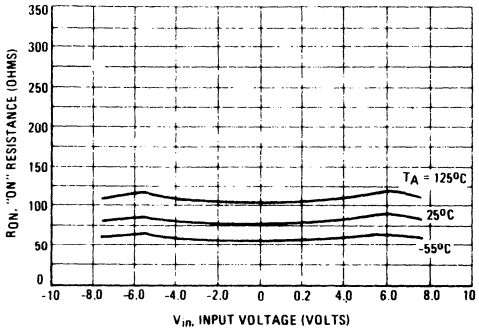


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V

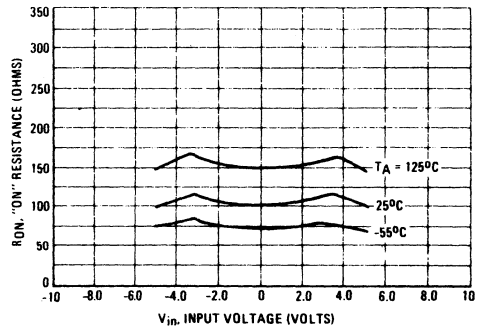


FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

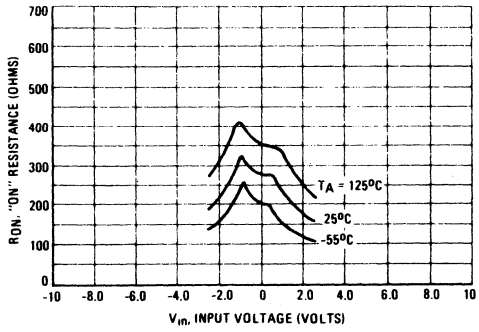
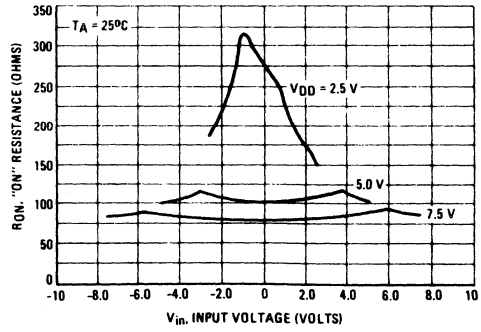


FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}



6

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}.

The example shows a 5 volt peak-to-peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS}.

FIGURE A — APPLICATION EXAMPLE

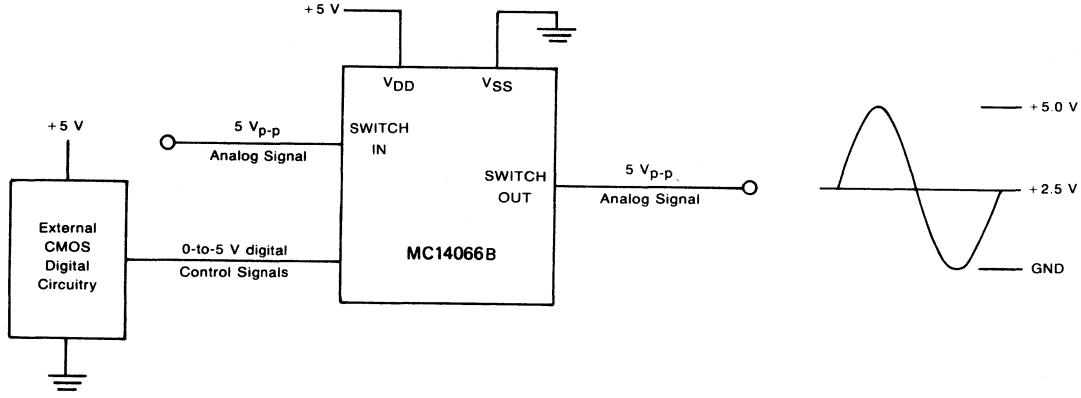
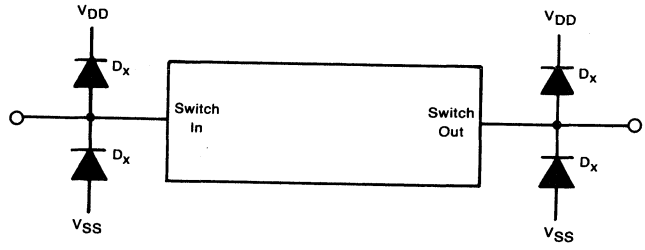


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



6

MOTOROLA

MC14067B
MC14097B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled analog switches featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

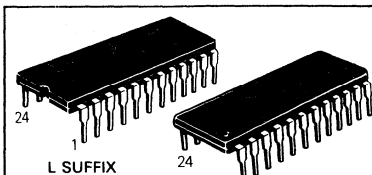
The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B, and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches (see MC14097 truth table).

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B

CMOS
(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



L SUFFIX
CERAMIC PACKAGE
CASE 623

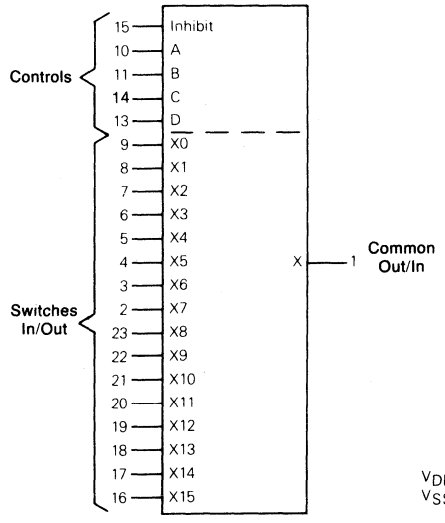
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

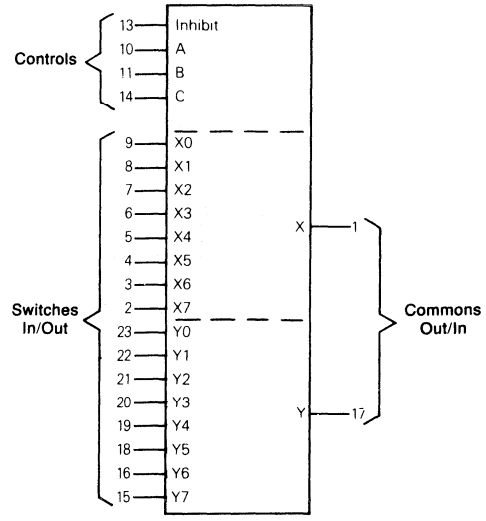
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MC14067B
16-Channel Analog
Multiplexer/Demultiplexer



V_{DD} = Pin 24
V_{SS} = Pin 12

MC14097B
Dual 8-Channel Analog
Multiplexer/Demultiplexer



6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14067 TRUTH TABLE

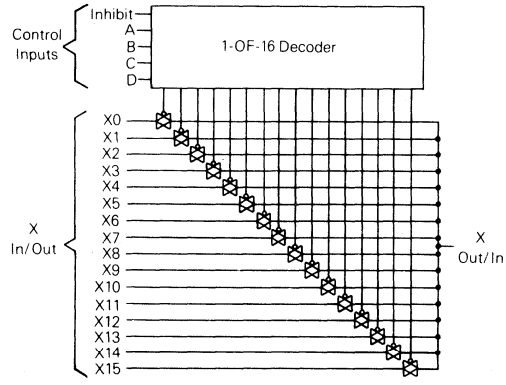
Control Inputs					Selected
A	B	C	D	Inh	Channel
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

MC14097 TRUTH TABLE

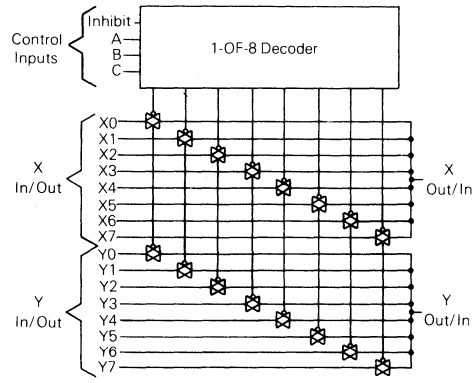
Control Inputs				Selected
A	B	C	Inh	Channels
X	X	X	1	None
0	0	0	0	X0 Y0
1	0	0	0	X1 Y1
0	1	0	0	X2 Y2
1	1	0	0	X3 Y3
0	0	1	0	X4 Y4
1	0	1	0	X5 Y5
0	1	1	0	X6 Y6
1	1	1	0	X7 Y7

X = Don't Care

MC14067 FUNCTIONAL DIAGRAM



MC14097 FUNCTIONAL DIAGRAM



6

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	—		3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	5	—	0.005	5	—	150	μA
		10	Switch I/O: $V_{SS} \leq V_{I/O} \leq V_{DD}$,	—	10	—	0.010	10	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	20	—	0.015	20	—	600	
Quiescent Current Per Package (CL/CP Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	20	—	0.005	20	—	150	μA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	40	—	0.010	40	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	80	—	0.015	80	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	$T_A = 25°C$ only	Typical			(0.07 μA/kHz)f + I_{DD}				μA
		10	(The channel component,				(0.20 μA/kHz)f + I_{DD}				
		15	$(V_{in} - V_{out})/R_{on}$, is not included.)				(0.36 μA/kHz)f + I_{DD}				
CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5	R_{on} = per spec,	—	1.5	—	2.25	1.5	—	1.5	V
		10	I_{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5	R_{on} = per spec,	3.5	—	3.5	2.75	—	3.5	—	V
		10	I_{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Leakage Current (CL/CP Device)	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN - X, Y (Voltages Referenced to V_{SS})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	$V_{in} = 0$ V, No load	—	—	—	10	—	—	—	μV
ON Resistance (AL Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	800	—	250	1050	—	1300	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	400	—	120	500	—	550	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	880	—	250	1050	—	1200	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	450	—	120	500	—	520	
		15	and $V_{in} = 0$ to V_{DD} (Switch)	—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5		—	**70**	—	25	**70**	—	**135**	Ω
		10		—	**50**	—	10	**50**	—	**95**	
		15		—	**45**	—	10	**45**	—	**65**	
Off-Channel Leakage Current (AL Device) (Figure 2)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 2)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	**Inhibit = V_{DD} (MC14067B)**	—	—	—	**100**	—	—	—	pF
			(MC14097B)				**60**				
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

* T_{low} = −55°C for AL Device, −40° for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

6

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	$V_{DD} - V_{SS}$ Vdc	Typ #	Max	Unit
Propagation Delay Times Channel Input-to-Channel Output (R_L = 200kΩ) MC14067B	t_{PLH}, t_{PHL}				ns
	(Figure 3)	5.0	35	90	
		10	15	40	
		15	12	30	
MC14097B					ns
		5.0	25	65	
		10	10	25	
		15	7	18	
Control Input-to-Channel Output Channel Turn-On Time (R_L = 10 kΩ) MC14067B/097B	t_{PZH}, t_{PZL}				ns
	(Figure 4)	5.0	240	600	
		10	115	290	
		15	75	190	
Channel Turn-Off Time (R_L = 300 kΩ) MC14067B/097B	t_{PHZ}, t_{PLZ}				ns
	(Figure 4)	5.0	250	625	
		10	120	300	
		15	75	190	
Any Pair of Address Inputs to Output MC14067B	t_{PLH}, t_{PHL}				ns
		5.0	280	700	
		10	115	290	
		15	85	215	
MC14097B					ns
	(Figure 10)	5.0	250	625	
		10	100	250	
		15	75	190	
Second Harmonic Distortion (R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p})	—	10	0.3	—	%
ON Channel Bandwidth [R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{SS})_{p-p}$(sine-wave)]	BW				MHz
$20 \log_{10} \frac{V_{out}}{V_{in}} = -3$ dB MC14067B	(Figure 5)	10	15	—	
MC14097B		10	25	—	
Off Channel Feedthrough Attenuation [R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{SS})_{p-p}$(sine-wave)] f_{in} = 20 MHz – MC14067B f_{in} = 12 MHz – MC14097B	— (Figure 5)	10	−40	—	dB
Channel Separation [R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{SS})_{p-p}$(sine-wave)] f_{in} = 20 MHz	— (Figure 6)	10	−40	—	dB
Crosstalk, Control Inputs-to-Common O/I (R1 = 1kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns, Inhibit = V_{SS})	— (Figure 7)	10	30	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 — ΔV ACROSS SWITCH

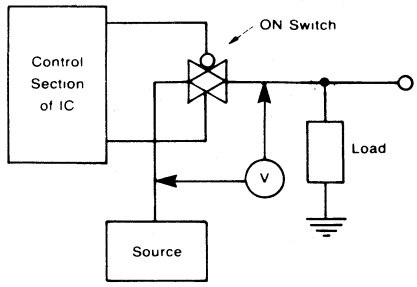
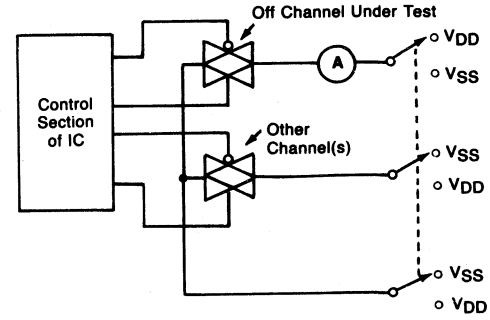
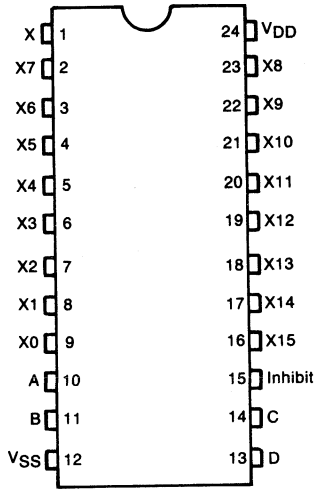


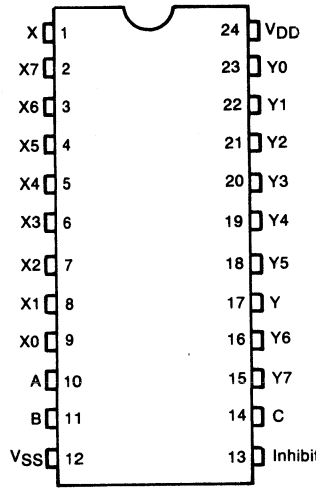
FIGURE 2 — OFF CHANNEL LEAKAGE



MC14067B PIN ASSIGNMENT



MC14097B PIN ASSIGNMENT



6

FIGURE 3 — PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS V_{in} to V_{out}

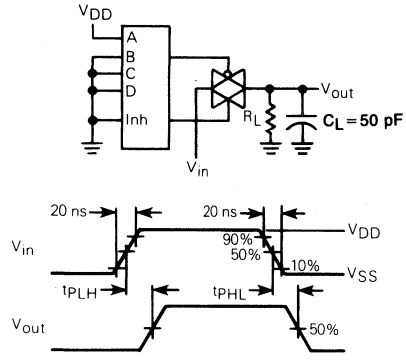


FIGURE 4 — TURN-ON AND DELAY TURN-OFF TEST CIRCUIT AND WAVEFORMS

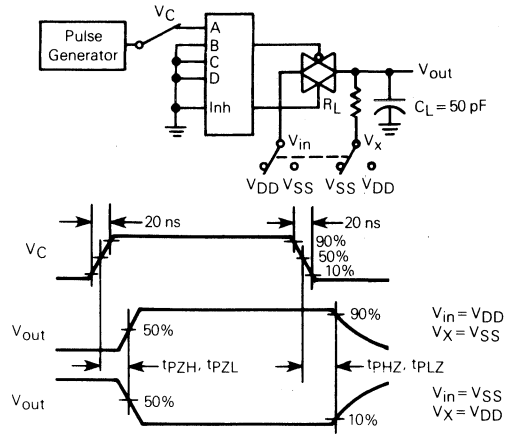


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

A, B, and C inputs used to turn ON or OFF the switch under test.

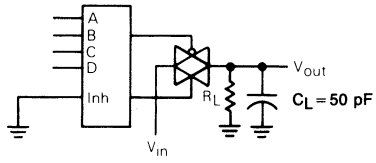


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

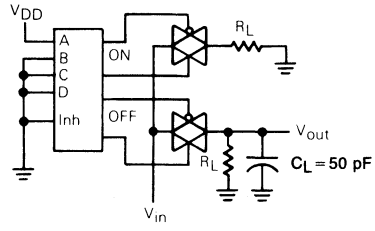
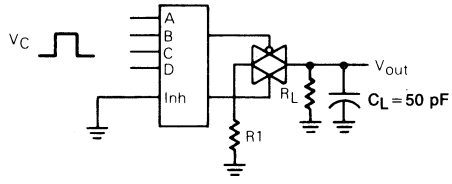


FIGURE 7 — CROSSTALK, CONTROL TO COMMON O/I



6

FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT

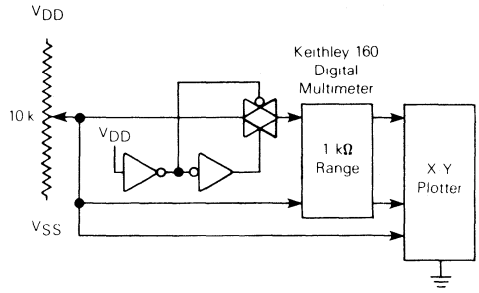
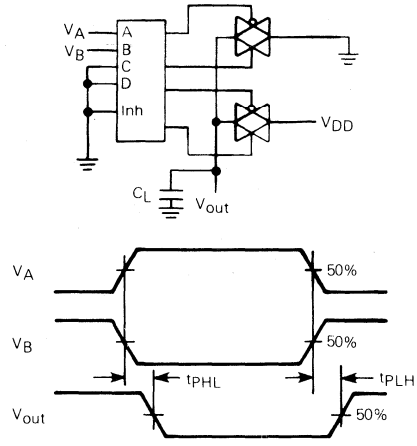


FIGURE 10 – PROPAGATION DELAY, ANY PAIR OF ADDRESS INPUTS to OUTPUT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 11 – V_{DD} = 7.5 V, V_{SS} = –7.5 V

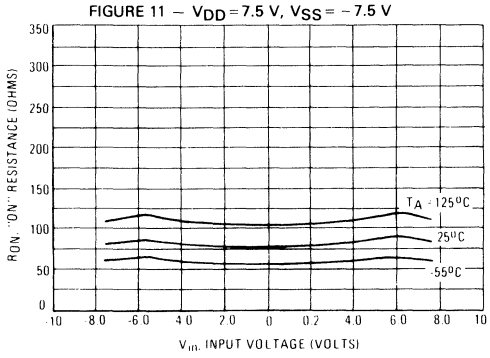


FIGURE 12 – V_{DD} = 5.0 V, V_{SS} = –5.0 V

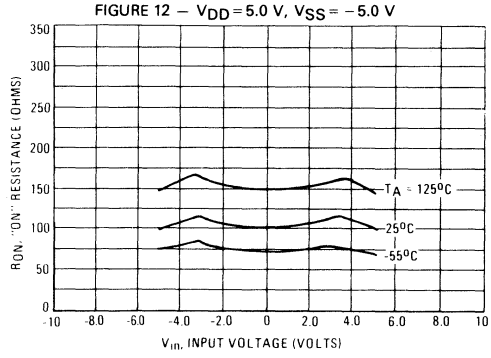


FIGURE 13 – V_{DD} = 2.5 V, V_{SS} = –2.5 V

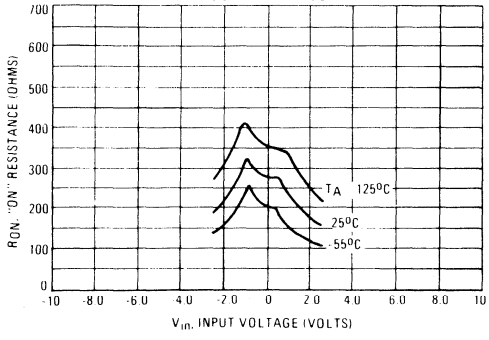
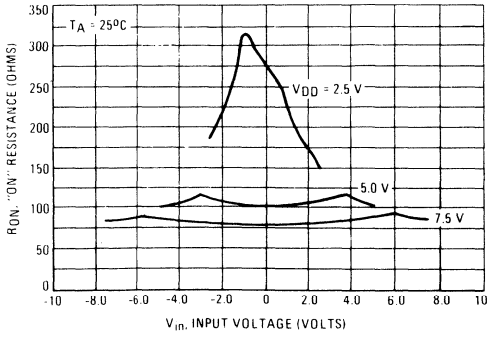


FIGURE 14 – COMPARISON AT 25°C, V_{DD} = –V_{SS}



6

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/ Demultiplexer. The 0-to-5 volt Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{SS}.

FIGURE A — APPLICATION EXAMPLE

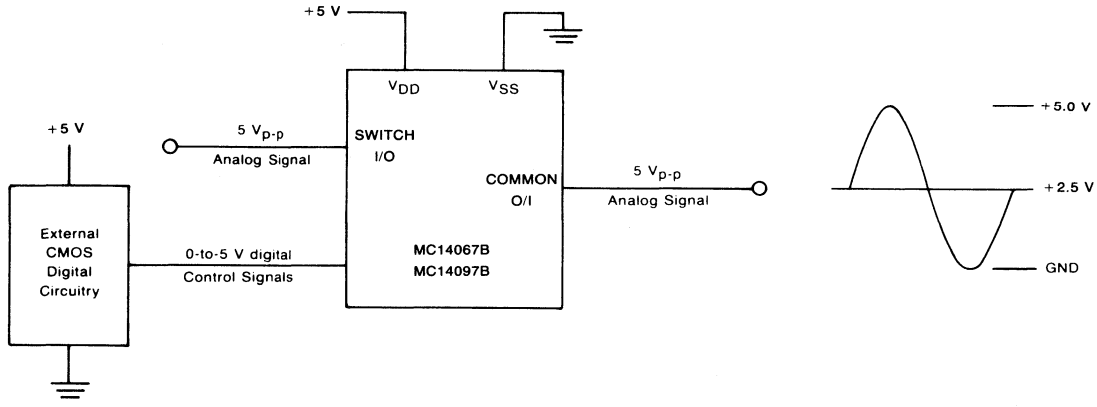
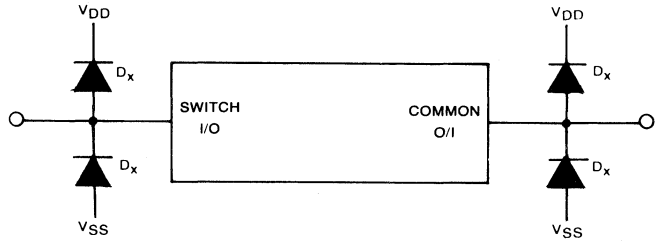


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



6

MOTOROLA

MC14068B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NAND" GATE

FOR COMPLETE DATA SEE MC14001B

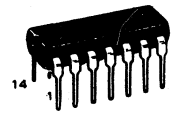
8 – INPUT "NAND" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

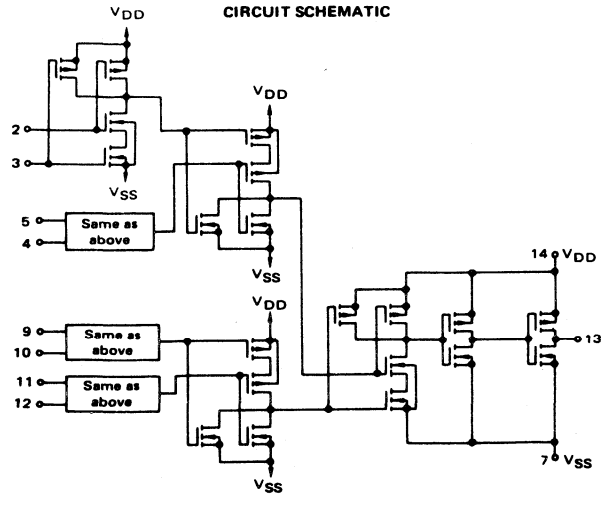
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

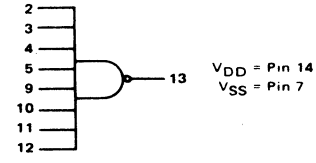
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



NC Pin 1,8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14069UB

HEX INVERTER

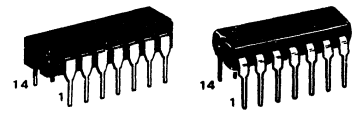
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

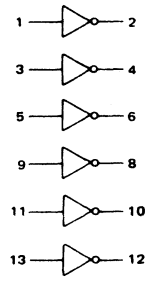
C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

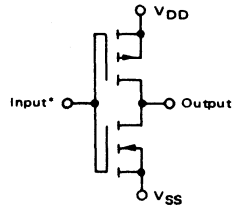
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



*Double diode protection on all inputs not shown.

PIN ASSIGNMENT

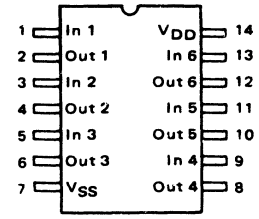
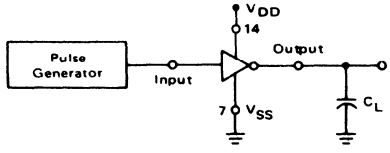
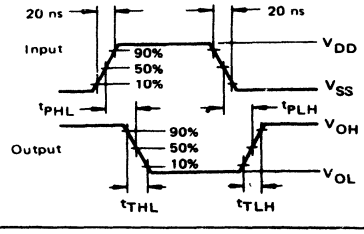


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} 0)	C_{in}	–		—	—	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	—	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	—	0.50	–	0.0010	0.50	–	15	
		15	—	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/6$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/6$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/6$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
$t_{TLH}, t_{THL} = (1.35\ ns/pF)\ C_L + 33\ ns$		5.0	–	–	–	100	200	–	–	
$t_{TLH}, t_{THL} = (0.60\ ns/pF)\ C_L + 20\ ns$		10	–	–	–	50	100	–	–	
$t_{TLH}, t_{THL} = (0.40\ ns/pF)\ C_L + 20\ ns$		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
$t_{PLH}, t_{PHL} = (0.90\ ns/pF)\ C_L + 20\ ns$		5.0	–	–	–	65	125	–	–	
$t_{PLH}, t_{PHL} = (0.36\ ns/pF)\ C_L + 22\ ns$		10	–	–	–	40	75	–	–	
$t_{PLH}, t_{PHL} = (0.26\ ns/pF)\ C_L + 17\ ns$		15	–	–	–	30	55	–	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14070B

QUAD EXCLUSIVE "OR" GATE

MC14077B

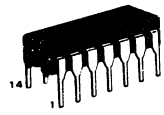
QUAD EXCLUSIVE "NOR" GATE

CMOS SSI

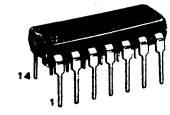
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B — Replacement for CD4030B and CD4070B Types
- MC14077B – Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE



CASE 646
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

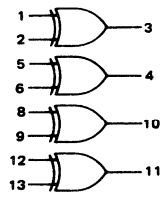
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

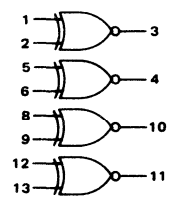
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

MC14070B
Quad Exclusive OR Gate

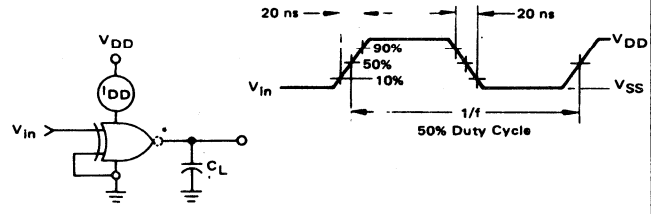


MC14077B
Quad Exclusive NOR Gate



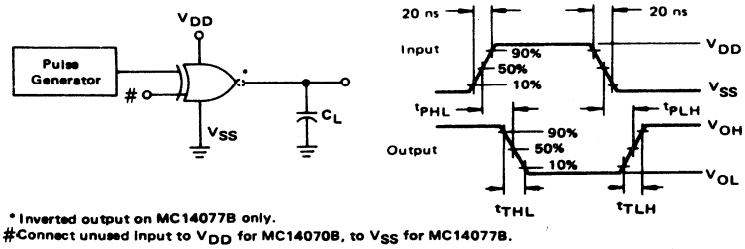
V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



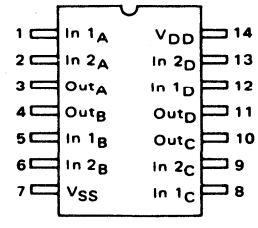
*Inverted output on MC14077B only.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



* Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 130 ns		5.0	–	–	–	175	350	–	–	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 57 ns		10	–	–	–	75	150	–	–	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	–	–	55	110	–	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MOTOROLA

MC14071B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

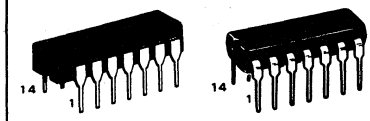
QUAD 2-INPUT "OR" GATE

FOR COMPLETE DATA SEE MC14001B

QUAD 2-INPUT "OR" GATE

The MC14071B is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). The primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4071B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

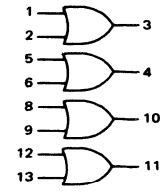
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

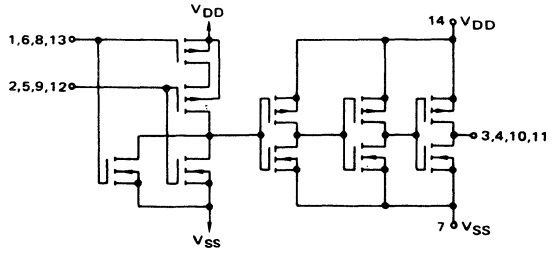
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/4 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14072B

DUAL 4 INPUT "OR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "OR" GATE

FOR COMPLETE DATA SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

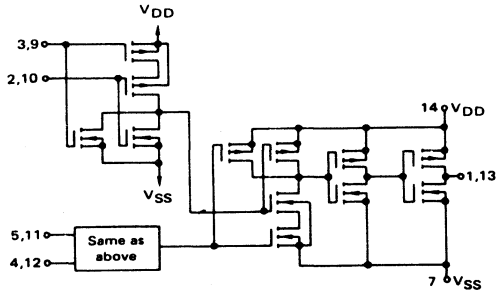
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

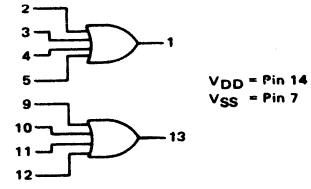
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATICS
(1/2 of Device Shown)



LOGIC DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14073B

TRIPLE 3–INPUT "AND" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

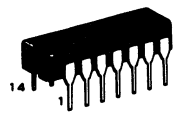
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE

FOR COMPLETE DATA
SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

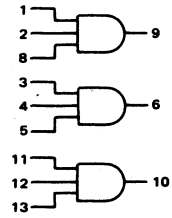
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

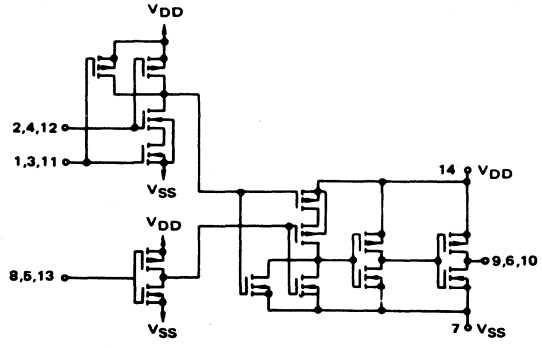
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14075B

TRIPLE 3–INPUT "OR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

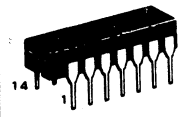
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE

FOR COMPLETE DATA
SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

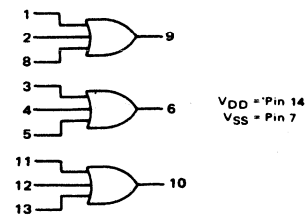
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

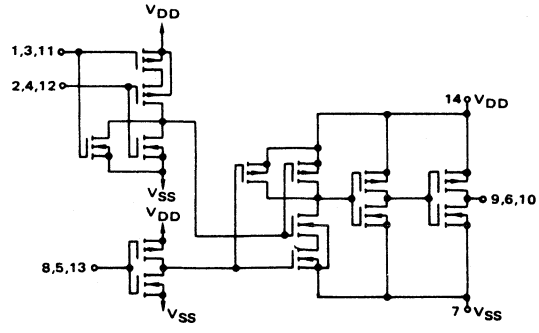
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/3 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14076B

4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

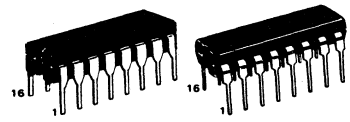
The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
  Schottky TTL Load Over the Rated Temper

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL or UBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP or UBCP (Plastic Package)
MC14XXXBCL or UBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

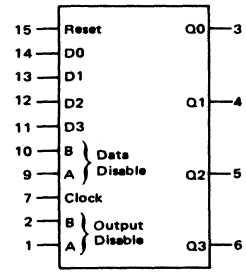
FUNCTION TABLE

INPUTS					OUTPUT
		Data Disable		Data	
Reset	Clock	A	B	D	Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	↗	1	X	X	Q_n
0	↗	X	1	X	Q_n
0	↗	0	0	0	0
0	↗	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
3-State Propagation Delay, Output "1" or "0" to High Impedance	t_{PHZ}, t_{PLZ}	5.0	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
3-State Prgpagation Delay, High Impedance to "1" or "0" Level	t_{PZH}, t_{PZL}	5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Clock Pulse Width	t_{WH}	5.0	260	130	–	ns
		10	110	55	–	
		15	80	40	–	
Reset Pulse Width	t_{WH}	5.0	370	185	–	ns
		10	150	75	–	
		15	110	55	–	
Data Setup Time	t_{su}	5.0	30	15	–	ns
		10	10	5	–	
		15	4	2	–	
Data Hold Time	t_h	5.0	130	65	–	ns
		10	60	30	–	
		15	50	25	–	
Data Disable Setup Time	t_{su}	5.0	220	110	–	ns
		10	80	40	–	
		15	50	25	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
		10	–	9.0	4.5	
		15	–	12	6.0	

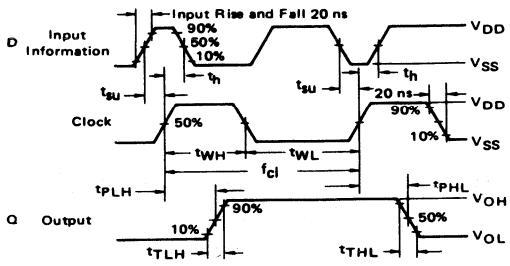
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

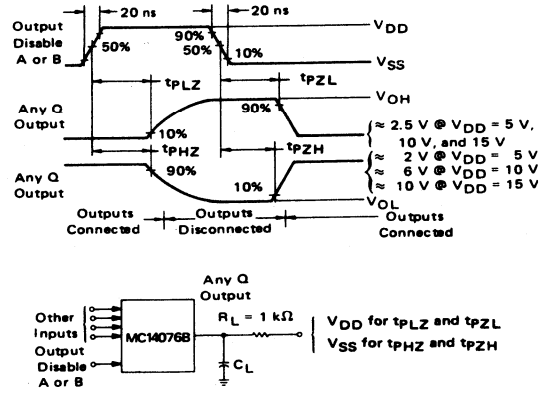
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FIGURE 1 – TIMING DIAGRAM

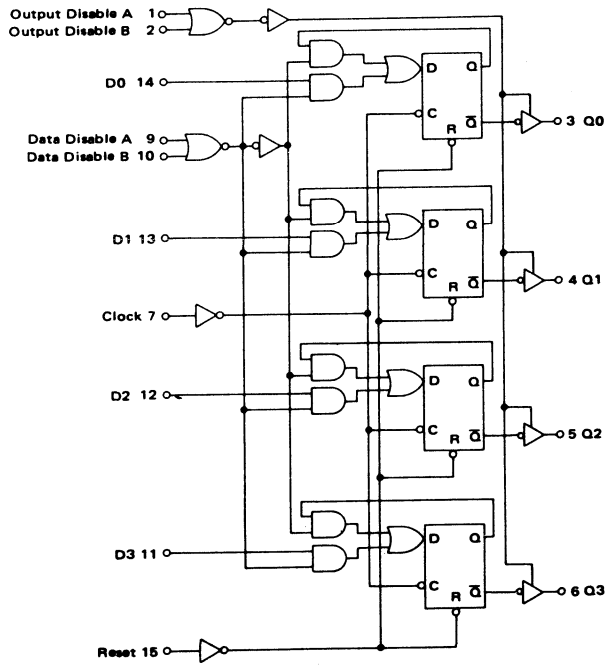


Reset = 0
Data Disable A and B = 0
Output Disable A and B = 0

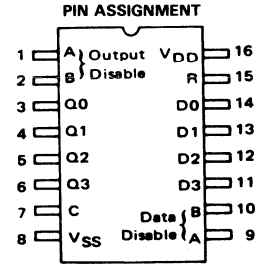
FIGURE 2 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



6

MOTOROLA

MC14077B

QUAD EXCLUSIVE "NOR" GATE

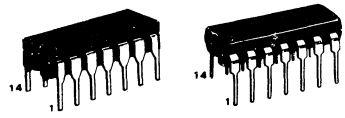
FOR COMPLETE DATA
SEE MC14070B

CMOS SSI

QUAD EXCLUSIVE "NOR"GATE

The MC14077B quad exclusive NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolothic structure. This complementary MOS logic gate finds primary use where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14077B – Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE

CASE 646
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

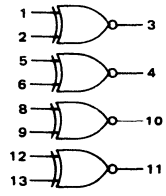
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

MC14077B
Quad Exclusive NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

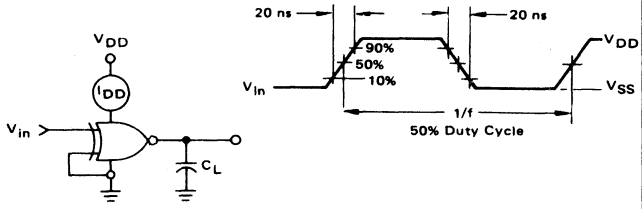
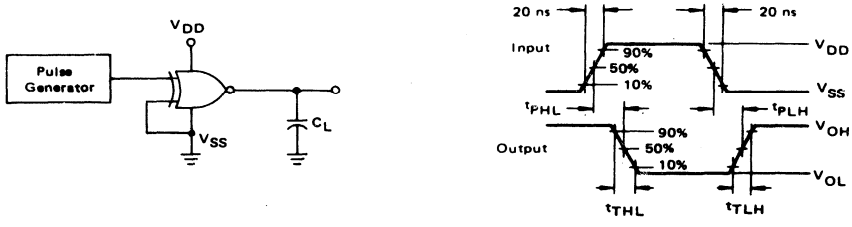


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

MOTOROLA

MC14078B

8 – INPUT "NOR" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

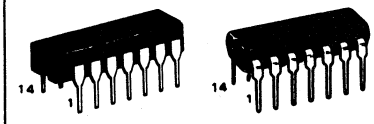
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NOR" GATE

FOR COMPLETE DATA
SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

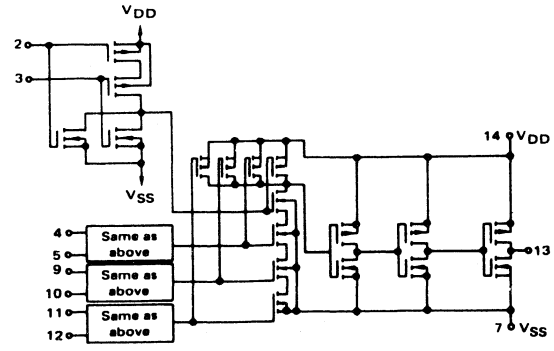
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

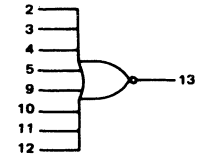
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



N.C. pins 1, 6, and 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14081B

QUAD 2-INPUT "AND" GATE

The MC14081B is constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). The primary use is where low power dissipation and/or high noise immunity is desired.

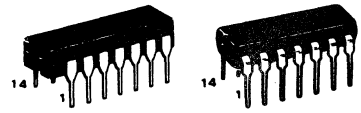
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE

FOR COMPLETE DATA SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

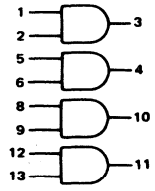
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

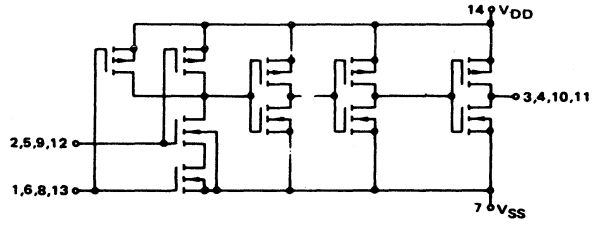
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14082B

DUAL 4-INPUT "AND" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

CMOS SSI

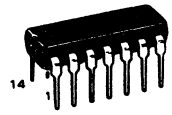
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE

FOR COMPLETE DATA SEE MC14001B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

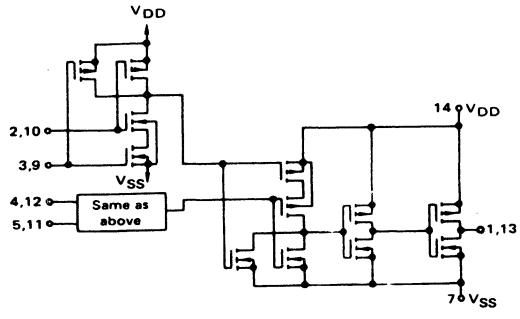
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

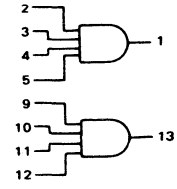
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATICS
(1/2 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14093B

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

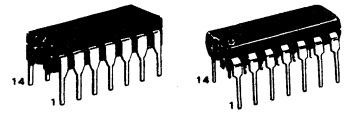
The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

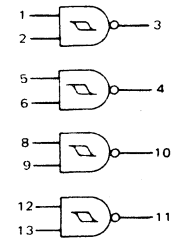
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4 µA/kHz) f + I_{DD}							
		15	I_T = (3.6 µA/kHz) f + I_{DD}							
Hysteresis Voltage	V_H	5.0	0.20	0.62	0.17	0.26	0.6	0.13	0.6	Vdc
(Pins 1, 5, 8 and 12 held high		10	0.29	0.85	0.25	0.38	0.8	0.20	0.8	
or Pins 2, 6, 9 and 13 held high)		15	0.39	1.20	0.33	0.50	0.9	0.27	1.1	
Threshold Voltage (Pins 2, 5, 9, 12 held high or Pins 1, 6, 8, 13 held high) **Positive-Going**	V_{T+}	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
		10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	
		15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	
Negative-Going	V_{T-}	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.05	6.08	2.60	8.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

#Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

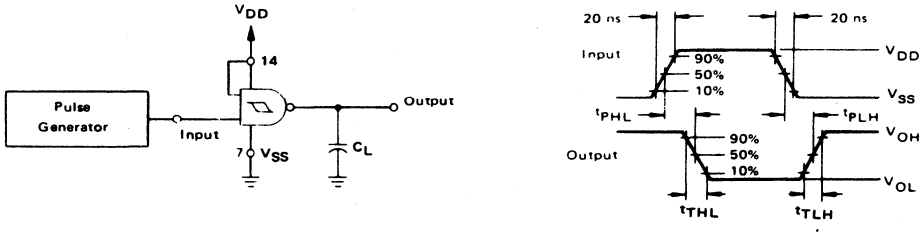
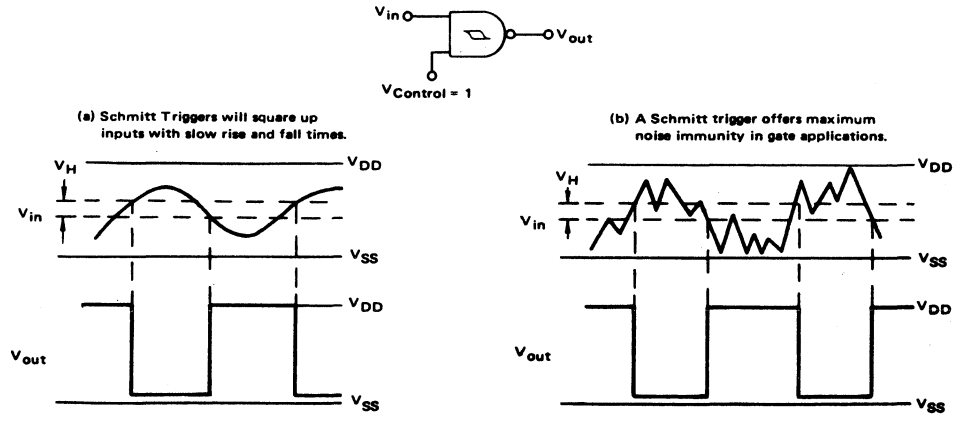
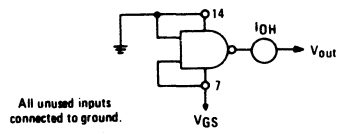


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



6

FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT



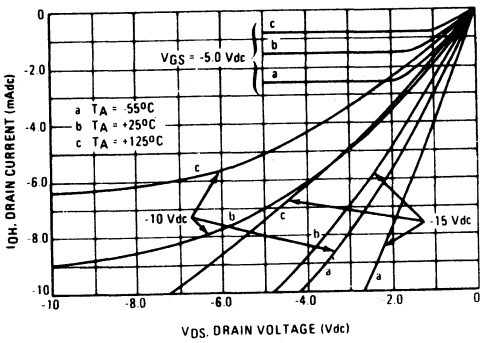
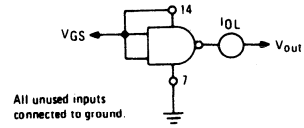


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



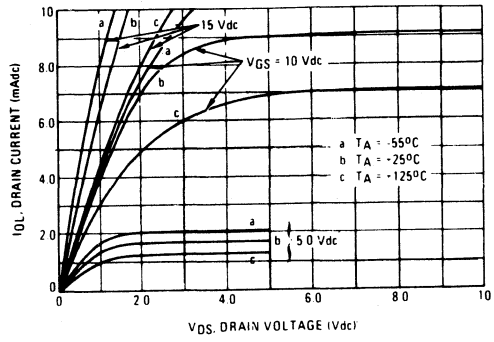
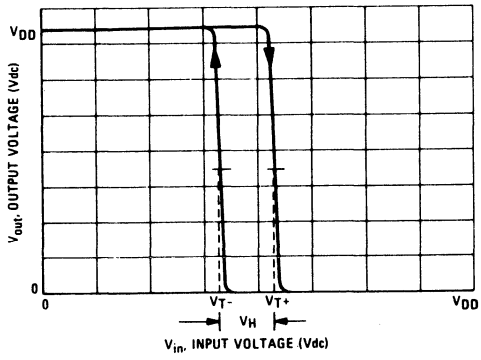
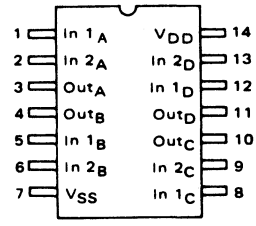


FIGURE 5 – TYPICAL TRANSFER CHARACTERISTICS



PIN ASSIGNMENT



6

MOTOROLA

MC14094B

8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

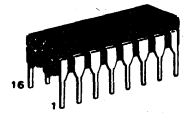
Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Pin-for-Pin Compatible with CD4094B

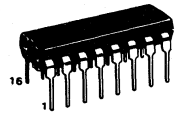
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-STAGE SHIFT/STORE REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

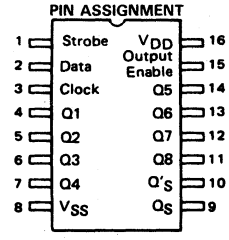
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

PIN ASSIGNMENT



Clock	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs Q_N	Serial Outputs Q_S*	Serial Outputs Q'_S
↑	0	X	X	Z	Z	Q7	No Chg.
↓	0	X	X	Z	Z	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	Q_N-1	Q7	No Chg.
↑	1	1	1	1	Q_N-1	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

Z = High Impedance
X = Don't Care
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0		5.0	–	0.005	5.0	–	150	µAdc
		10		10	–	0.010	10	–	300	
		15		20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.1 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (14 µA/kHz) f + I_{DD}							
		15	I_T = (140 µA/kHz) f + I_{DD}							
3-State Output Leakage Current (AL Device)	I_{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	µA
3-State Output Leakage Current (CL/CP Device)	I_{TL}	15	—	±1.0	—	—	±1.0	—	±7.5	µA

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

6

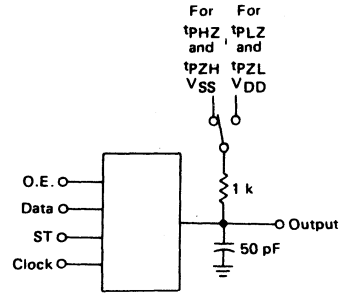
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Serial out QS	t_{PHL}					
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	–	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	–	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	–	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	–	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	–	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 127 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns	t_{PHZ},	5.0	–	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/pF) C_L + 57 ns	t_{PZL}	10	–	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	–	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns	t_{PLZ},	5.0	–	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns	t_{PZH}	10	–	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	–	70	140	
Setup Time	t_{su}					ns
Data in to Clock		5.0	125	60	–	
		10	55	30	–	
		15	35	20	–	
Hold Time	t_h	5.0	0	−40	—	ns
Clock to Data		10	20	−10	—	
		15	20	0	—	
Clock Pulse Width, High	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	83	40	–	
Clock Rise and Fall Time	$t_{r(cl)}$	5	—	–	15	μs
	$t_{f(cl)}$	10	—	–	5.0	
		15	—	–	4.0	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	5.0	2.5	
		15	–	6.0	3.0	
Strobe Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	70	35	–	

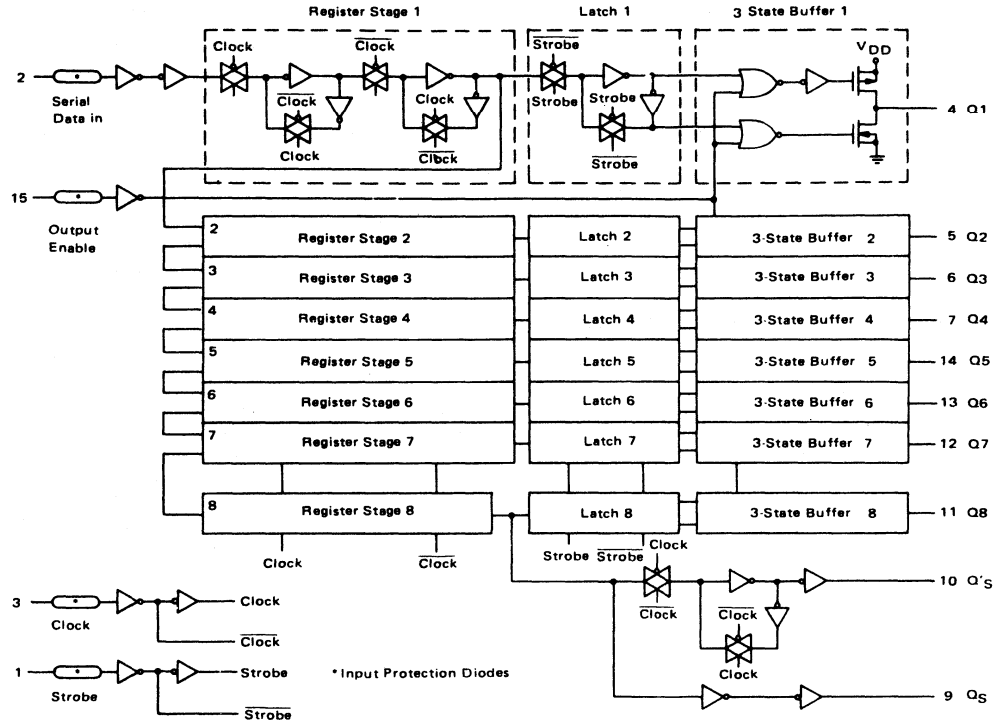
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

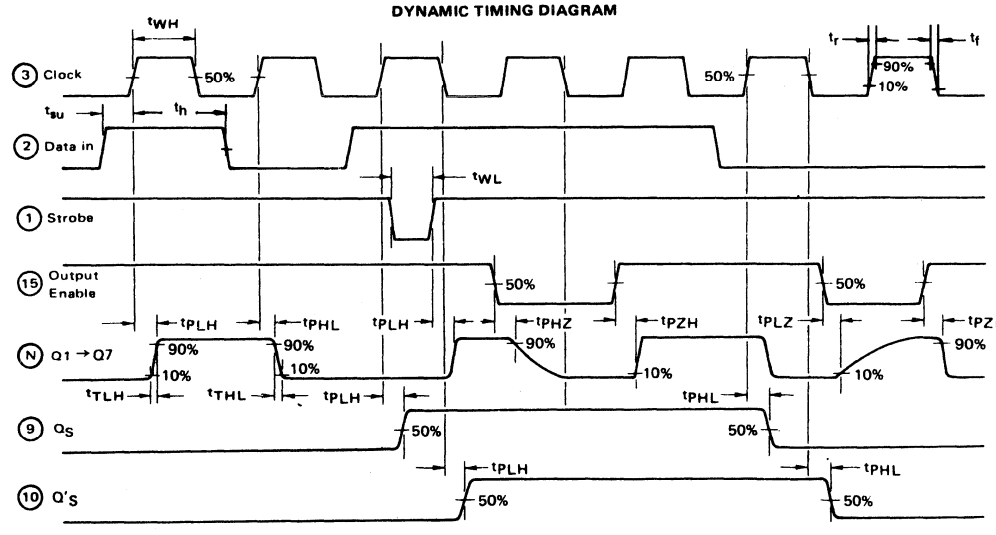
3-STATE TEST CIRCUIT



BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM



MOTOROLA

MC14097B

FOR COMPLETE DATA
SEE MC14067B

CMOS
(LOW-POWER COMPLEMENTARY MOS)

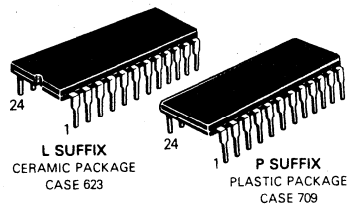
ANALOG MULTIPLEXER/
DEMULTIPLEXER

ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14097 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches.

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4097B



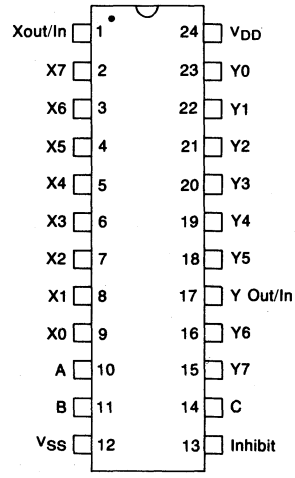
ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

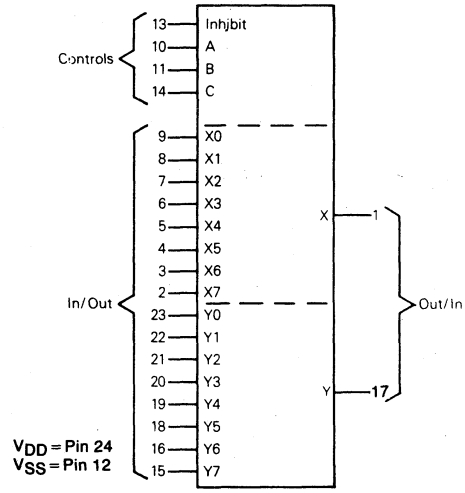
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT

MC14097B



MC14097B
Dual 8-Channel Analog Multiplexer/Demultiplexer



6

MOTOROLA

MC14099B
MC14599B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/$\overline{\text{Read}}$ line controls this port in the MC14599B.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

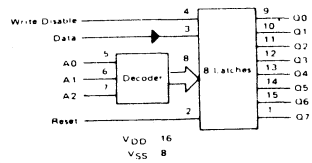
- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

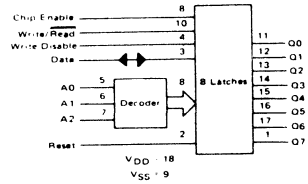
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

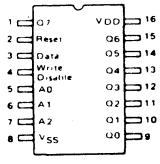
MC14099B



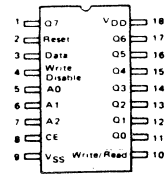
MC14599B



PIN ASSIGNMENT



PIN ASSIGNMENT

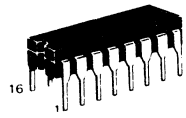


CMOS MSI

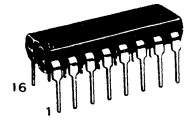
(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

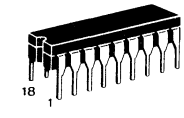
MC14599B WITH BIDIRECTIONAL PORT



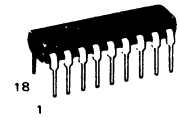
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Input Capacitance MC14599B – Data (pin 3) (V_{in} = 0)	C_{in}	–	–	–	–	15.0	22.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.0 μA/kHz) f + I_{DD}							
		15	I_T = (4.5 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

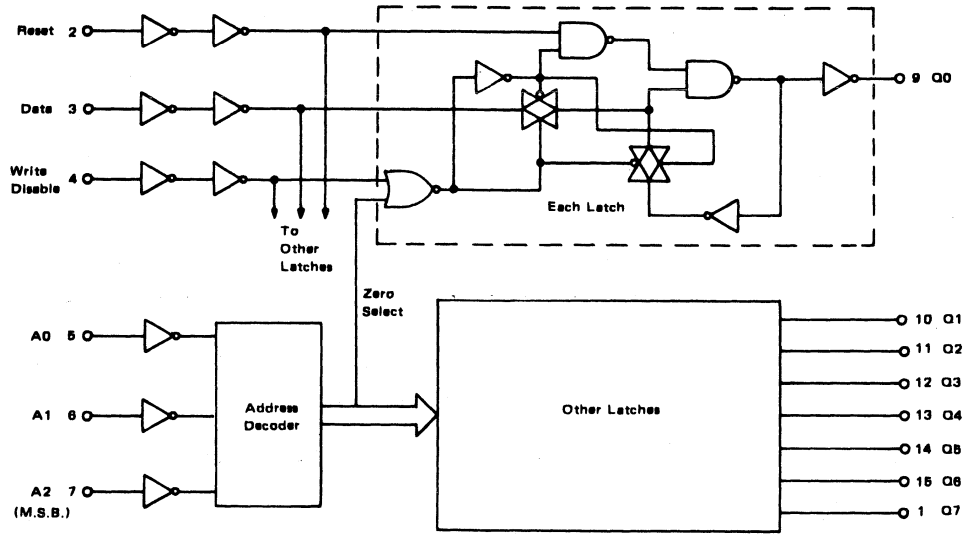
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L +32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L +20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L +20 ns		15	–	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					ns
Data to Output Q		5.0	–	200	400	
		10	–	75	150	
		15	–	50	100	
Write Disable to Output Q		5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Reset to Output Q		5.0	–	175	350	ns
		10	–	80	160	
		15	–	65	130	
CE to Output Q (MC14599B only)		5.0	–	225	450	ns
		10	-	100	200	
		15	–	75	150	
Propagation Delay Time, MC14599B only	t_{PHL}, t_{PLH}					ns
Chip Enable, Write/$\overline{\text{Read}}$ to Data		5.0	–	200	400	
		10	–	80	160	
		15	–	65	130	
Address to Data		5.0	–	200	400	ns
		10	–	90	180	
		15	–	75	150	
Pulse Widths	$t_{w(H)}$					ns
Reset	$t_{w(L)}$	5.0	150	75	–	
		10	75	40	–	
		15	50	25	–	
Write Disable		5.0	320	160	–	ns
		10	160	80	–	
		15	120	60	–	
Set Up Time	t_{su}					ns
Data to Write Disable		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
Hold Time	t_h					ns
Write Disable to Data		5.0	150	75	–	
		10	75	40	–	
		15	50	25	–	
Set Up Time	t_{su}	5.0	100	45	–	ns
Address to Write Disable		10	80	30	–	
		15	40	10	–	
Removal Time	t_{rem}	5.0	0	−80	–	ns
Write Disable to Address		10	0	−40	–	
		15	0	−40	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

MC14099B
FUNCTION DIAGRAM



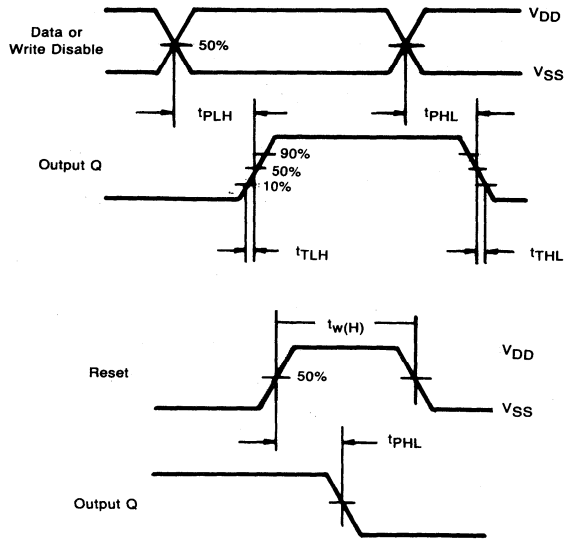
TRUTH TABLE

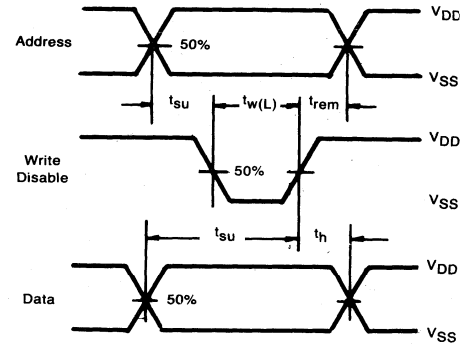
Write Disable	Reset	Addressed Latch	Unaddressed Latches
0	0	Data	Q_n*
0	1	Data	Reset†
1	0	Q_n*	Q_n*
1	1	Reset	Reset

* Q_n is previous state of latch.
† Reset to zero state.

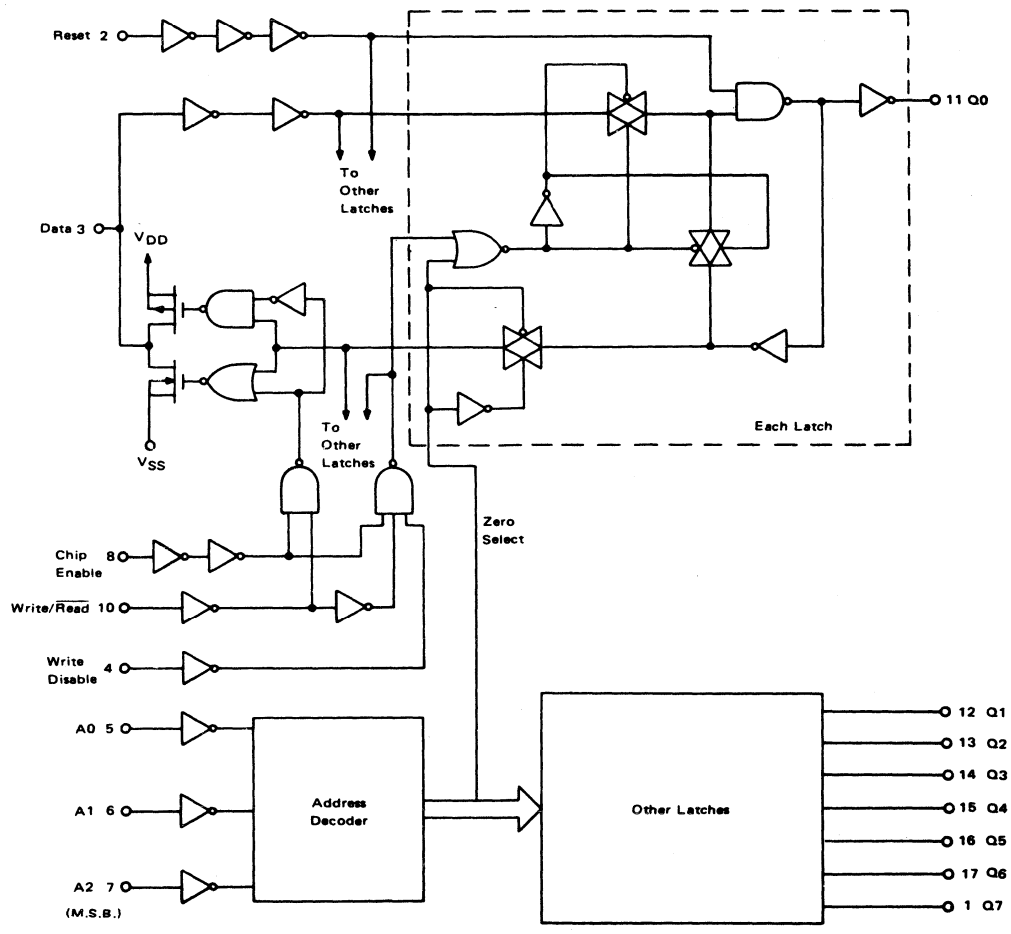
CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

SWITCHING WAVEFORMS





MC14599B
FUNCTION DIAGRAM



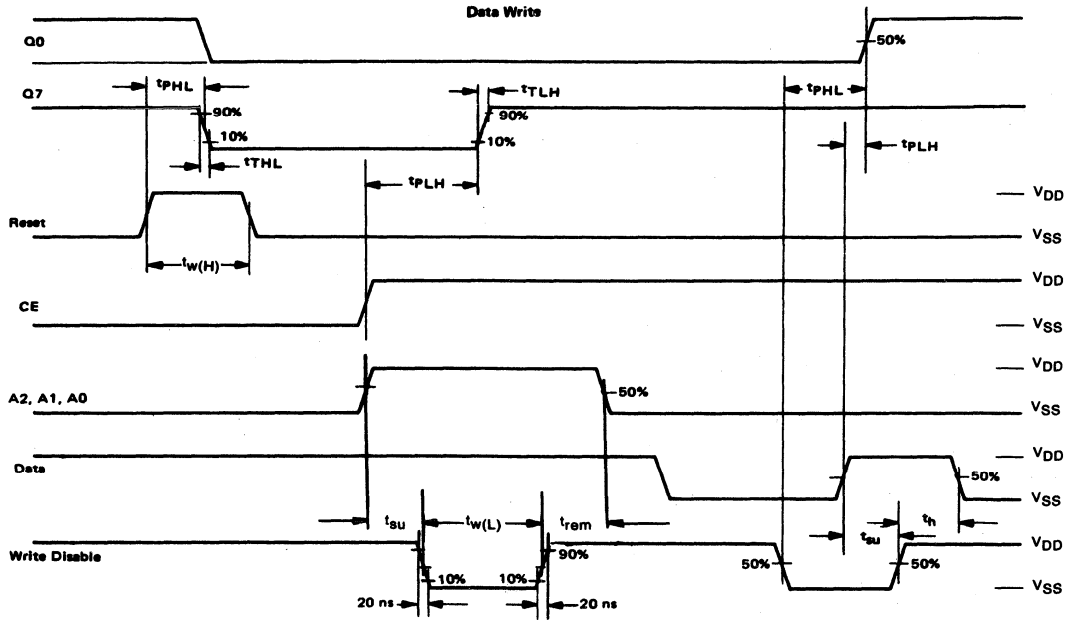
TRUTH TABLE

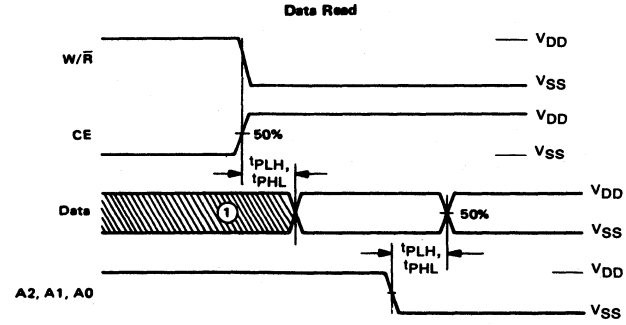
Chip Enable	Write/Read	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	•	•	Z
1	1	0	0	Data	•	Input
1	1	1	0	•	•	Z
1	0	X	0	•	•	Q_n
X	X	X	1	0	0	Z/0

X = Don't care.
• = No change in state of latch.
Z = High impedance.
Q_n = State of addressed latch.

CAUTION: To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

MC14599B
SWITCHING WAVEFORMS





NOTE: 1. Invalid Data Output
2. Reset in LOW State

MOTOROLA

MC14106B

Advance Information

CMOS SSI

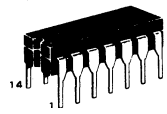
(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER

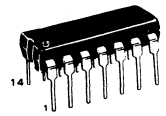
HEX SCHMITT TRIGGER

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage Over the MC14584B
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace the MC14584B or MC14069UB



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

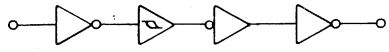
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

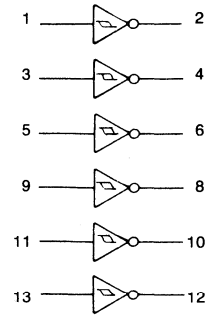
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in}=V_{DD}$	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in}=0$	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Hysteresis Voltage	V_H†	5.0	0.3	2.0	0.3	1.1	2.0	0.3	2.0	Vdc
		10	1.2	3.4	1.2	1.7	3.4	1.2	3.4	
		15	1.6	5.0	1.6	2.1	5.0	1.6	5.0	
Threshold Voltage Positive-Going	V_{T+}	5.0	2.2	3.6	2.2	2.9	3.6	2.2	3.6	Vdc
		10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
Negative-Going	V_{T-}	5.0	0.9	2.8	0.9	1.9	2.8	0.9	2.8	Vdc
		10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		15	4.0	7.4	4.0	5.8	7.4	4.0	7.4	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH}=2.5 Vdc) Source		5.0	−3.0	—	−2.4	−4.2	—	1.7	—	
(V_{OH}=4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	0.36	—	
(V_{OH}=9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	0.9	—	
(V_{OH}=13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	2.4	—	
(V_{OL}=0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL}=0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL}=1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH}=2.5 Vdc) Source		5.0	−2.5	—	−2.1	−4.2	—	−1.7	—	
(V_{OH}=4.6 Vdc)		5.0	−0.52	—	−0.44	−0.88	—	−0.36	—	
(V_{OH}=9.5 Vdc)		10	−1.3	—	−1.1	−2.25	—	−0.9	—	
(V_{OH}=13.5 Vdc)		15	−3.6	—	−3.0	−8.8	—	−2.4	—	
(V_{OL}=0.4 Vdc) Sink	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
(V_{OL}=0.5 Vdc)		10	1.3	—	1.1	2.25	—	0.9	—	
(V_{OL}=1.5 Vdc)		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±0.1	µAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±0.1	µAdc
Input Capacitance (V_{in}=0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
		10	—	0.50	—	0.0010	0.50	—	15	
		15	—	1.00	—	0.0015	1.00	—	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	—	1.0	—	0.0005	1.0	—	7.5	µAdc
		10	—	2.0	—	0.0010	2.0	—	15	
		15	—	4.0	—	0.0015	4.0	—	34	
Total Supply Current**† (Dynamic Plus Quiescent, Per Package) (C_L=50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T=(1.8\ \mu A/kHz)\ f+I_{DD}$							µAdc
		10	$I_T=(3.6\ \mu A/kHz)\ f+I_{DD}$							
		15	$I_T=(5.4\ \mu A/kHz)\ f+I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = $(V_{DD}-V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

†$V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+max} - V_{T-min}$).

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

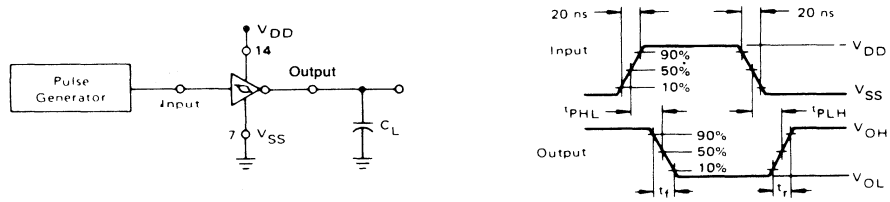
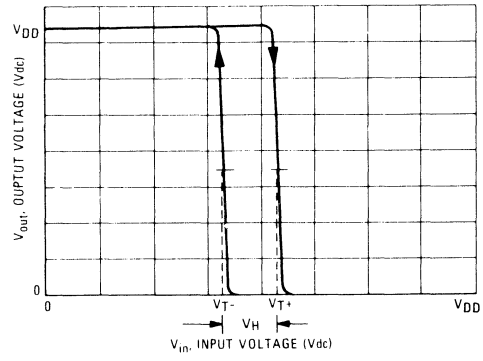
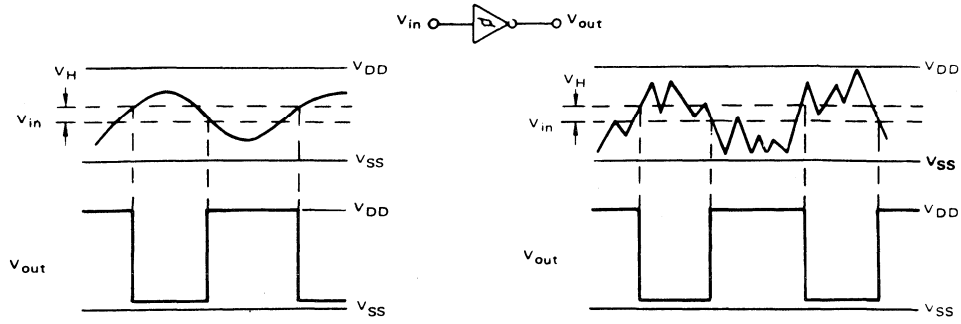


FIGURE 2 — TYPICAL TRANSFER CHARACTERISTICS



APPLICATIONS

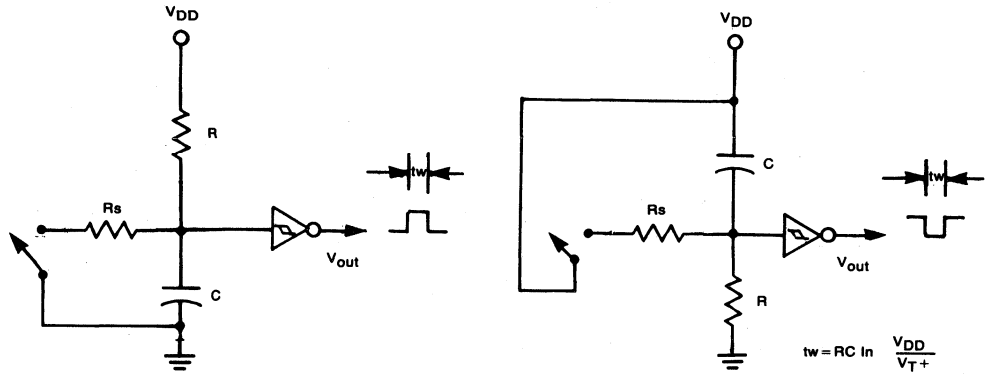


(a) Schmitt Triggers will square up inputs with slow rise and fall times.

(b) A Schmitt trigger offers maximum noise immunity in gate applications.

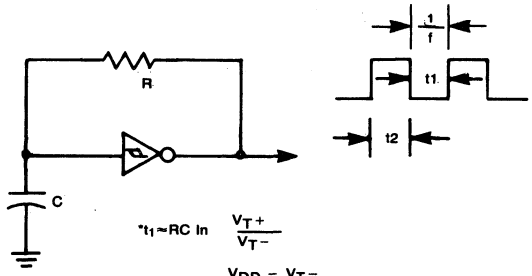
FIGURE 3

FIGURE 4 — MONOSTABLE MULTIVIBRATOR



Useful as Pushbutton/Keyboard Debounce Circuit.

FIGURE 5 — ASTABLE MULTIVIBRATOR



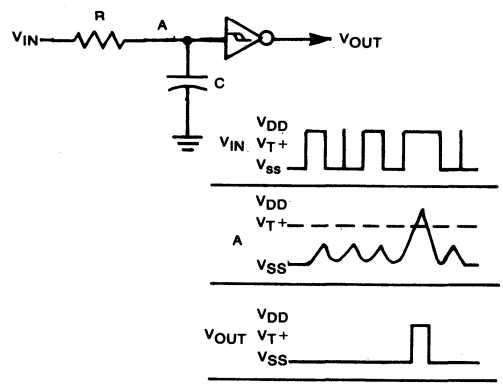
$*t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$

$*t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$

$\frac{1}{f} \approx RC \ln \left[\left(\frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}} \right) \left(\frac{V_{T+}}{V_{T-}} \right) \right]$

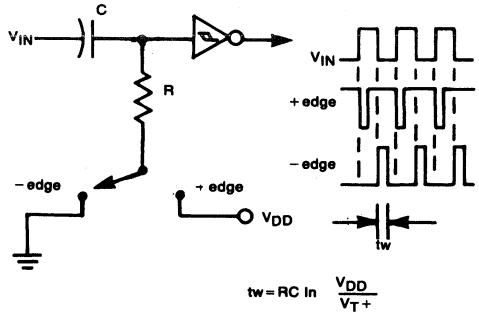
$*t_1 + t_2 >> t_{PHL} + t_{PLH}$

FIGURE 6 — INTEGRATOR



Useful in discriminating against short pulse durations.

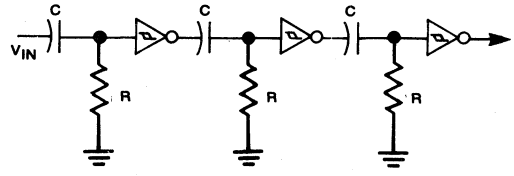
FIGURE 7 — DIFFERENTIATOR



$tw = RC \ln \frac{V_{DD}}{V_{T+}}$

Useful as an edge detector circuit.

FIGURE 8 — POSITIVE EDGE TIME DELAY CIRCUIT



MOTOROLA

MC14160B
BCD COUNTER
with Asynchronous Clear

MC14161B
4-BIT BINARY COUNTER
with Asynchronous Clear

MC14162B
BCD COUNTER
with Synchronous Clear

MC14163B
4-BIT BINARY COUNTER
with Synchronous Clear

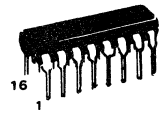
CMOS MSI

SYNCHRONOUS PRESETTABLE 4-BIT COUNTERS

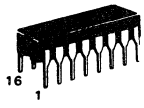
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable BCD counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B). The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

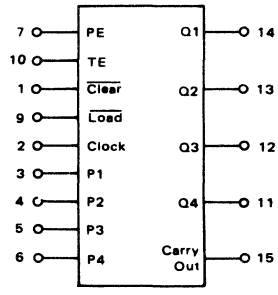
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.56 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.1 µA/kHz) f + I_{DD}							
		15	I_T = (1.9 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

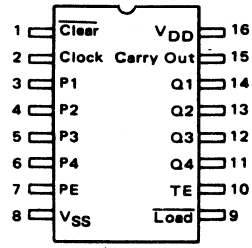
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
		5.0	—	100	200	
		10	—	50	100	
		15	—	40	80	
Output Fall Time	t_{THL}					ns
		5.0	—	100	200	
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	—	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	—	100	200	
Clock to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 395 ns		5.0	—	440	880	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 167 ns		10	—	185	370	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 112 ns		15	—	125	250	
TE to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 225 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 77 ns		15	—	90	180	
$\overline{\text{Clear}}$ to Q (MC14106B, MC14161B only)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 110 ns		5.0	—	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 37 ns		10	—	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 22 ns		15	—	100	200	
Setup Times						
Data to Clock	t_{su}	5.0	320	160	—	ns
		10	130	65	—	
		15	90	45	—	
$\overline{\text{Load}}$ to Clock		5.0	600	300	—	
		10	260	130	—	
		15	180	90	—	
Enable to Clock (PE or TE)		5.0	420	210	—	
		10	170	85	—	
		15	120	60	—	
$\overline{\text{Clear}}$ to Clock (MC14162B, MC14163B only)		5.0	310	155	—	
		10	110	55	—	
		15	70	35	—	
Hold Times						
Clock to Data	t_h	5.0	25	−15	—	ns
		10	15	−20	—	
		15	30	−15	—	
Clock to $\overline{\text{Load}}$		5.0	−40	−195	—	
		10	−10	−80	—	
		15	−5	−50	—	
Clock to PE		5.0	−40	−175	—	
		10	−10	−70	—	
		15	0	−40	—	
Clock to TE		5.0	−150	−280	—	
		10	−30	−130	—	
		15	−20	−80	—	
Clock to $\overline{\text{Clear}}$ (MC14162B, MC14163B only)		5.0	80	40	—	
		10	30	15	—	
		15	−10	−70	—	
$\overline{\text{Clear}}$ Removal Time (MC14160B, MC14161B only)	t_{rem}	5.0	90	30	—	ns
		10	65	20	—	
		15	55	20	—	

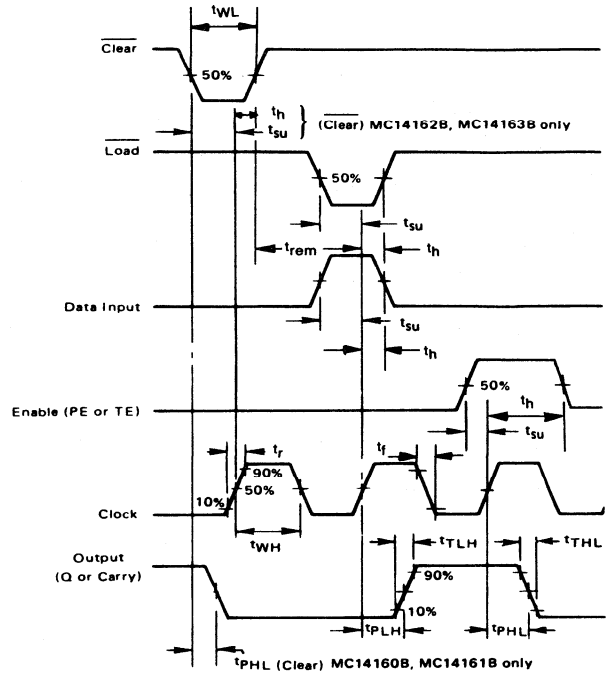
SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$) (Continued)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
$\overline{\text{Clear}}$ Pulse Width, Low (MC14160B, MC14161B only)	t_{WL}	5.0	200	100	—	ns
		10	90	45	—	
		15	60	30	—	
$\overline{\text{Clear}}$ Pulse Width, High	t_{WH}	5.0	250	125	—	ns
		10	100	50	—	
		15	70	35	—	
Clock Rise and Fall Time	t_r, t_f	5	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Clock Pulse Frequency	f_{cl}	5.0	—	2.0	1.0	MHz
		10	—	5.0	2.5	
		15	—	8.0	4.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

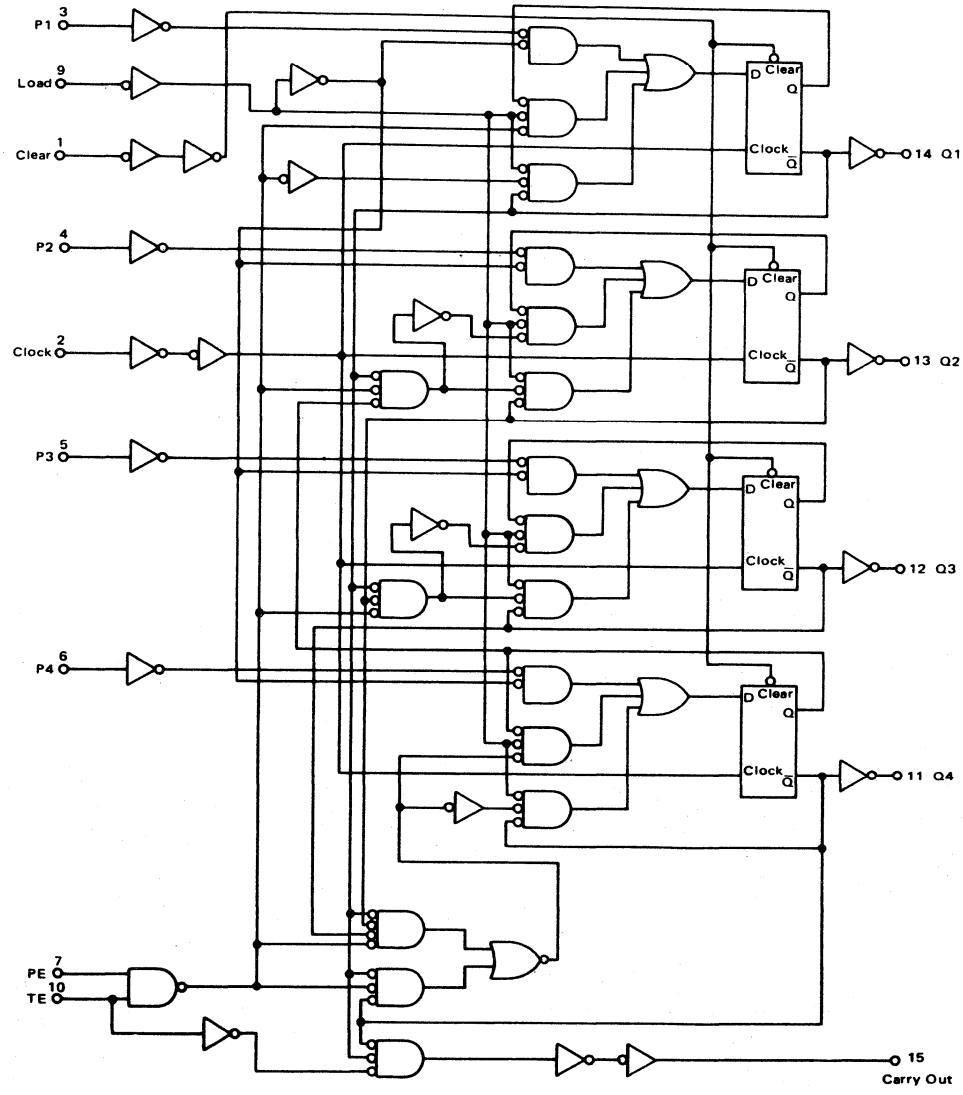


FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be acomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

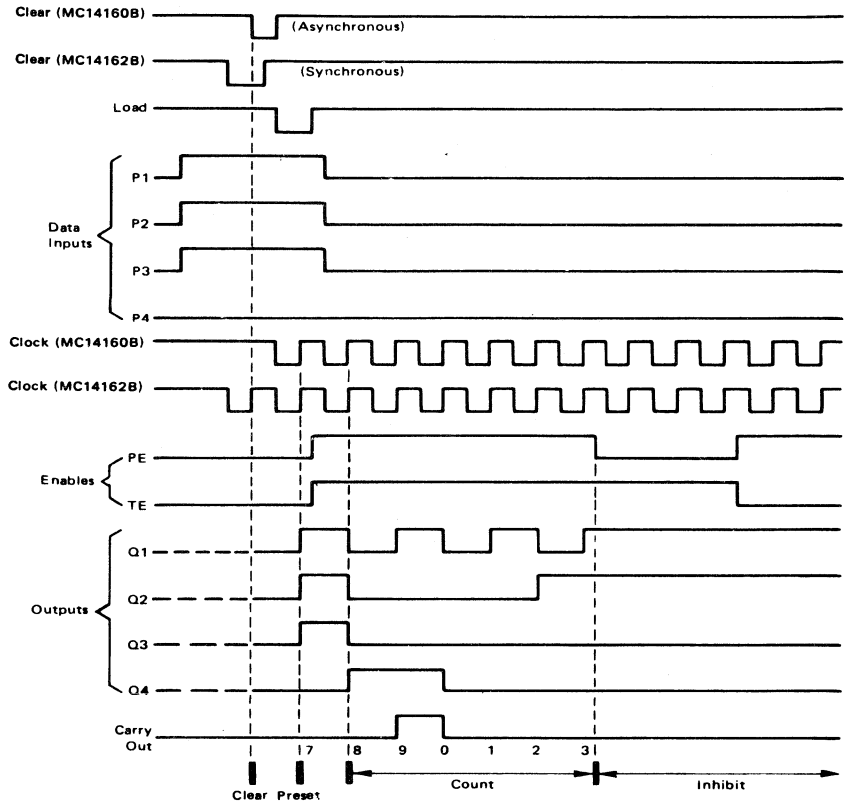
MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)



MC14160B, MC14162B TIMING DIAGRAM

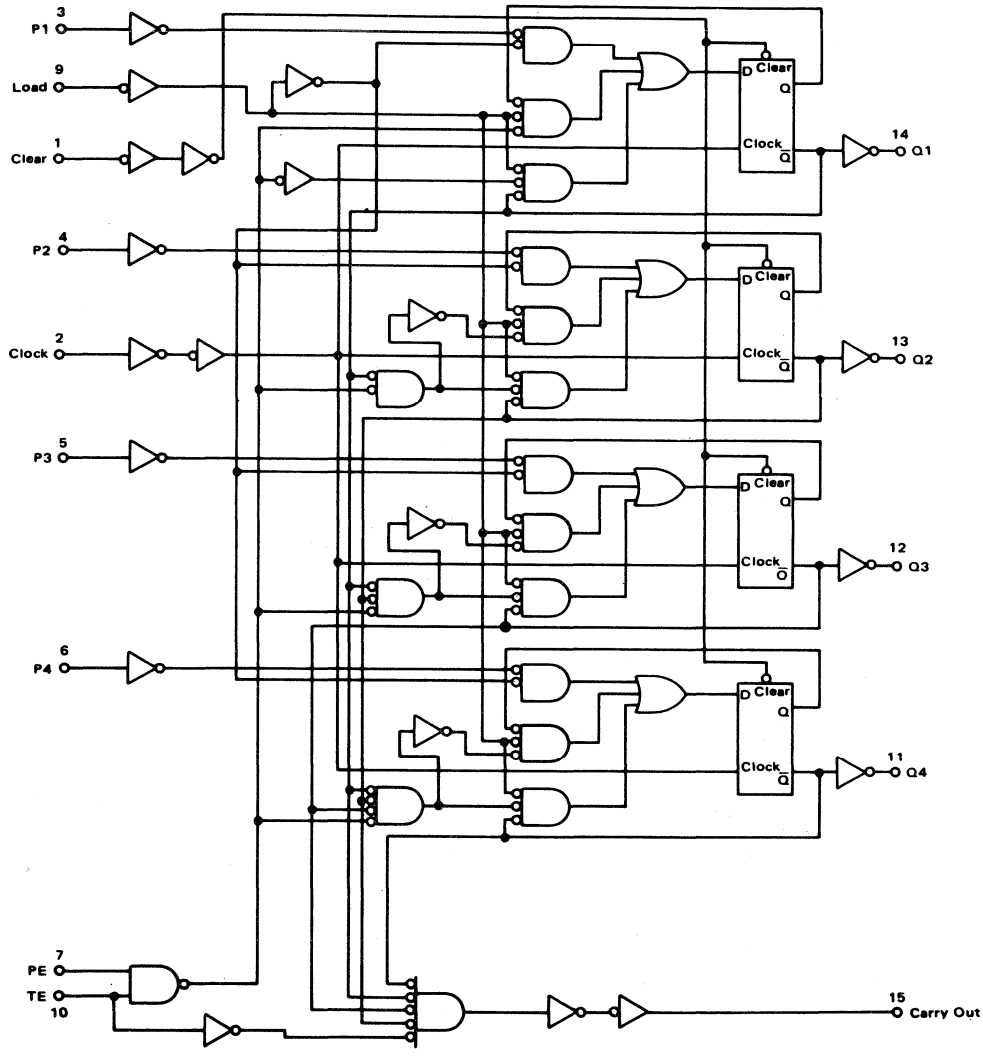
Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



6

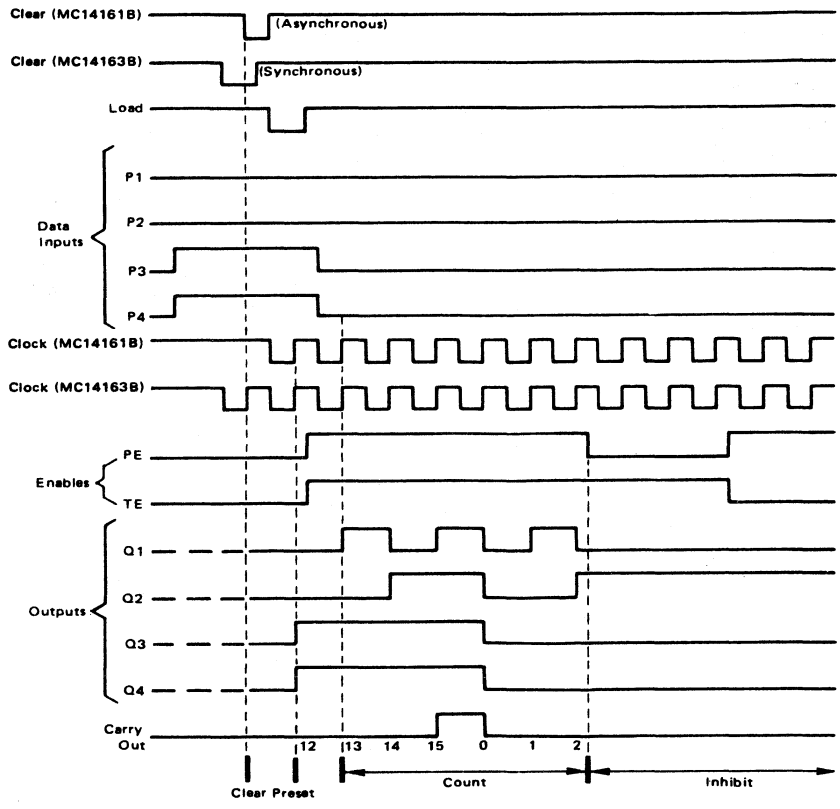
MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



MC14161B, MC14163B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit



6

MOTOROLA

MC14174B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP

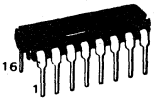
HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- Functional Equivalent to TTL 74174



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

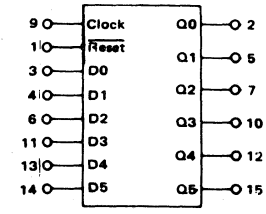
TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUT	
Clock	Data	$\overline{\text{Reset}}$	Q	
⌐⌐	0	1	0	
⌐⌐	1	1	1	
⌐¬	X	1	Q	No Change
X	X	0	0	

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.1 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.3 μA/kHz) f + I_{DD}							
		15	I_T = (3.7 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.003.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

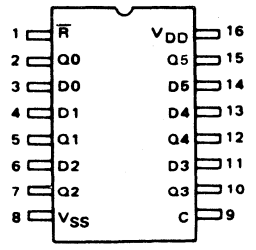
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time — Clock to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns	t_{PHL}	5.0	–	210	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	–	85	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	–	65	120	
Propagation Delay Time — $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	–	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock Pulse Width	t_{WH}	5.0	150	75	–	ns
		10	90	45	–	
		15	70	35	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	7.0	2.0	MHz
		10	–	12.0	5.0	
		15	–	15.5	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Data Setup Time	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	0	–	
Data Hold Time	t_h	5.0	80	40	–	ns
		10	40	20	–	
		15	30	15	–	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

*The formulas given are for the typical characteristics only at 25°C.

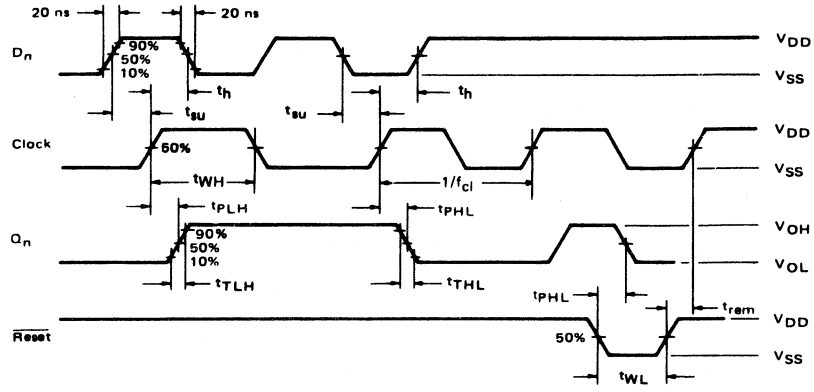
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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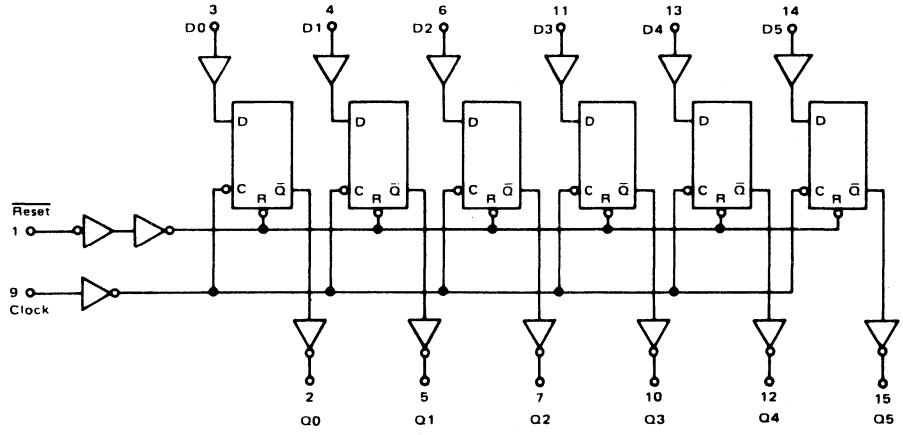
PIN ASSIGNMENT



TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



6

MOTOROLA

MC14175B

CMOS SSI

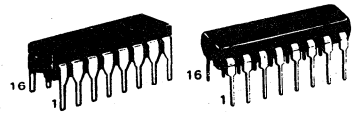
(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input ($\overline{R}$) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Compatible with Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

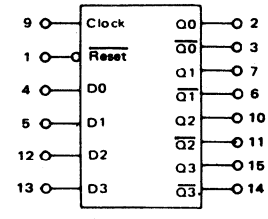
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUTS			OUTPUTS		
Clock	Data	$\overline{Reset}$	Q	$\overline{Q}$	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.4 μA/kHz) f + I_{DD}							
		15	I_T = (5.0 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

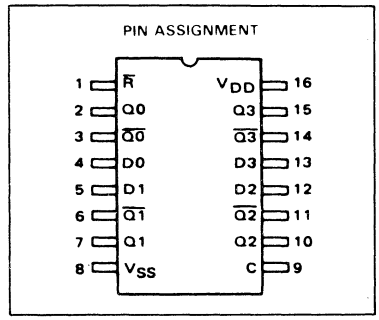
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

PIN ASSIGNMENT



6

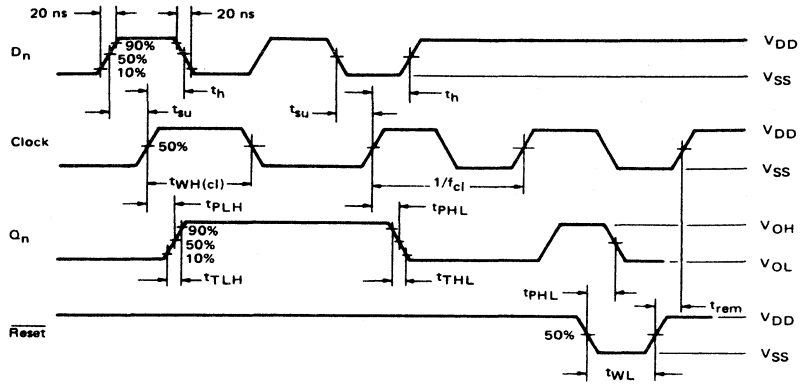
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time — Clock to Q, $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns		5.0	–	220	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns		10	–	90	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns		15	–	70	120	
Propagation Delay Time — Reset to Q, $\overline{Q}$	t_{PHL}, t_{PLH}					ns
t_{PHL} = (0.9 ns/pF) C_L + 280 ns		5.0	–	325	500	
t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	200	
t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	150	
Clock Pulse Width	t_{WH}	5.0	250	110	–	ns
		10	100	45	–	
		15	75	35	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	60	30	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.5	2.0	MHz
		10	–	11	5.0	
		15	–	14	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Data Setup Time	t_{su}	5.0	120	60	–	ns
		10	50	25	–	
		15	40	20	–	
Data Hold Time	t_h	5.0	80	40	–	ns
		10	40	20	–	
		15	30	15	–	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

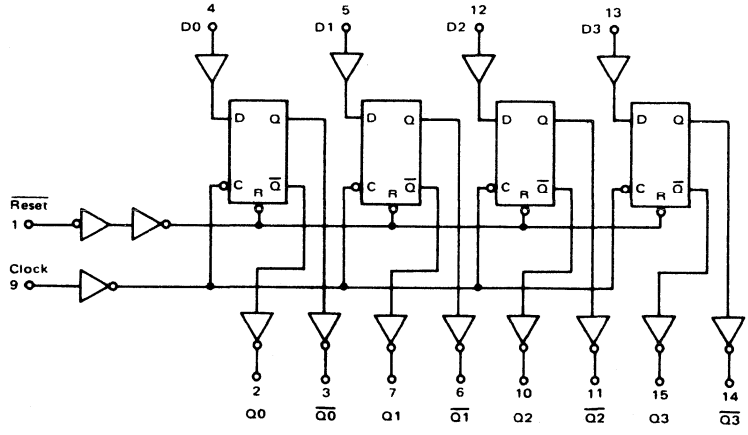
*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



6

MOTOROLA

MC14194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

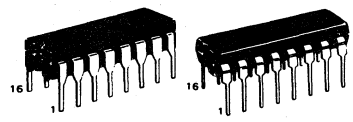
The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of LS194

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

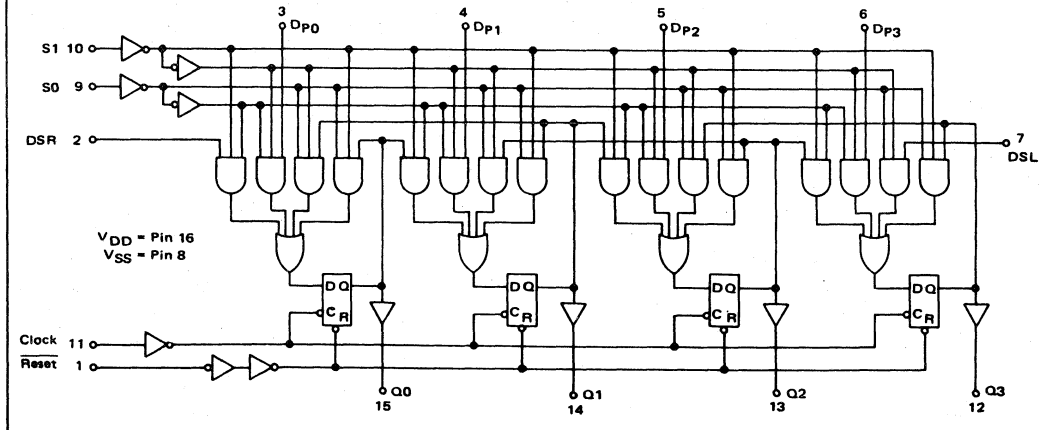
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	12.0	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.95 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.9 μA/kHz) f + I_{DD}							
		15	I_T = (2.9 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

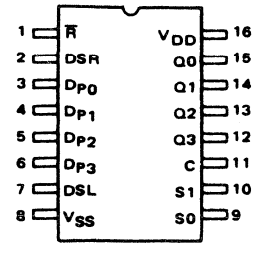
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{Reset}$ = 1)					OUTPUTS (@ t_{n+1})			
	S1	S0	DSR	DSL	D_{P0-3}	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care

t_{n+1} = State after the next positive-going transition of the clock.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

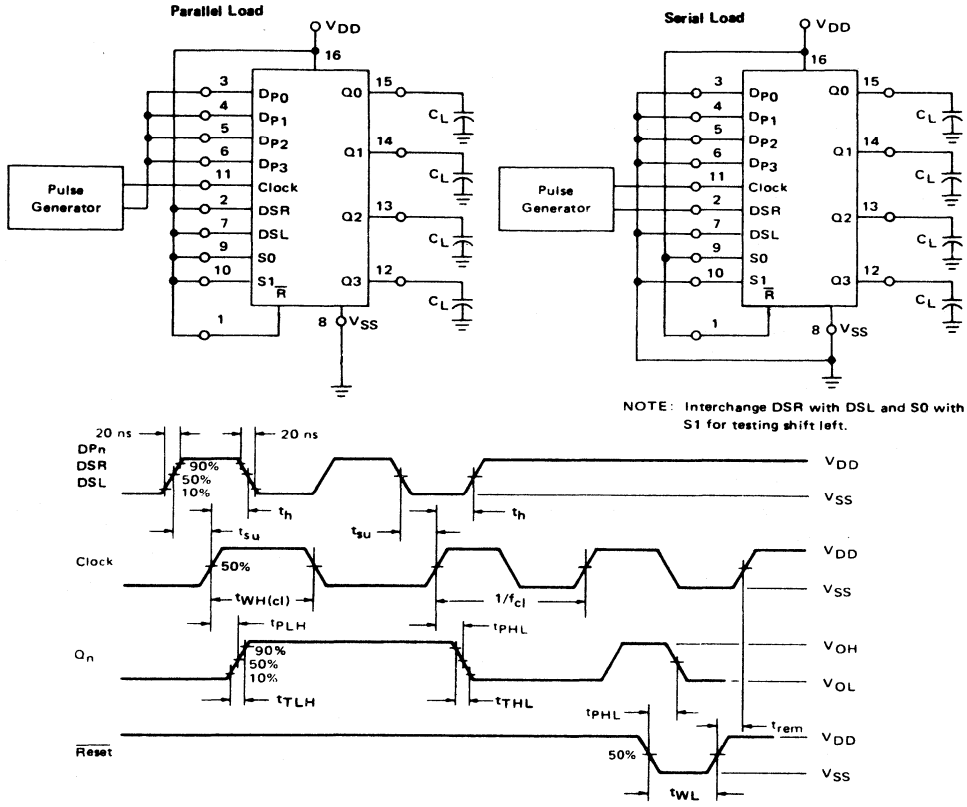
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
Clock to Q						
t_{PLH},t_{PHL} = (0.9 ns/pF) C_L + 230 ns		5.0	–	275	550	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 92 ns		10	–	110	220	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
$\overline{Reset}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PHL} = (0.36 ns/pF) C_L + 122 ns		10	–	140	280	
t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	110	220	
Clock Pulse Width	t_{WH}	5.0	280	140	–	ns
		10	110	55	–	
		15	85	40	–	
$\overline{Reset}$ Pulse Width	t_{WH}	5.0	180	90	–	ns
		10	70	35	–	
		15	50	26	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
(Shift Right or Left Mode)		10	–	9.0	4.5	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Setup Time	t_{su}					ns
Data to Clock		5.0	10	-8.0	–	
		10	20	0	–	
		15	40	9.0	–	
Mode Control (S) to Clock		5.0	200	100	–	ns
		10	75	36	–	
		15	55	27	–	
Hold Time	t_h					ns
Data to Clock		5.0	180	90	–	
		10	50	25	–	
		15	35	10	–	
Mode Control (S) to Clock		5.0	0	-40	–	ns
		10	0	-27	–	
		15	0	-20	–	
$\overline{Reset}$ Removal Time	t_{rem}	5.0	300	150	–	ns
		10	110	55	–	
		15	80	40	–	

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



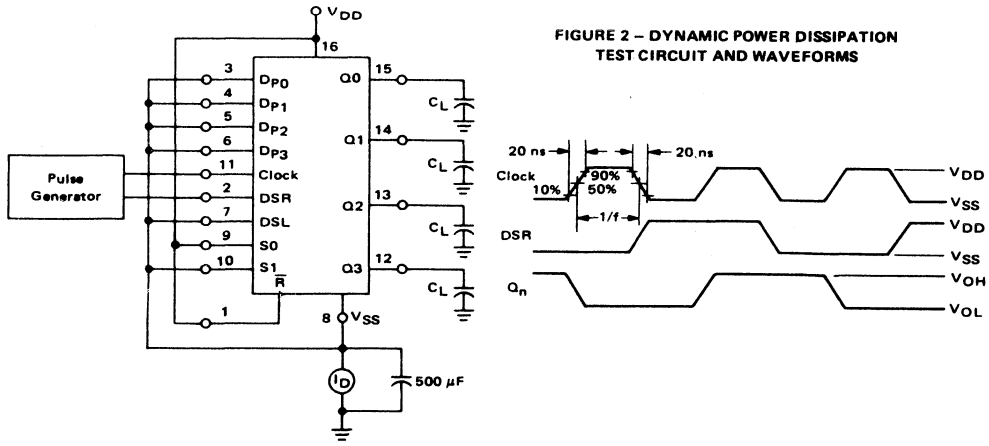


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

MOTOROLA

MC14415

QUAD PRECISION TIMER/DRIVER

The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

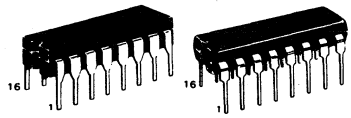
The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
  3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
  3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage - MC14415EFL/FL/FP MC14415EVL/VL/VP	−0.5 to +18.0 −0.5 to +6.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	±20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

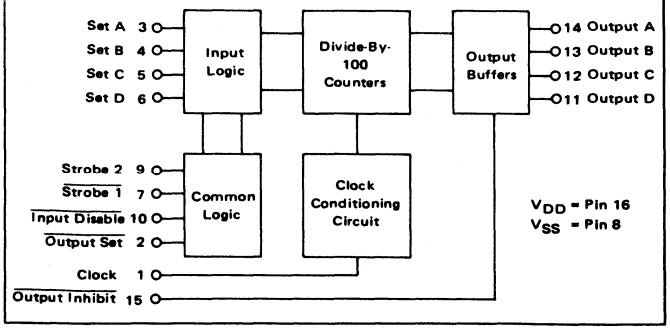
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

ORDERING INFORMATION

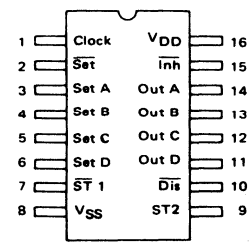
Operating Range: −55°C to +125°C
MC14415EFL (3 to 18 V, Ceramic Package)
MC14415EVL (3 to 6 V, Ceramic Package)

Operating Range: −40°C to +85°C
MC14415FL (3 to 18 V, Ceramic Package)
MC14415FP (3 to 18 V, Plastic Package)
MC14415VL (3 to 6 V, Ceramic Package)
MC14415VP (3 to 6 V, Plastic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level (No Load)	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	–	–	–	–	
"1" Level	V_{OH}	5.0	–	–	3.0	4.14	–	–	–	Vdc
		10	–	–	8.0	9.09	–	–	–	
		15	–	–	–	14.12	–	–	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq$ 1.5 Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq$ 3.0 Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq$ 4.5 Vdc)		15	–	–	–	6.75	–	–	–	
($\Delta V_{out} \leq$ 1.5 Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq$ 3.0 Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq$ 4.5 Vdc)		15	–	–	–	6.75	–	–	–	
Output Drive Voltage (NPN Driver)	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	–	–	3.0	4.14	–	–	–	
(I_{OH} = 5.0 mA)			–	–	2.7	3.44	–	–	–	
(I_{OH} = 10 mA			–	–	2.5	3.30	–	–	–	
(I_{OH} = 15 mA)			–	–	2.2	3.08	–	–	–	
(I_{OH} = 0 mA)		10	–	–	8.0	9.09	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	7.7	8.45	–	–	–	
(I_{OH} = 10 mA)			–	–	7.5	8.30	–	–	–	
(I_{OH} = 15 mA)			–	–	7.1	8.14	–	–	–	
(I_{OH} = 0 mA)		15	–	–	–	14.12	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	13.81	–	–	–	
(I_{OH} = 10 mA)			–	–	–	13.70	–	–	–	
(I_{OH} = 15 mA)			–	–	–	13.61	–	–	–	
Output Drive Current	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	
Input Leakage Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
		5.0	–	0.25	–	0.00005	0.25	–	3.5	
		10	–	1.0	–	0.00022	1.0	–	14	
		15	–	–	–	0.00050	–	–	–	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)	P_D									mW
		5.0	$P_D = (56\ mW/MHz)\ f + P_Q$							
		10	$P_D = (225\ mW/MHz)\ f + P_Q$							
		15	$P_D = (510\ mW/MHz)\ f + P_Q$							

*T_{low} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP
T_{high} = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

**The formulas given are for the typical characteristics only.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (2.0 ns/pF) C_L + 10 ns		5.0	–	40	85	
t_{TLH} = (1.25 ns/pF) C_L + 6 ns		10	–	25	60	
t_{TLH} = (1.10 ns/pF) C_L + 3 ns		15	–	20	–	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	–	70	150	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	–	35	80	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	–	25	–	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (2.7 ns/pF) C_L + 560 ns		5.0	–	600	1200	
t_{PHL} = (1.2 ns/pF) C_L + 282 ns		10	–	300	600	
t_{PLH} = (0.91 ns/pF) C_L + 286 ns		15	–	150	–	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (2.4 ns/pF) C_L + 564 ns		5.0	–	600	1200	
t_{PHL} = (1.0 ns/pF) C_L + 285 ns		10	–	300	600	
t_{PHL} = (0.75 ns/pF) C_L + 289 ns		15	–	150	–	
Turn-On Delay Time (Inhibit to Output)	t_{PHL}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Turn-Off Delay Time (Inhibit to Output)	t_{PLH}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Input Pulse Coincidence (Figure 3)	PC_{min}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Pulse Width (Figure 1)	t_{WH}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Clock Frequency	f_{cl}					MHz
		5.0	–	0.7	–	
		10	–	1.0	–	
		15	–	1.5	–	
Clock Input Rise and Fall Times (Figure 1)	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

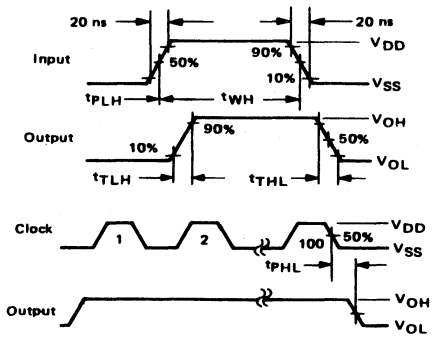
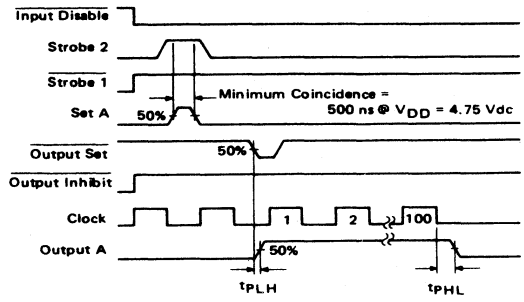
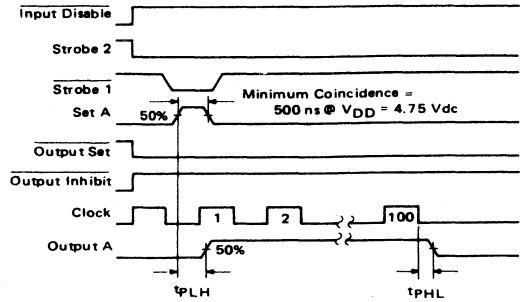


FIGURE 2 — TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

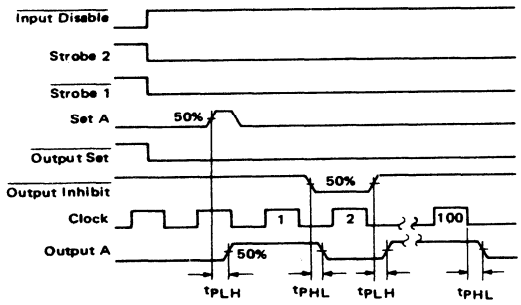
MODE 1 – $\overline{\text{OUTPUT SET}}$ INITIATES TIME DELAY



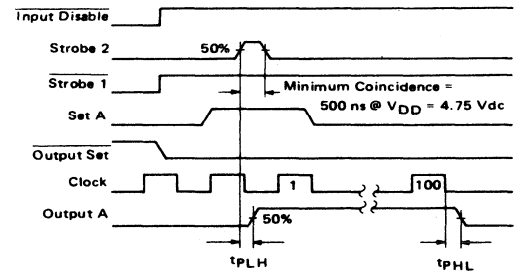
MODE 2 : SET A INITIATES TIME DELAY



MODE 3: $\overline{\text{OUTPUT INHIBIT}}$ DISABLES TIME DELAY

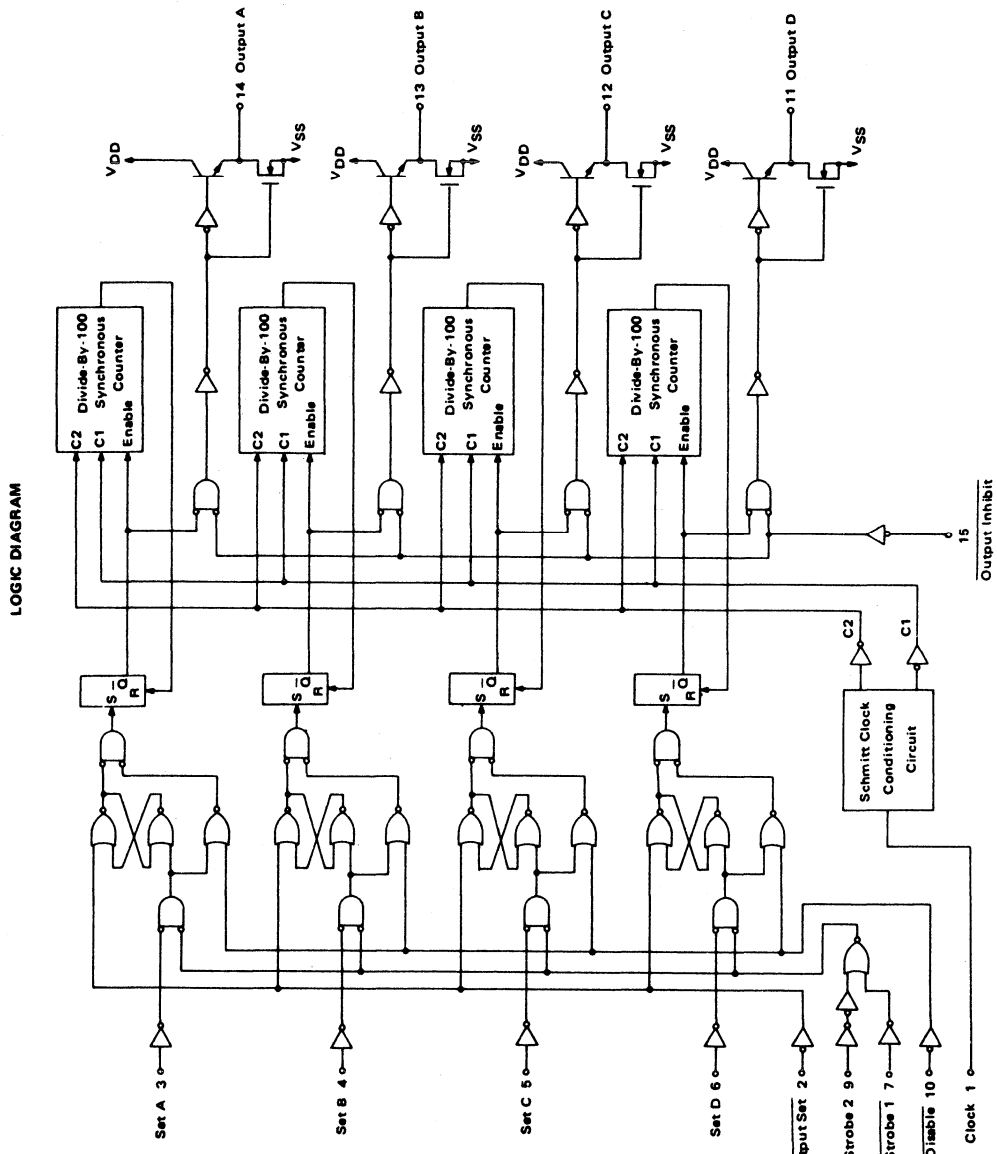


MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



6

LOGIC DIAGRAM



MOTOROLA

MC14460

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

AUTOMOTIVE SPEED CONTROL PROCESSOR

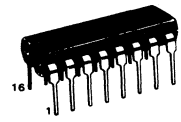
AUTOMOTIVE SPEED CONTROL PROCESSOR

The MC14460 device is designed to measure vehicle speed and provide pulse-width modulated outputs to trim a throttle positioning servo to maintain an internally stored reference speed.

The stored reference speed can be altered by the DECEL and ACCEL driver commands. The DECEL command trims down the speed, while ACCEL trims up the speed.

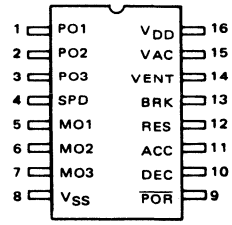
A BRAKE input is provided to turn off the outputs with a RESUME driver command to return the vehicle to the last stored speed.

- On-Chip Master Oscillator for System Time Reference
- Separate On-Chip Pulse Oscillator for Output Pulse Width Adjustment (Analogous to System Gain)
- Diode Protection on All Inputs
- Internal Redundant Brake and Minimum Speed Checks
- Acceleration Rates Controlled During ACCEL and RESUME Modes of Operation
- Low Frequency Speed Sensors Used
- No Throttle Position Feedback Required
- Power-On Reset
- Buffered Outputs Compatible with Discrete Transistor Driver Interface
- Low Power Dissipation
- Operating Temperature Range: −40° to +85°C

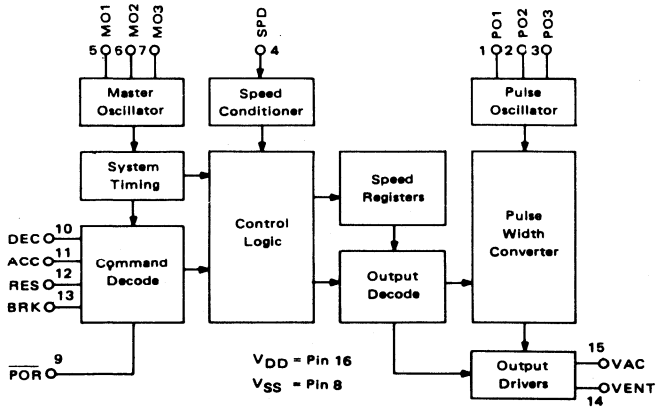


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: −12mW/°C from 65°C to 85°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = −40°C to +85°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Supply Voltage Pin 16	V_{DD}	–	4.0	5.0	6.0	Vdc
Output Voltage Pins 1, 2, 5, 6, 14, 15	V_{OL}	5.0	–	–	0.5	Vdc
	V_{OH}	5.0	4.5	–	–	Vdc
Input Voltage Pins 3, 7, 9, 10, 11, 12, 13	V_{IL}	–	–	–	0.3 V_{DD}	Vdc
	V_{IH}	–	0.7 V_{DD}	–	–	Vdc
Pin 4	V_{IL}	–	$\frac{V_{DD}}{2}$ −1.5	–	–	Vdc
	V_{IH}	–	–	–	$\frac{V_{DD}}{2}$ +1.5	Vdc
Input Hysteresis Pin 4 ($V_{IH} - V_{IL}$)	HYS	–	0.4	–	–	Vdc
Output Drive Current Pins 1, 2, 5, 6 V_{OH} = 4.6 Vdc	I_{OH}	5.0	-0.29	–	–	mAdc
V_{OL} = 0.4 Vdc	I_{OL}	5.0	+0.36	–	–	mAdc
Pins 14, 15 V_{OH} = 2.5 Vdc	I_{OH}	5.0	-2.0	–	–	mAdc
Input Current Pins 3, 4, 7, 10, 11, 12, 13 V_{IL} = 0.0 Vdc	I_{IL}	6.0	–	–	-1.0	μAdc
V_{OH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Pin 9 V_{IL} = 0.0 Vdc	I_{IL}	6.0	15	–	200	μAdc
V_{IH} = 6.0 Vdc	I_{IH}	6.0	–	–	+1.0	μAdc
Supply Current Pin 16 (Both Oscillators Active, VAC and VENT Outputs High)	I_{DD}	6.0	–	1.0	10	mAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SYSTEM TIMING

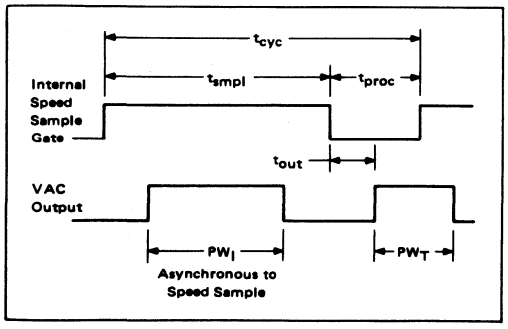
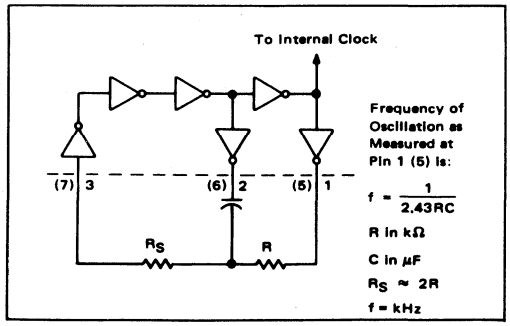


FIGURE 2 – OSCILLATORS



6

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{DD} = 4–6 Vdc)

Characteristics	Symbol	Min	Typ	Max	Unit
ACCEL Input Hold Time	t_{ACC}	$16/f_M$	9.52*	–	ms
DECEL Input Hold Time	t_{DEC}	$16/f_M$	9.52*	–	ms
RESUME Input Hold Time	t_{RES}	1	–	–	μs
BRAKE Input Hold Time	t_{BRK}	1	–	–	μs
Master Oscillator Frequency (Figure 2) T_A = -40°C to +85°C, R_S = 100 kΩ R = 43 kΩ, C = 5600 pF Useful Range	f_M	 1596 1344	 1680 1680	 1764 2016	 Hz Hz
Pulse Oscillator Frequency (Figure 2) T_A = -40°C to +85°C, R_S = 100 kΩ R = 43 kΩ, C = 5600 pF Useful Range	f_P	 1596 400	 1680 1600	 1764 3200	 Hz Hz
Speed Input Frequency	f_S	–	–	300	Hz
Speed Sample Time ($1008/f_M$)	t_{smpl}	–	600*	–	ms
Speed Processing Time ($16/f_M$)	t_{proc}	–	8.9*	–	ms
System Cycle Time ($1024/f_M$)	t_{cyc}	–	608.9*	–	ms
Output Delay Time ($9/f_M$)	t_{out}	–	5.4*	–	ms
Output Pulse Width Initializations (≈$1/f_P$) Trim Outputs (≈$1/f_P$)	 PW_I PW_T	 280* 10*	 – –	 760* 80*	 ms ms

*f_M = 1680 Hz, f_P = 1600 Hz, f_S = 2.222 Hz/MPH

SYSTEM PERFORMANCE (T_A = 25°C, V_{DD} = 5 Vdc, f_M = 1680 Hz, f_S = 2.222 Hz/MPH)

Characteristic	Symbol	Typical	Unit
Speed Resolution ($f_M/2016\ f_S$)	S_{RES}	0.375	MPH
Minimum Operating Speed ($f_M/31.5\ f_S$)	S_{min}	24	MPH
Maximum Stored Speed ($f_M/8.4\ f_S$)	S_{max}	90	MPH
Controlled Acceleration Rate (ACCEL or RESUME Modes) $(f_M)^2/f_S$ (6.881) (10^5)	A	1.85	MPH/s
Redundant Brake Speed Drop Below Stored Reference Speed ($-f_M/63\ f_S$)	S_{RB}	-12	MPH
Speed Deviation Assumes Suitable Mechanical Hookup and Pulse Oscillator Frequency Adjusted to Suit Throttle Servo Requirements Level Road (no wind, ±1% grades) Transient Road Conditions (±10 MPH winds, ±7% grades)	 ΔS_N ΔS_T	 ±2 ±3	 MPH MPH
Stored Speed Accuracy Steady-State (Acceleration = 0) Transient (Acceleration = ± A MPH/s)	 RS_{SS} RS_T	 0.375 0.6 A	 MPH MPH

TRUTH TABLE

OUTPUT		
VAC	VENT	SERVO DRIVE
0	0	Decrease Speed
0	1	Hold Speed
1	0	Invalid Output
1	1	Increase Speed

6

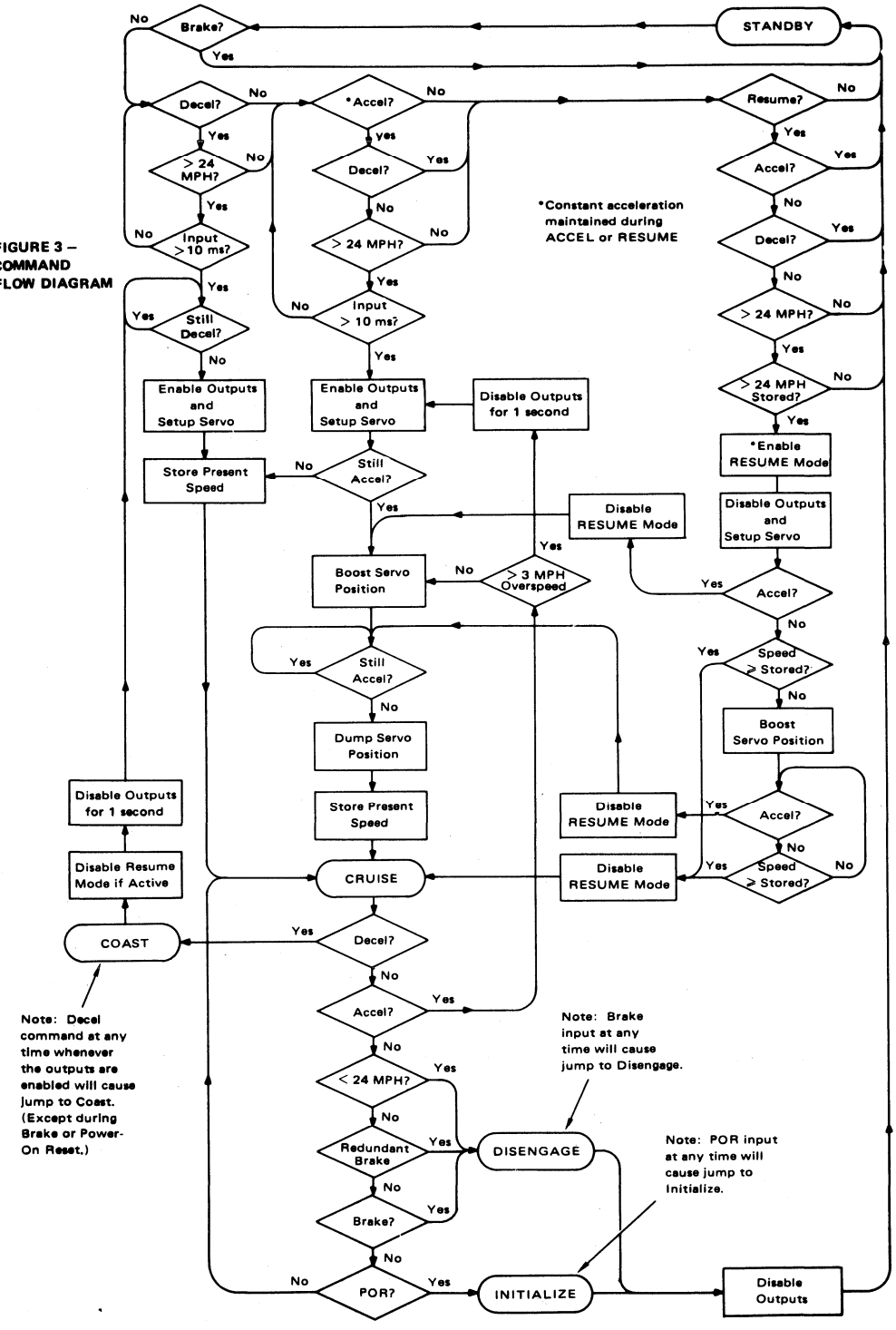


FIGURE 3 – COMMAND FLOW DIAGRAM

6

DEVICE OPERATION

PULSE OSCILLATOR (PO1, PO2, PO3; Pins 1, 2, 3)

These pins are the output pins of the output Pulse Oscillator, which is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the relative pulse width of the VAC and VENT outputs.

SPEED (SPD, Pin 4)

This is the Speed input to be controlled or stored. This input is level sensitive with hysteresis to allow use of slowly changing waveforms. Input frequency should never exceed 1/3 the Master Oscillator frequency (f_M).

MASTER OSCILLATOR (MO1, MO2, MO3; Pins 5, 6, 7)

The Master Oscillator is a three-terminal RC type. See Figure 2 for design parameters. This oscillator sets the master system timing.

POWER-ON RESET (POR, Pin 9)

This pin is the Power-On Reset input. As long as this input is LOW, the internal system is cleared and the VAC and VENT outputs are disabled. An internal pullup device will source 15–200 μAdc of current from this pin to allow capacitor charging for automatic power-on reset.

DECEL (DEC, Pin 10)

This is the DECEL command input. When held HIGH both VAC and VENT outputs will be LOW. When the DECEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

ACCEL (ACC, Pin 11)

This is the ACCEL command input. When held HIGH the VAC and VENT outputs will be modulated to maintain a fixed rate of acceleration. When the ACCEL input returns LOW the last sample of the SPD input will be stored as the reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

continued

THROTTLE SERVO

A. Two Coil Vacuum Powered

Truth Table:

VAC Coil	VENT Coil	Throttle Action
Off	Off	Release
Off	On	Hold
On	Off	Weak Pull
On	On	Pull

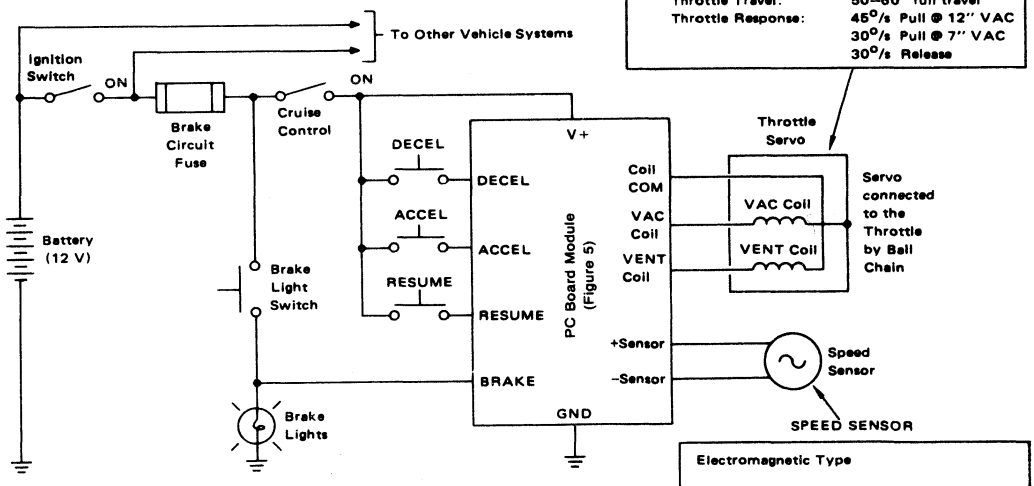
B. Coil Type

Coil Impedance: 80–90 Ω
Coil Inductance: 125–150 mH

C. Servo Response

Minimum Pulse Width: 5 ms
Throttle Travel: 50–60° full travel
Throttle Response: 45°/s Pull @ 12" VAC
30°/s Pull @ 7" VAC
30°/s Release

FIGURE 4 – TYPICAL AUTOMOTIVE CRUISE CONTROL APPLICATION



SPEED SENSOR

Electromagnetic Type

Poles: 8/revolution
Output Freq: 2.222 Hz/MPH (8000 pulses/mile)
Output Voltage: > 3.0 Vp-p @ 24 MPH
Maximum Freq: 360 Hz (162 MPH)
DC Resistance: < 40 Ω

DEVICE OPERATION continued

RESUME (RES, Pin 12)

This is the RESUME command input. When taken HIGH the system will lock into a mode where the VAC and VENT outputs are modulated to maintain a fixed rate acceleration. This acceleration ends when the SPD input sample matches the stored reference speed. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

BRAKE (BRK, Pin 13)

This is the BRAKE command input. When this input is taken HIGH the system is disabled (both VAC and VENT outputs LOW) until a DECEL, ACCEL, or RESUME command is received. The flow diagram in Figure 3 gives the detailed constraints/operation of this input.

VENT (Pin 14)

This is the VENT output. See Truth Table for operation.

VAC (Pin 15)

This is the VAC output. See Truth Table for operation.

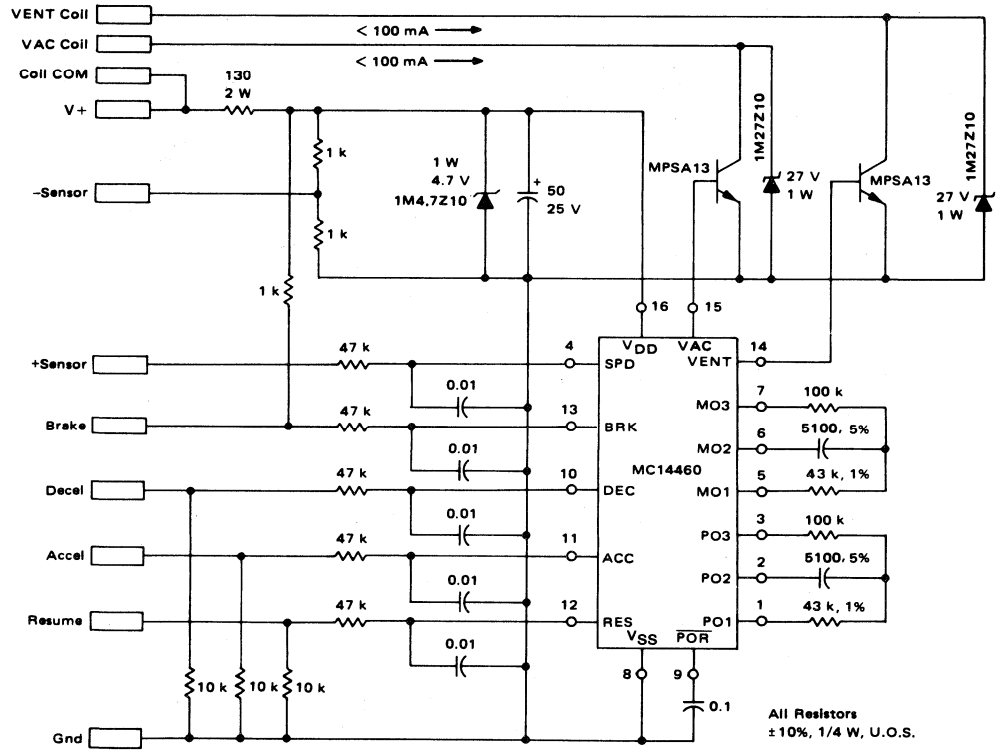
GROUND (V_{SS}, Pin 8)

Pin 8 is the ground connection for the package.

POSITIVE POWER SUPPLY (V_{DD}, Pin 16)

Pin 16 is the power supply connection for the package.

FIGURE 5 – PC BOARD MODULE FOR CRUISE CONTROL



Environment

Ambient Temperature (T_A)	-40°C to 85°C
V+ Operating Range	11–15 Vdc
V+ Transients	9–16 Vdc
Load Dump	80 V Peak decaying to 12 V in < 200 ms
Inductive	±300 V Peak decaying in < 1 ms
Jump Start	+24 Vdc for 5 min.
Reverse Battery	-12 Vdc continuous

6

MOTOROLA

MC14490

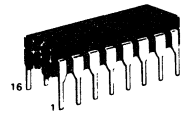
HEX CONTACT BOUNCE ELIMINATOR

The MC14490 is constructed with complementary MOS enhancement mode devices, and is used for the elimination of extraneous level changes that result when interfacing with mechanical contacts. The digital contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input has stabilized. The bounce eliminator circuit will remove bounce on both the "make" and the "break" of a contact closure. The clock for operation of the MC14490 is derived from an internal R-C oscillator which requires only an external capacitor to adjust for the desired operating frequency (bounce delay). The clock may also be driven from an external clock source or the oscillator of another MC14490 (see Figure 5).

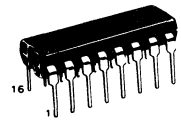
- Diode Protection on All Inputs
- Six Debouncers Per Package
- Internal Pullups on All Data Inputs
- Can Be Used as a Digital Integrator, System Synchronizer, or Delay Line
- Internal Oscillator (R-C), or External Clock Source
- TTL Compatible Data Inputs/Outputs
- Single Line Input, Debounces Both "Make" and "Break" Contacts
- Does Not Require "Form C" (Single Pole Double Throw) Input Signal
- Cascadable for Longer Time Delays
- Schmitt Trigger on Clock Input (Pin 7)
- Supply Voltage Range = 3.0 V to 18 V
- Chip Complexity: 546 FETs or 136.5 Equivalent Gates

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

HEX CONTACT BOUNCE ELIMINATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



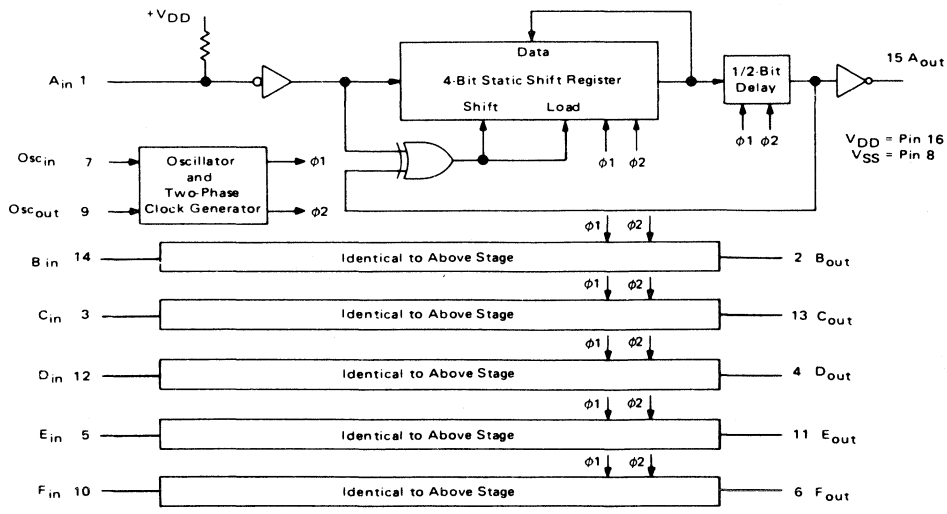
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

CERAMIC PACKAGE: MC14490L
(−55°C to +125°C)

PLASTIC PACKAGE: MC14490P
(−40°C to 85°C)

BLOCK DIAGRAM



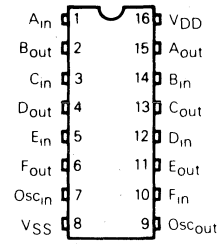
6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mA
Source										
Oscillator Output										
(V_{OH} = 2.5 V)		5.0	−0.6	–	−0.5	−1.5	–	−0.4	–	
(V_{OH} = 4.6 V)		5.0	−0.12	–	−0.1	−0.3	–	−0.08	–	
(V_{OH} = 9.5 V)		10	−0.23	–	−0.20	−0.8	–	−0.16	–	
(V_{OH} = 13.5 V)		15	−1.4	–	−1.2	−3.0	–	−1.0	–	
Debounce Outputs										
(V_{OH} = 2.5 V)		5.0	−0.9	–	−0.75	−2.2	–	−0.6	–	
(V_{OH} = 4.6 V)		5.0	−0.19	–	−0.16	−0.46	–	−0.12	–	
(V_{OH} = 9.5 V)		10	−0.60	–	−0.50	−1.2	–	−0.4	–	
(V_{OH} = 13.5 V)		15	−1.8	–	−1.5	−4.5	–	−1.2	–	
Sink	I_{OL}									mA
Oscillator Output										
(V_{OL} = 0.4 V)		5.0	0.36	–	0.30	0.9	–	0.24	–	
(V_{OL} = 0.5 V)		10	0.9	–	0.75	2.3	–	0.6	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.5	10	–	2.8	–	
Debounce Outputs										
(V_{OL} = 0.4 V)		5.0	2.6	–	2.2	4.0	–	1.8	–	
(V_{OL} = 0.5 V)		10	4.0	–	3.3	9	–	2.7	–	
(V_{OL} = 1.5 V)		15	12	–	10	35	–	8.1	–	
Input Current										
Debounce Inputs (V_{in} = V_{DD})	I_{IH}	15	–	2	–	0.2	2	–	11	μA
Input Current Oscillator – Pin 7 (V_{in} = V_{SS} or V_{DD})	I_{in}	15	–	±620	–	±255	±400	–	±250	μA
Pullup Resistor Source Current	I_{IL}	5.0	210	375	140	190	255	70	130	μA
Debounce Inputs		10	415	740	280	380	500	145	265	
(V_{in} = V_{SS})		15	610	1100	415	570	750	215	400	
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{SS}	5.0	–	150	–	40	100	–	90	μA
(V_{in} = V_{SS} or V_{DD}, I_{out} = 0 μA)		10	–	280	–	90	225	–	180	
		15	–	840	–	225	650	–	550	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time All Outputs	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time Oscillator Output	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Debounce Outputs	t_{THL}	5.0 10 15	– – –	60 30 20	120 60 40	
Propagation Delay Time Oscillator Input to Debounce Outputs	t_{PHL}	5.0 10 15	– – –	285 120 95	570 240 190	ns
	t_{PLH}	5.0 10 15	– – –	370 160 120	740 320 240	
Clock Frequency (50% Duty Cycle) (External Clock)	f_{cl}	5.0 10 15	– – –	2.8 6 9	1.4 3.0 4.5	MHz
Setup Time (See Figure 1)	t_{su}	5.0 10 15	100 80 60	50 40 30	– – –	ns
Maximum External Clock Input Rise and Fall Time Oscillator Input	t_r, t_f	5.0 10 15	No Limit			ns
Oscillator Frequency OSC_{out} $C_{ext} \geq 100$ pF* **Note: These equations are intended to be a design guide. Laboratory experimentation may be required. Formulas are typically ± 15% of actual frequencies.**	f_{osc}, typ	5.0 10 15	$\frac{1.5}{C_{ext}\ (\text{in } \mu F)}$ $\frac{4.5}{C_{ext}\ (\text{in } \mu F)}$ $\frac{6.5}{C_{ext}\ (\text{in } \mu F)}$			Hz

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

***POWER-DOWN CONSIDERATIONS**

Large values of C_{ext} may cause problems when powering down the MC14490 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge through the input protection diodes at Pin 7 or the parasitic diodes at Pin 9. Current through these internal diodes must be limited to 10 mA; therefore the turn-off time of the power supply must not be faster than $t = (V_{DD} - V_{SS}) \cdot C_{ext}/(10\ mA)$. For example, if $V_{DD} - V_{SS} = 15$ V and $C_{ext} = 1\ \mu F$, the power supply must turn off no faster than $t = (15\ V) \cdot (1\ \mu F)/10\ mA = 1.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of the power supply to zero volts occurs, the MC14490 may sustain damage. To avoid this possibility, use external clamping diodes, D1 and D2, connected as shown in Figure 2.

FIGURE 1 — SWITCHING WAVEFORMS

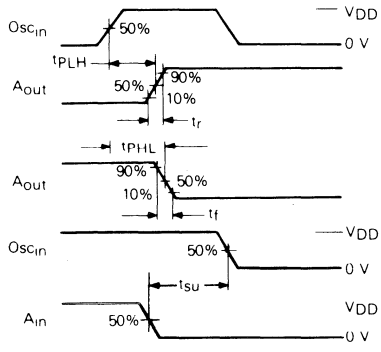
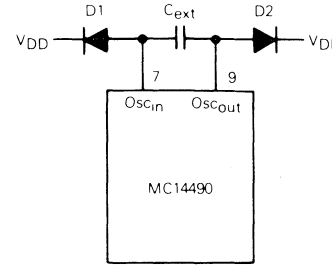


FIGURE 2 — DISCHARGE PROTECTION DURING POWER DOWN



6

THEORY OF OPERATION

The MC14490 Hex Contact Bounce Eliminator is basically a digital integrator. The circuit can integrate both up and down. This enables the circuit to eliminate bounce on both the leading and trailing edges of the signal, shown in the timing diagram of Figure 3.

Each of the six Bounce Eliminators is composed of a 4½-bit register (the integrator) and logic to compare the input with the contents of the shift register, as shown in Figure 4. The shift register requires a series of timing pulses in order to shift the input signal into each shift register location. These timing pulses (the clock signal) are represented in the upper waveform of Figure 3. Each of the six Bounce Eliminator circuits has an internal resistor as shown in Figure 4. A pullup resistor was incorporated rather than a pulldown resistor in order to implement switched ground input signals, such as those coming from relay contacts and push buttons. By switching ground, rather than a power supply lead, system faults (such as shorts to ground on the signal input leads) will not cause excessive currents in the wiring and contacts. Signal lead shorts to ground are much more probable than shorts to a power supply lead.

When the relay contact is open, (see Figure 4) the high level is inverted, and the shift register is loaded with a low on each negative edge of the clock signal. To understand the operation, we assume all bits of the shift register are loaded with lows and the output is at a high level.

At clock edge 1 (Figure 3) the input has gone low and a high has been loaded into the first bit or storage location of the shift register. Just after the negative edge of clock 1, the input signal has bounced back to a high. This causes the shift register to be reset to lows in all four bits — thus starting the timing sequence over again.

During clock edges 3 to 6 the input signal has stayed low. Thus, a high has been shifted into all four shift register bits and, as shown, the output goes low during the positive edge of clock pulse 6.

It should be noted that there is a 3½ to 4½ clock period delay between the clean input signal and output signal. In this example there is a delay of 3.8 clock periods from the beginning of the clean input signal.

After some time period of N clock periods, the contact is opened and at N + 1 a low is loaded into the first bit. Just after N + 1, when the input bounces low, all bits are set to a high. At N + 2 nothing happens because the input and output are low and all bits of the shift register are high. At time N + 3 and thereafter the input signal is a high, clean signal. At the positive edge of N + 6 the output goes high as a result of four lows being shifted into the shift register.

Assuming the input signal is long enough to be clocked through the Bounce Eliminator, the output signal will be no longer or shorter than the clean input signal plus or minus one clock period.

The amount of time distortion between the input and output signals is a function of the difference in bounce characteristics on the edges of the input signal and the clock frequency. Since most relay contacts have more bounce when making as compared to breaking, the overall delay, counting bounce period, will be greater on the leading edge of the input signal than on the trailing edge. Thus, the output signal will be shorter than the input signal — if the leading edge bounce is included in the overall timing calculation.

The only requirement on the clock frequency in order to obtain a bounce free output signal is that four clock periods do not occur while the input signal is in a false state. Referring to Figure 3, a false state is seen to occur three times at the beginning of the input signal. The input signal goes low three times before it finally settles down to a valid low state. The first three low pulses are referred to as false states.

If the user has an available clock signal of the proper frequency, it may be used by connecting it to the oscillator input (pin 7). However, if an external clock is not available the user can place a small capacitor across the oscillator input and output pins in order to start up an internal clock source (as shown in Figure 4). The clock signal at the oscillator output pin may then be used to clock other MC14490 Bounce Eliminator packages. With the use of the MC14490, a large number of signals can be cleaned up, with the requirement of only one small capacitor external to the Hex Bounce Eliminator packages.

6

FIGURE 3 — TIMING DIAGRAM

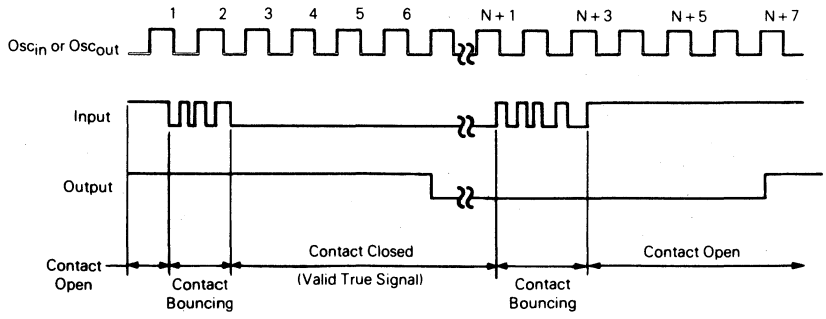
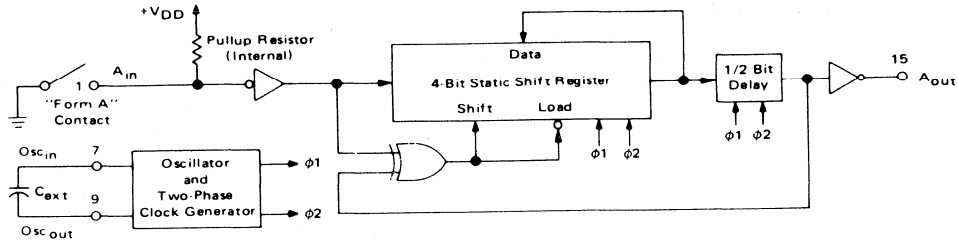


FIGURE 4 – TYPICAL "FORM A" CONTACT DEBOUNCE CIRCUIT
(Only One Debouncer Shown)



OPERATING CHARACTERISTICS

The single most important characteristic of the MC14490 is that it works with a single signal lead as an input, making it directly compatible with mechanical contacts (Form A and B).

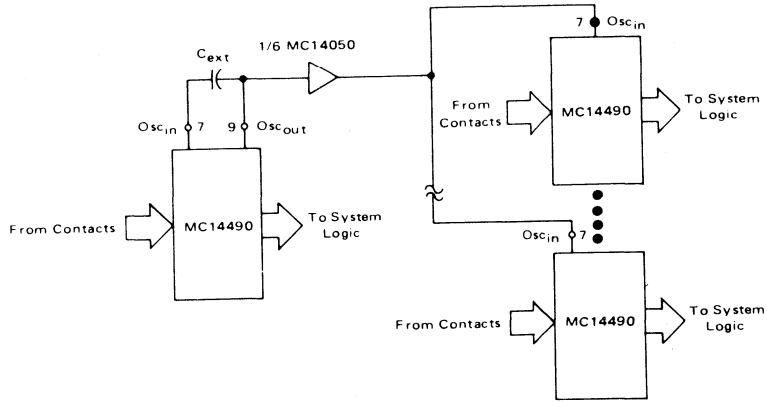
The circuit has a built in pullup resistor on each input. The worst case value of the pullup resistor (determined from the Electrical Characteristics table) is used to calculate the contact wetting current. If more contact current is required, an external resistor may be connected between V_{DD} and the input.

Because of the built-in pullup resistors, the inputs cannot be driven with a single standard CMOS gate when V_{DD} is below 5 V. At this voltage, the input should be driven with paralleled standard gates or by the MC14049 or MC14050 buffers.

The clock input circuit (pin 7) has Schmitt trigger shaping such that proper clocking will occur even with very slow clock edges, eliminating any need for clock preshaping. In addition, other MC14490 oscillator inputs can be driven from a single oscillator output buffered by an MC14050 (see Figure 5). Up to six MC14490s may be driven by a single buffer.

The MC14490 is TTL compatible on both the inputs and the outputs. When V_{DD} is at 4.5 V, the buffered outputs can sink 1.6 mA at 0.4 V. The inputs can be driven with TTL as a result of the internal input pullup resistors.

FIGURE 5 – TYPICAL SINGLE OSCILLATOR
DEBOUNCE SYSTEM

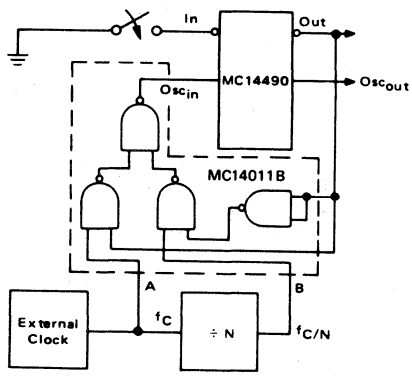


TYPICAL APPLICATIONS

ASYMMETRICAL TIMING

In applications where different leading and trailing edge delays are required (such as a fast attack/slow release timer.) Clocks of different frequencies can be gated into the MC14490 as shown in Figure 6. In order to produce a slow attack/fast release circuit leads A and B should be interchanged. The clock out lead can then be used to feed clock signals to the other MC14490 packages where the asymmetrical input/output timing is required.

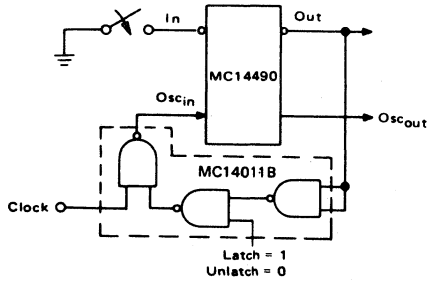
FIGURE 6 – FAST ATTACK/SLOW RELEASE CIRCUIT



LATCHED OUTPUT

The contents of the Bounce Eliminator can be latched by using several extra gates as shown in Figure 7. If the latch lead is high the clock will be stopped when the output goes low. This will hold the output low even though the input has returned to the high state. Any time the clock is stopped the outputs will be representative of the input signal four clock periods earlier.

FIGURE 7 – LATCHED OUTPUT CIRCUIT



MULTIPLE TIMING SIGNALS

As shown in Figure 8, the Bounce Eliminator circuits can be connected in series. In this configuration each output is delayed by four clock periods relative to its respective input. This configuration may be used to generate multiple timing signals such as a delay line, for programming other timing operations.

One application of the above is shown in Figure 9, where it is required to have a single pulse output for a single operation (make) of the push button or relay contact. This only requires the series connection of two Bounce Eliminator circuits, one inverter, and one NOR gate in order to generate the signal $\overline{A}B$ as shown in Figures 9 and 10. The signal $\overline{A}B$ is four clock periods in length. If the inverter is switched to the A output, the pulse $A\overline{B}$ will be generated upon release or break of the contact. With the use of a few additional parts many different pulses and waveshapes may be generated.

FIGURE 8 – MULTIPLE TIMING CIRCUIT CONNECTIONS

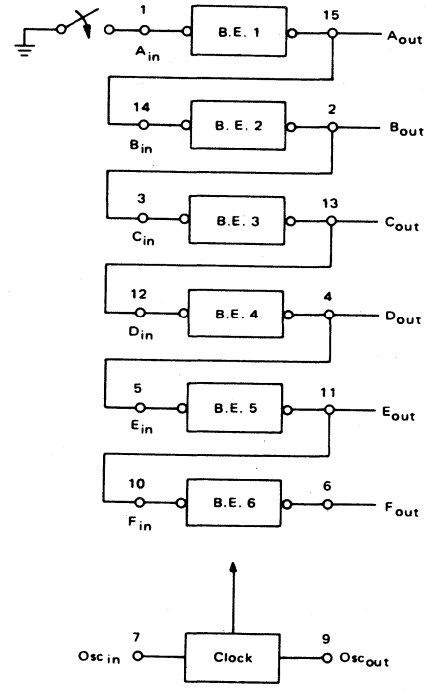


FIGURE 9 – SINGLE PULSE OUTPUT CIRCUIT

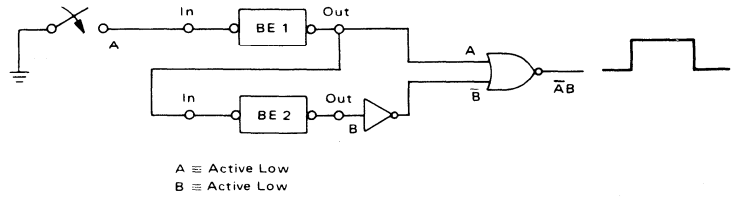
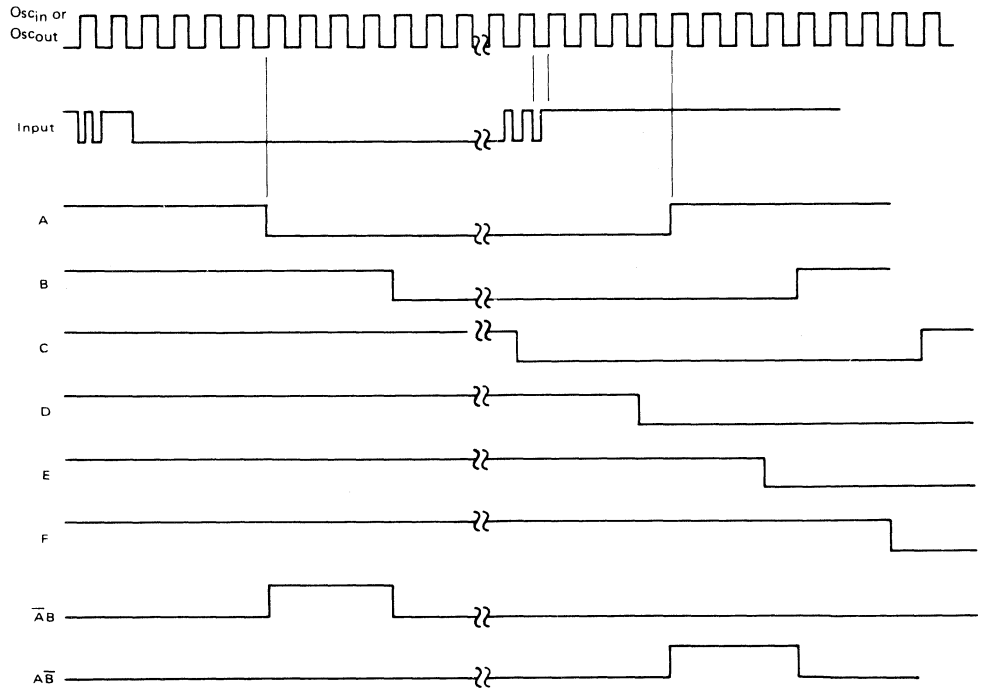


FIGURE 10 – MULTIPLE OUTPUT SIGNAL TIMING DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14500B

INDUSTRIAL CONTROL UNIT

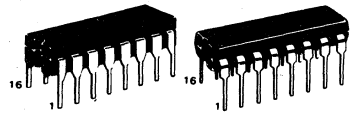
The MC14500B Industrial Control Unit (ICU) is a single-bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single-bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored-program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

- 16 Instructions
- DC to 1.0 MHz Operation at V_{DD} = 5 V
- On-Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 to 18 V Operation
- Low Quiescent Current Characteristic of CMOS Devices
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range
- Detailed Operation and Applications Given in Handbook HB-209
- Development System Described in Application Note AN-889

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

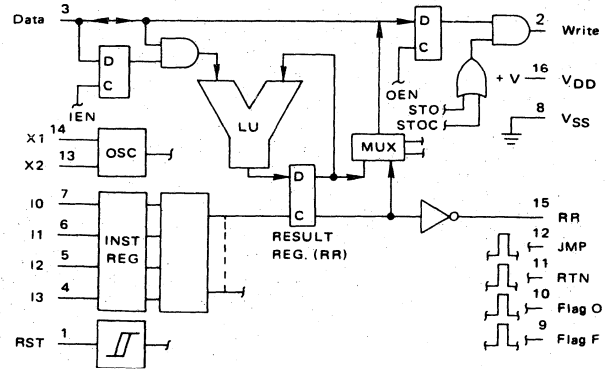
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

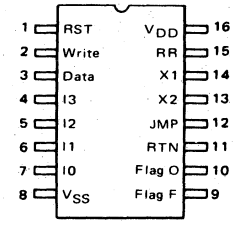
A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			V	Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage	"0" Level	V_{IL}									V
RST, D, X2											
(V_O = 4.5 or 0.5 V)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)			15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage #	"0" Level	V_{IL}									V
I0, I1, I2, I3											
(V_O = 4.5 or 0.5 V)			5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 V)			10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 V)			15	–	2.4	–	3.4	2.4	–	2.4	
	"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 V)			5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 V)			10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 V)			15	10	–	10	4.3	–	10	–	
Output Drive Current	Source	I_{OH}									mA
Data, Write (AL/CL/CP Device)											
(V_{OH} = 4.6 V)			5.0	1.2	–	−1.0	-2.0	–	−0.7	–	
(V_{OH} = 9.5 V)			10	−3.6	–	−3.0	-6.0	–	−2.1	–	
(V_{OH} = 13.5 V)			15	−7.2	–	−6.0	-12	–	−4.2	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	1.9	–	1.6	3.2	–	1.1	–	
(V_{OL} = 0.5 V)			10	3.6	–	3.0	6.0	–	2.1	–	
(V_{OL} = 1.5 V)			15	7.2	–	6.0	12	–	4.2	–	
Output Drive Current	Source	I_{OH}									mA
Other Outputs (AL Device)											
(V_{OH} = 2.5 V)			5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 V)			5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 V)			10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 V)			15	-4.2	–	-3.4	8.8	–	-2.4	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current	Source	I_{OH}									mA
Other Outputs (CL/CP Device)											
(V_{OH} = 2.5 V)			5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 V)			5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 V)			10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 V)			15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 V)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)			15	3.6	–	3.0	8.8	–	2.4	–	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

6

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} V	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current, RST (AL/CL/CP Device)	I_{in}	15	25	–	–	150	–	–	250	μA
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance (Data)	C_{in}	–	–	–	–	15	–	–	–	pF
Input Capacitance (All Other Inputs)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package) I_{out} = 0 μA, V_{in}=0 or V_{DD}	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
Quiescent Current (CL/CP Device) (Per Package) I_{out} = 0 μA, V_{in}=0 or V_{DD}	I_{DD}	5.0 10 15	– – –	20 40 80	– – –	0.005 0.010 0.015	20 40 80	– – –	150 300 600	μA
**Total Supply Current at an External Load Capacitance (C_L) on All Outputs	I_T	–	I_T = (1.5 μA/kHz) f + I_{DD} I_T = (3.0 μA/kHz) f + I_{DD} I_T = (4.5 μA/kHz) f + I_{DD}							μA

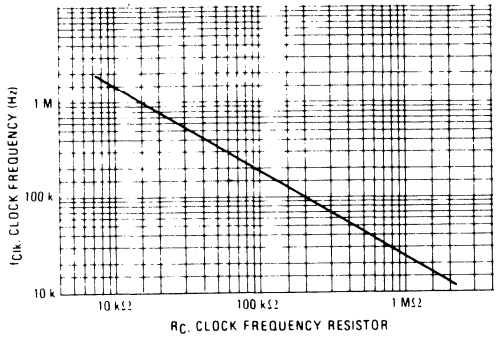
* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
** The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (T_A = 25°C; t_r = t_f = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1 TTL load for Data and Write.)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ #	All Types Max	Unit
Propagation Delay Time, X1 to RR	t_{PLH}, t_{PHL}	5.0	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
X1 to Flag F, Flag O, RTN, JMP		5.0	–	200	400	
		10	–	100	200	
		15	–	85	170	
X1 to Write		5.0	–	225	450	
		10	–	125	250	
		15	–	100	200	
X1 to Data		5.0	–	250	500	
		10	–	120	240	
		15	–	100	200	
RST to RR		5.0	–	250	500	
		10	–	125	250	
		15	–	100	200	
RST to X1		5.0	–	450	Note 1	
		10	–	200		
		15	–	150		
RST to Flag F, Flag O, RTN, JMP		5.0	–	400	800	
		10	–	200	400	
		15	–	150	300	
RST to Write, Data		5.0	–	450	900	
		10	–	225	450	
		15	–	175	350	
Clock Pulse Width, X1	$t_{W(cl)}$	5.0	400	200	–	ns
		10	200	100	–	
		15	180	90	–	
Reset Pulse Width, RST	$t_{W(R)}$	5.0	500	250	–	ns
		10	250	125	–	
		15	200	100	–	
Setup Time – Instruction	$t_{su(I)}$	5.0	400	200	–	ns
		10	250	125	–	
		15	180	90	–	
Data	$t_{su(D)}$	5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
Hold Time – Instruction	$t_{h(I)}$	5.0	100	0	–	ns
		10	50	0	–	
		15	50	0	–	
Data	$t_{h(D)}$	5.0	200	100	–	
		10	100	50	–	
		15	100	50	–	

NOTE 1. Maximum Reset Delay may extend to one-half clock period.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

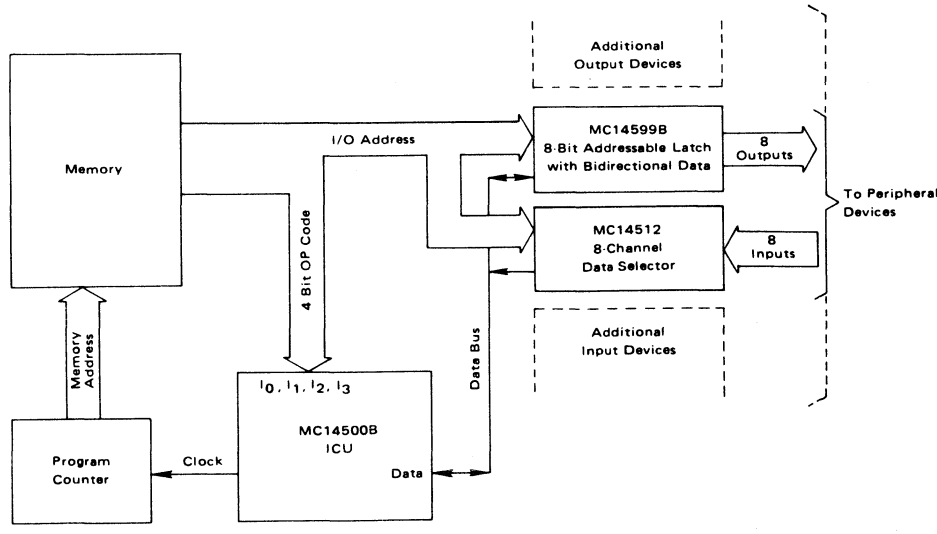


Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I_3
5	Bit 2 Instruction Word	I_2
6	Bit 1 Instruction Word	I_1
7	LSB Instruction Word	I_0
8	Negative Supply (Ground)	V_{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

TABLE 1. MC14500B INSTRUCTION SET

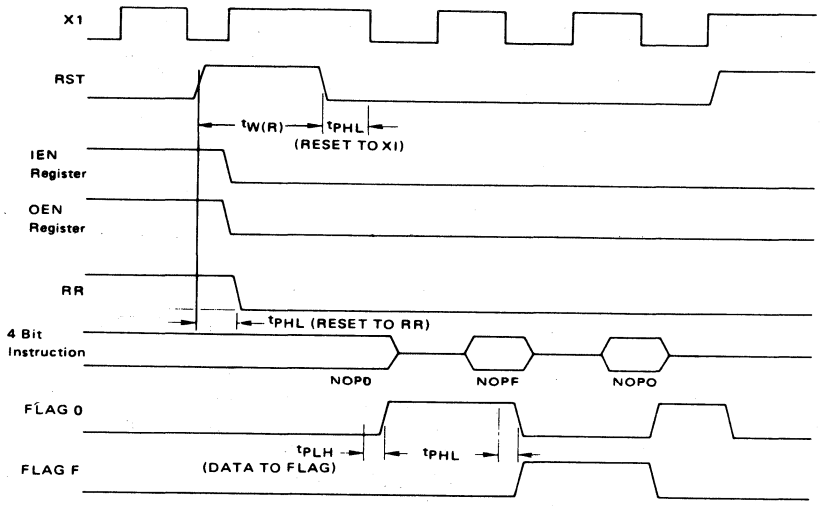
Instruction Code		Mnemonic	Action
0	0000	NOPO	No change in registers. RR → RR, Flag O → ⎍
1	0001	LD	Load result register. Data → RR
2	0010	LDC	Load complement. $\overline{Data}$ → RR
3	0011	AND	Logical AND. RR·Data → RR
4	0100	ANDC	Logical AND complement. RR·$\overline{Data}$ → RR
5	0101	OR	Logical OR. RR + Data → RR
6	0110	ORC	Logical OR complement. RR + $\overline{Data}$ → RR
7	0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8	1000	STO	Store. RR → Data Pin, Write → ⎍
9	1001	STOC	Store complement. $\overline{RR}$ → Data Pin, Write → ⎍
A	1010	IEN	Input enable. Data → IEN Register
B	1011	OEN	Output enable. Data → OEN Register
C	1100	JMP	Jump. JMP Flag → ⎍
D	1101	RTN	Return. RTN Flag → ⎍ and skip next instruction
E	1110	SKZ	Skip next instruction if RR = 0
F	1111	NOPF	No change in registers. RR → RR, Flag F → ⎍

FIGURE 2 – OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM

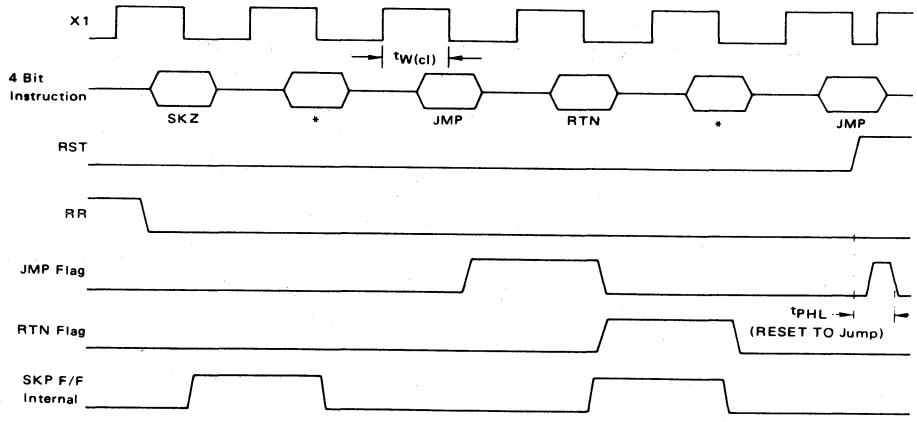


TIMING WAVEFORMS

Instructions NOPO, NOPF
RR, IEN, OEN remain unaffected



Instructions SKZ, JMP, RTN
RR, IEN, OEN remain unaffected

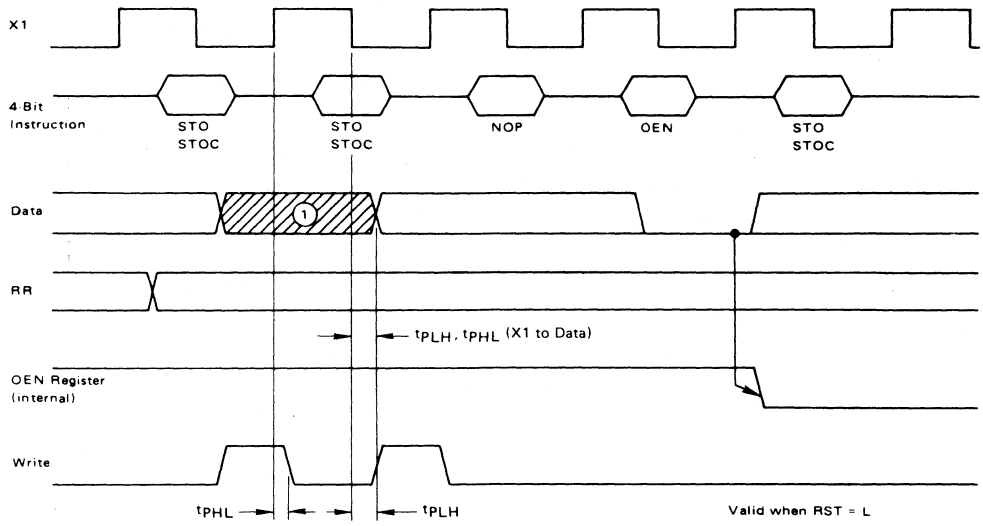


* Instructions Ignored.

6

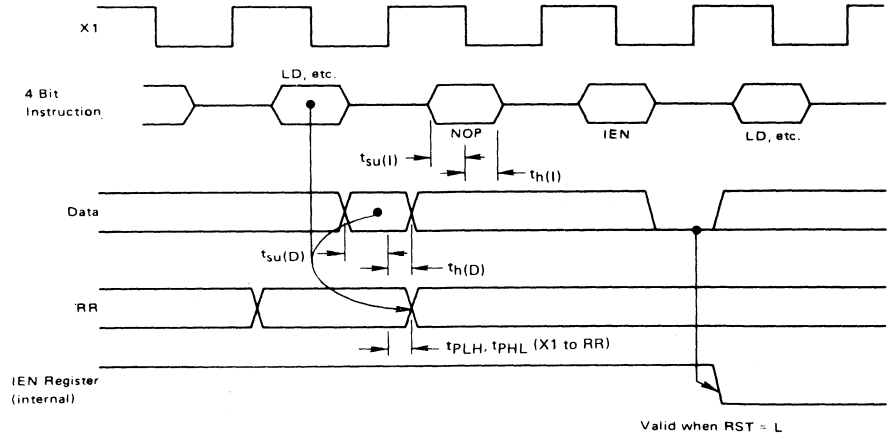
TIMING WAVEFORMS

Instructions STO, STOC, OEN



NOTE 1. Valid output data.

Instructions LD, LDC, AND, ANDC OR, ORC, XNOR, IEN



6

MOTOROLA

MC14501UB

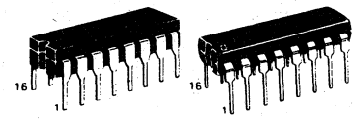
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501UB is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

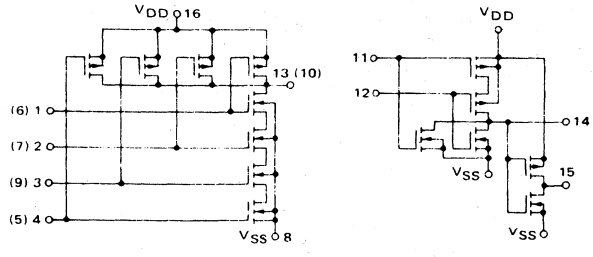
C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

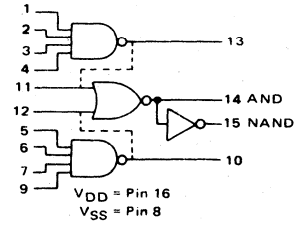
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
(V_O = 1.4 or 3.6 Vdc) "1" Level	V_{IH}	5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mAdc
(AL Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc) NAND*		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	–2.1	–	–1.75	–3.0	–	–1.22	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.42	–	–0.35	–0.63	–	–0.24	–	
(V_{OH} = 9.5 Vdc)		10	–1.06	–	–0.88	–1.58	–	–0.62	–	
(V_{OH} = 13.5 Vdc)		15	–3.1	–	–2.63	–6.12	–	–1.84	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	–3.6	–	–3.0	–5.1	–	–2.1	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.72	–	–0.6	–1.08	–	–0.42	–	
(V_{OH} = 9.5 Vdc) Inverter		10	–1.8	–	–1.5	–2.7	–	–1.05	–	
(V_{OH} = 13.5 Vdc)		15	–5.4	–	–4.5	–10.5	–	–3.15	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND*		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.92	–	0.77	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	2.34	–	1.95	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	6.12	–	5.1	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.54	–	1.28	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.90	–	3.25	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	10.2	–	8.5	22	–	5.95	–	
Output Drive Current	I_{OH}									mAdc
(CL/CP Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc) NAND*		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	–1.68	–	–1.4	–3.0	–	–1.05	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.34	–	–0.28	–0.63	–	–0.21	–	
(V_{OH} = 9.5 Vdc)		10	–0.84	–	–0.7	–1.58	–	–0.52	–	
(V_{OH} = 13.5 Vdc)		15	–2.52	–	–2.1	–6.12	–	–1.57	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	–2.88	–	–2.4	–5.1	–	–1.8	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.58	–	–0.48	–1.08	–	–0.36	–	
(V_{OH} = 9.5 Vdc) Inverter		10	–1.44	–	–1.2	–2.7	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.32	–	–3.6	–10.5	–	–2.7	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND*		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.79	–	0.66	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.98	–	1.65	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	5.4	–	4.5	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.32	–	1.1	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.3	–	2.75	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	9.0	–	7.5	22.0	–	5.95	–	

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

*The output drive current of Pin 15 is tested with Pin 14 open-circuited.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic		Figure	Symbol	V_{DD}	Typ #	Max	Unit
Output Rise Time	NAND, NOR	2, 3	t_{TLH}				ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	65	130	
Output Fall Time	NAND, NOR	2, 3	t_{THL}				ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	40	80	
Output Rise Time	NOR-Inverter	3	t_{TLH}				ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns				5.0	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns				10	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 17 ns				15	40	80	
Output Fall Time	NOR-Inverter	3	t_{THL}				ns
t_{THL} = (0.67 ns/pF) C_L + 26.5 ns				5.0	60	120	
t_{THL} = (0.45 ns/pF) C_L + 17.5 ns				10	40	80	
t_{THL} = (0.37 ns/pF) C_L + 11.5 ns				15	30	60	
Propagation Delay Time	NAND	2	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns				50	130	260	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	NOR	3	t_{PLH}, t_{PHL}	5.0	115	230	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns				10	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns				15	45	90	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns	NOR-Inverter	3	t_{PLH}, t_{PHL}	5.0	130	260	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	

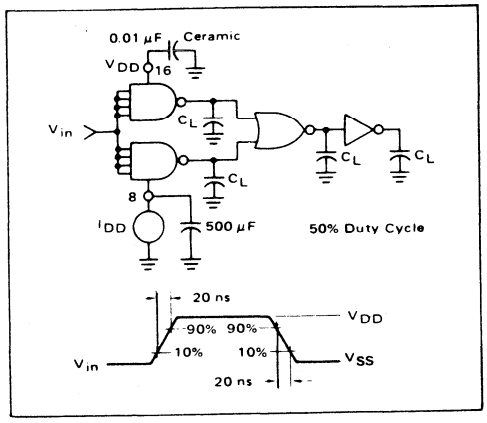
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



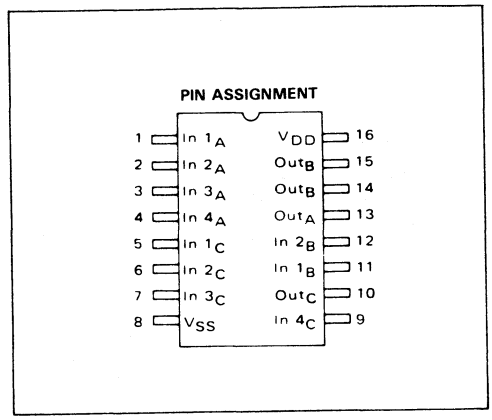


FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

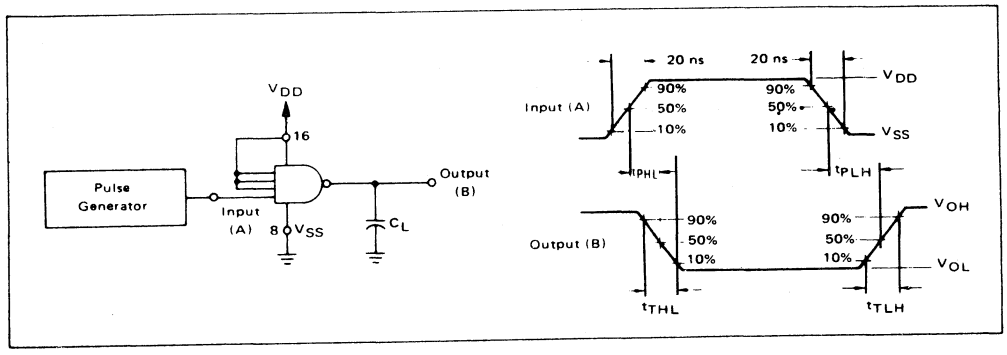
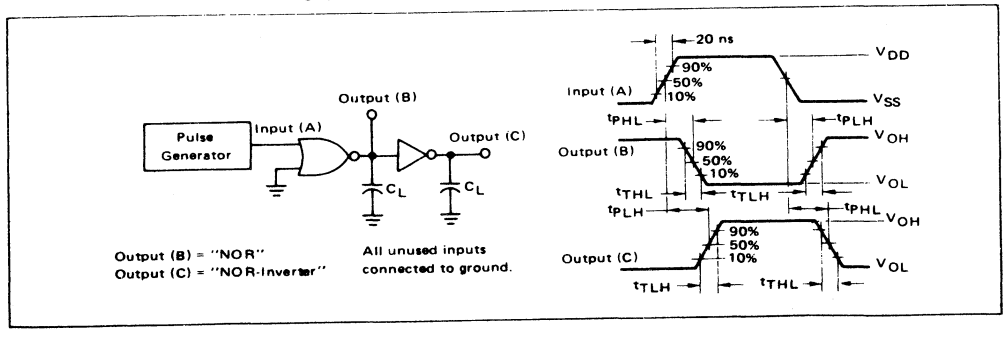


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



6

MOTOROLA

MC14502B

STROBED HEX INVERTER/BUFFER

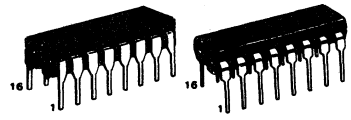
The MC14502B is a strobed hex buffer/inverter with 3-state outputs, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Separate Output Disable Control
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 4LSTTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

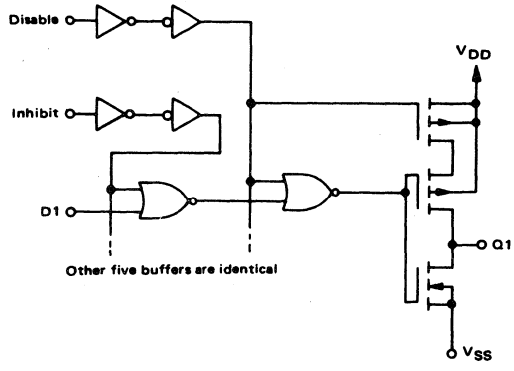
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

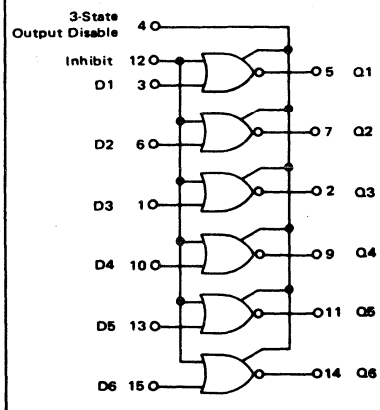
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	+30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	**3.5**	–	**2.8**	**6.6**	–	**2.0**	–	mAdc
(V_{OL} = 0.5 Vdc)		10	**7.8**	–	**6.3**	**17**	–	**4.4**	–	
(V_{OL} = 1.5 Vdc)		15	**29**	–	**24**	**66**	–	**16**	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	**2.3**	–	**1.9**	**6.6**	–	**1.6**	–	mAdc
(V_{OL} = 0.5 Vdc)		10	**5.0**	–	**4.2**	**17**	–	**3.4**	–	
(V_{OL} = 1.5 Vdc)		15	**19**	–	**16**	**66**	–	**13**	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	**1.0**	–	**0.002**	**1.0**	–	**30**	µAdc
(Per Package)		10	–	**2.0**	–	**0.004**	**2.0**	–	**60**	
		15	–	**4.0**	–	**0.006**	**4.0**	–	**120**	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	**4.0**	–	**0.002**	**4.0**	–	**30**	µAdc
(Per Package)		10	–	**8.0**	–	**0.004**	**8.0**	–	**60**	
		15	–	**16**	–	**0.006**	**16**	–	**120**	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (5.3 µA/kHz) f + I_{DD}							
		15	I_T = (8.0 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

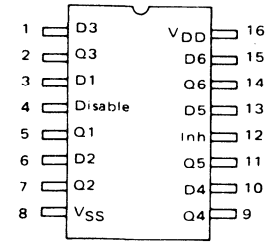
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	40	80	ns
		10	–	20	40	
		15	–	15	30	
Propagation Delay Time Data to Q	t_{PHL}	5.0	–	135	270	ns
		10	–	55	110	
		15	–	40	80	
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0	–	335	670	ns
		10	–	145	290	
		15	–	95	190	
Propagation Delay Time Data to Q, Inhibit to Q	t_{PLH}	5.0	–	295	590	ns
		10	–	130	260	
		15	–	95	190	
3-State Propagation Delay, Output "1" to High Impedance	t_{PHZ}	5.0	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
3-State Propagation Delay, High Impedance to "1" Level	t_{PZH}	5.0	–	260	520	ns
		10	–	105	210	
		15	–	80	160	
3–State Propagation Delay, Output "0" to High Impedance	t_{PLZ}	5.0	–	150	300	ns
		10	–	70	140	
		15	–	55	110	
3-State Propagation Delay, High Impedance to "0" Level	t_{PZL}	5.0	–	160	320	ns
		10	–	65	130	
		15	–	50	100	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

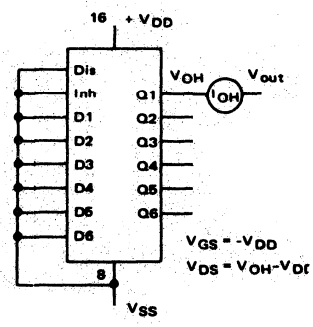
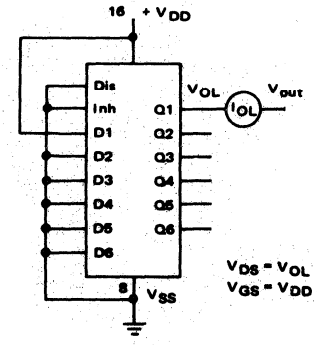


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})



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FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

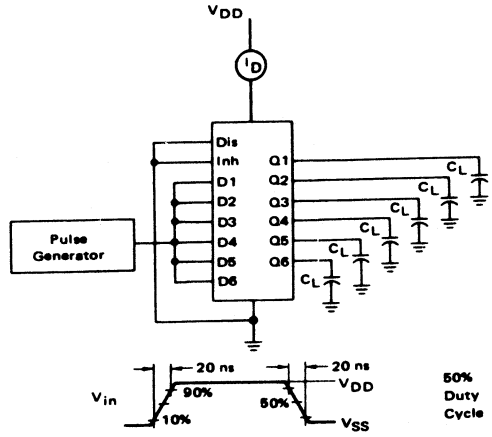
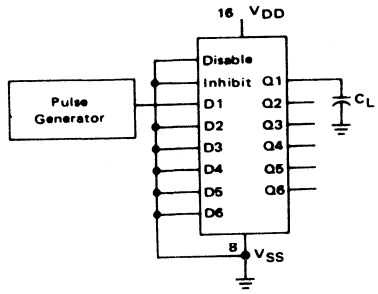


FIGURE 4 — AC TEST CIRCUIT AND WAVEFORMS (t_{TLH}, t_{THL}, t_{PLH}, and t_{PHL})



For all t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH} measurements V_{in} may be applied to any other D_n input or to Inhibit.

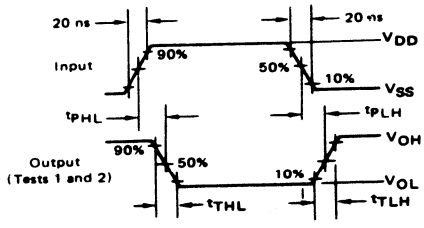
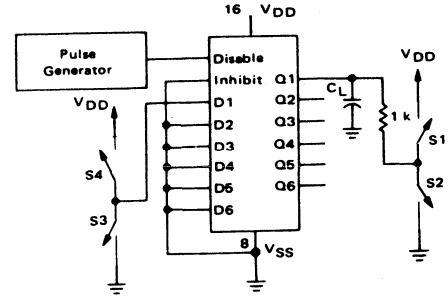
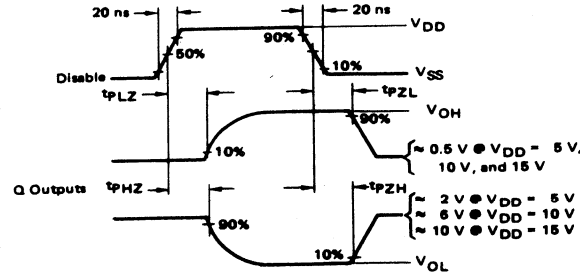


FIGURE 5 — 3-STATE AC TEST CIRCUIT AND WAVEFORMS (t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL})

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open





6

MOTOROLA

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

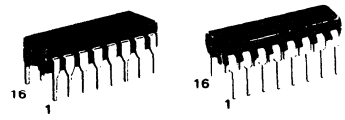
The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

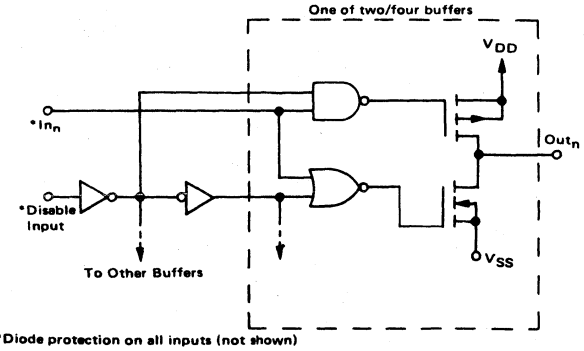
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

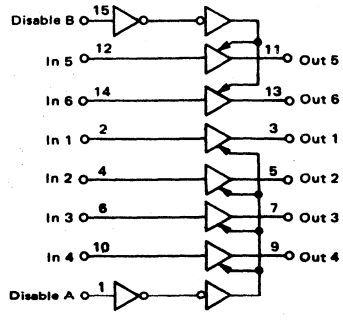
X = Don't Care

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 1.4 or 3.6 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 2.8 or 7.2 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	-4.3	–	-3.6	-5.0	–	-2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.8	–	-4.80	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.2	–	-1.02	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-3.1	–	-2.60	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-8.2	–	-6.80	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.5	2.2	–	1.8	2.1	–	1.2	–	
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.10	25.00	–	11.2	–	
Output Drive Current (CL/CP Device)***	I_{OH}						–			mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.0	–	-3.60	-5.5	–	-2.4	–	
(V_{OH} = 2.5 Vdc)		5.0	-4.6	–	-4.20	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-0.88	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-2.4	–	-2.20	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-6.6	–	-6.00	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.1	–	1.95	2.2	–	1.25	–	
(V_{OL} = 0.4 Vdc)		5.0	2.3	–	2.10	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.45	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	15.2	–	13.80	25.00	–	11.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**†	I_T	5.0	$I_T = (2.5\ \mu A/kHz)\ f + I_{DD}$							µAdc
(Dynamic plus Quiescent, Per Package)		10	$I_T = (6.0\ \mu A/kHz)\ f + I_{DD}$							
(C_L = 50 pF on all outputs)		15	$I_T = (10\ \mu A/kHz)\ f + I_{DD}$							
(All outputs switching, 50% Duty Cycle)										
3-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
(AL Device)			–		–			–		
3-State Output Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc
(CL/CP Device)			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

***Care must be taken not to exceed maximum current ratings (see maximum ratings table)

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.006.

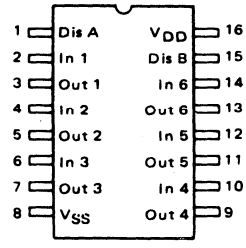
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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ #	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3-State Propagation Delay Time	t_{PHZ}	5.0	75	150	ns
Output "1" to High Impedance		10	40	80	
		15	35	70	
Output "0" to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to "0" Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

PIN ASSIGNMENT



6

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

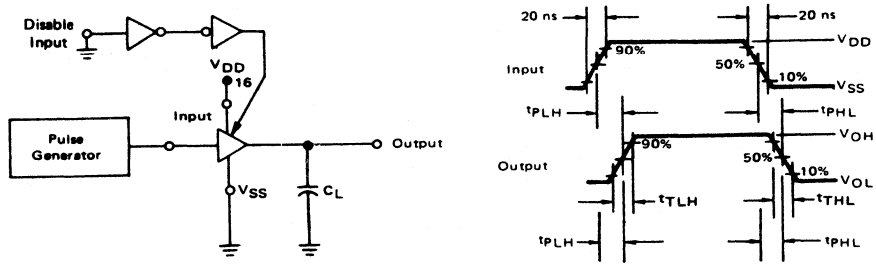
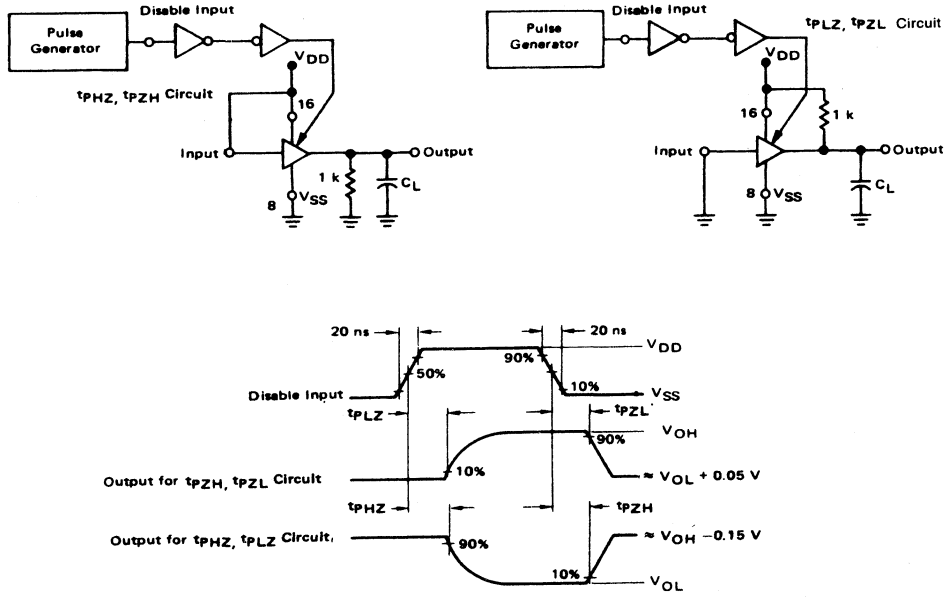


FIGURE 2 — 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})



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MOTOROLA

MC14504B

CMOS SSI

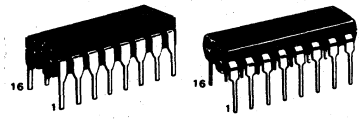
(LOW-POWER COMPLEMENTARY MOS)

TTL or CMOS to CMOS HEX LEVEL SHIFTER

HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

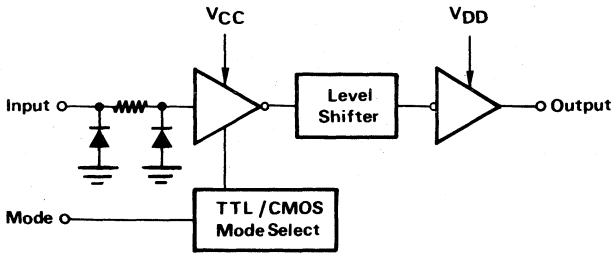
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

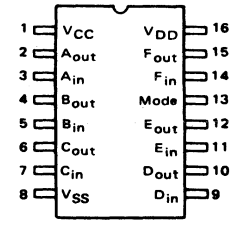
LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields **referenced to the V_{SS} pin, only.** Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{in} \leq 18$ V and $V_{SS} \leq V_{out} \leq V_{DD}$ are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +18.0	V
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}	Input Voltage (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package**	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum ratings are those values beyond which damage to the device may occur.
**Power dissipation temperature derating: Plastic "P" package: −12 mW/°C from 65°C to 85°C. Ceramic "L" package: −12 mW/C° from 100°C to 125°C.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}										Vdc
V_{in} = 0 V		–	5.0	–	0.05	–	0	0.05	–	0.05	
		–	10	–	0.05	–	0	0.05	–	0.05	
		–	15	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{CC} "1" Level	V_{OH}										Vdc
		–	5.0	4.95	–	4.95	5.0	–	4.95	–	
		–	10	9.95	–	9.95	10	–	9.95	–	
		–	15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL-CMOS		5	10	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.5 Vdc) TTL-CMOS		5	15	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.0 Vdc) CMOS-CMOS		5	10	–	1.5	–	2.25	1.5	–	1.4	
(V_{OL} = 1.5 Vdc) CMOS-CMOS		5	15	–	1.5	–	2.25	1.5	–	1.5	
(V_{OL} = 1.5 Vdc) CMOS-CMOS		10	15	–	3.0	–	4.5	3.0	–	2.9	
Input Voltage "1" Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL-CMOS		5	10	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 13.5 Vdc) TTL-CMOS		5	15	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 9.0 Vdc) CMOS-CMOS		5	10	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS-CMOS		5	15	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS-CMOS		10	15	7.1	–	7.0	5.5	–	7.0	–	
Output Drive Current (AL Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	-3.0	–	−2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	-0.64	–	−0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	-1.6	–	−1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	-4.2	–	−3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL)	I_{in}	–	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP)	I_{in}	–	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD} or	–	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)	I_{CC}	–	10	–	0.10	–	0.0010	0.10	–	3.0	
CMOS-CMOS Mode		–	15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD} or	–	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)	I_{CC}	–	10	–	1.0	–	0.0010	1.0	–	7.5	
CMOS-CMOS Mode		–	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{DD}	5.0	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)		5.0	10	–	1.0	–	0.0010	1.0	–	7.5	
TTL-CMOS Mode		5.0	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{CC}	5.0	5.0	–	5.0	–	2.5	5.0	–	6.0	mAdc
(Per Package)		5.0	10	–	5.0	–	2.5	5.0	–	6.0	
TTL-CMOS Mode		5.0	15	–	5.0	–	2.5	5.0	–	6.0	

*T_{LOW} = −55°C for AL Device, −40°C for CL/CP Device
T_{HIGH} = +125°C for AL Device, +85°C for CL/CP Device

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits Min	Limits Typ #	Limits Max	Units
Propagation Delay, High to Low	t_{PHL}	TTL–CMOS	5.0	10	–	140	280	ns
		$V_{DD} > V_{CC}$	5.0	15	–	140	280	
		CMOS–CMOS	5.0	10	–	120	240	
		$V_{DD} > V_{CC}$	5.0	15	–	120	240	
			10	15	–	70	140	
		CMOS–CMOS	10	5.0	–	185	370	
		$V_{CC} > V_{DD}$	15	5.0	–	185	370	
			15	10	–	175	350	
Propagation Delay, Low to High	t_{PLH}	TTL–CMOS	5.0	10	–	170	340	ns
		$V_{DD} > V_{CC}$	5.0	15	–	160	320	
		CMOS–CMOS	5.0	10	–	170	340	
		$V_{DD} > V_{CC}$	5.0	15	–	170	340	
			10	15	–	100	200	
		CMOS–CMOS	10	5.0	–	275	550	
		$V_{CC} > V_{DD}$	15	5.0	–	275	550	
			15	10	–	145	290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	–	5.0	–	100	200	ns
			–	10	–	50	100	
			–	15	–	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – INPUT SWITCHPOINT CMOS to CMOS MODE

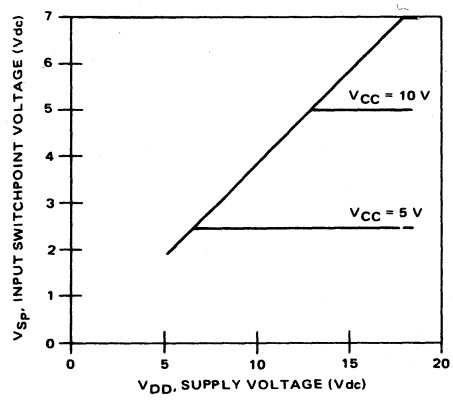


FIGURE 2 – INPUT SWITCHPOINT TTL to CMOS MODE

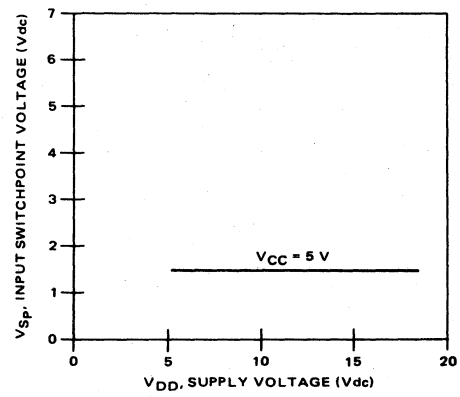


FIGURE 3 – OPERATING BOUNDARY CMOS to CMOS MODE

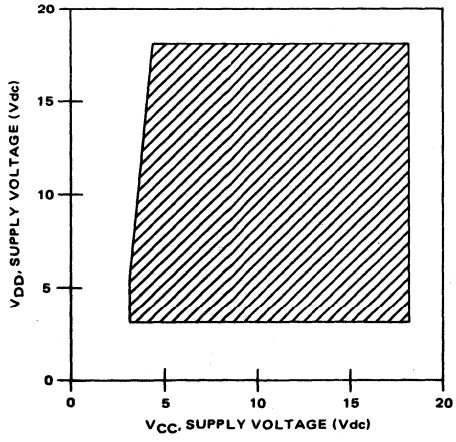
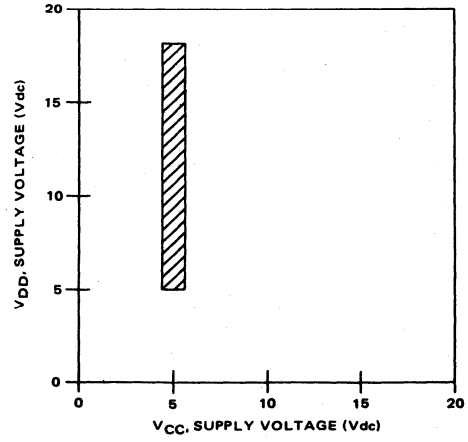


FIGURE 4 – OPERATING BOUNDARY TTL to CMOS MODE



6

MOTOROLA

MC14506UB

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

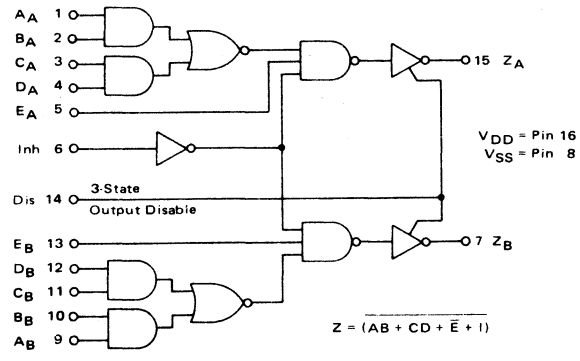
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

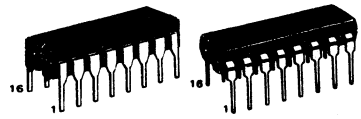
LOGIC DIAGRAM



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.0	–	4.50	2 0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.1 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

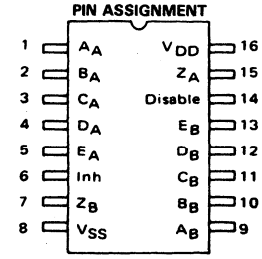
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

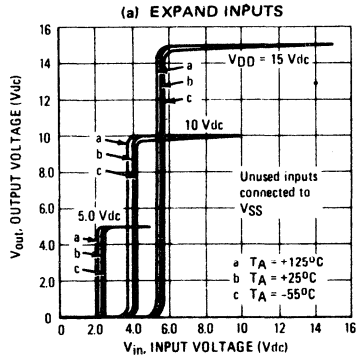
Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 210 ns		5.0	–	295	580	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	225	
t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	180	
t_{PHL} = (1.7 ns/pF) C_L + 185 ns	t_{PHL}	5.0	–	270	480	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	140	
Expand Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	430	
t_{PLH} = (0.66 ns/pF) C_L + 42 ns		10	–	75	160	
t_{PLH} = (0.5 ns/pF) C_L + 25 ns		15	–	50	125	
t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	–	200	330	ns
t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	110	
t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	90	
Inhibit Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	500	
t_{PLH} = (0.66 ns/pF) C_L + 67 ns		10	–	100	225	
t_{PLH} = (0.5 ns/pF) C_L + 40 ns		15	–	65	160	
t_{PHL} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	400	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	150	
3-State Propagation Delay Time						
"1" to High Impedance	t_{PHZ}	5.0	–	60	150	ns
		10	–	45	110	
		15	–	35	90	
"0" to High Impedance	t_{PLZ}	5.0	–	90	225	ns
		10	–	55	140	
		15	–	40	100	
High Impedance to "1"	t_{PZH}	5.0	–	110	300	ns
		10	–	50	125	
		15	–	40	100	
High Impedance to "0"	t_{PZL}	5.0	–	170	425	ns
		10	–	70	175	
		15	–	50	125	

*The formulas given are for the typical characteristics only at 25°C.

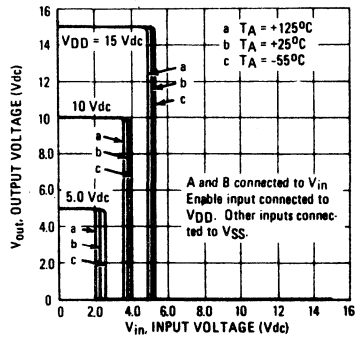
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

(a) EXPAND INPUTS



(b) DATA INPUTS



6

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

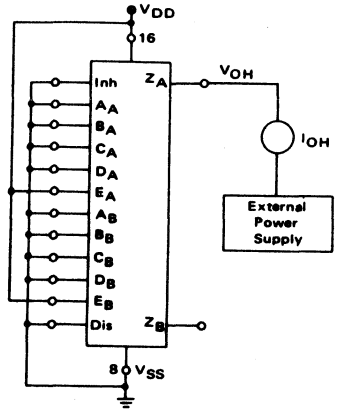


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

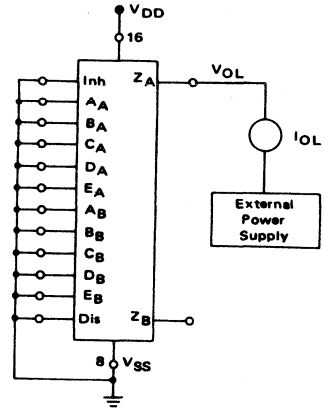


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

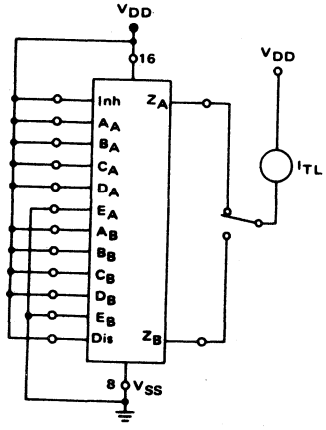
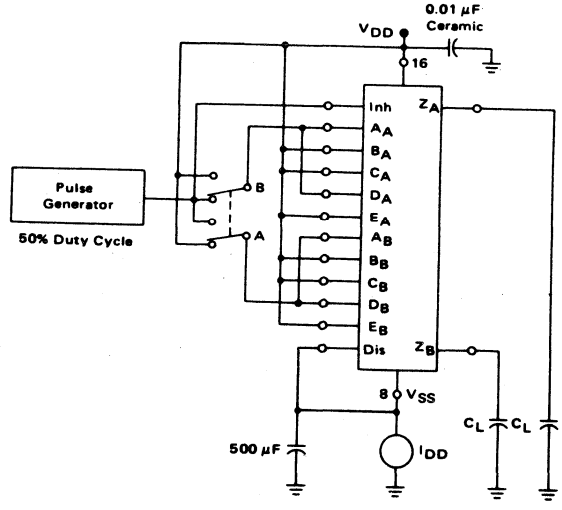


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT



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FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

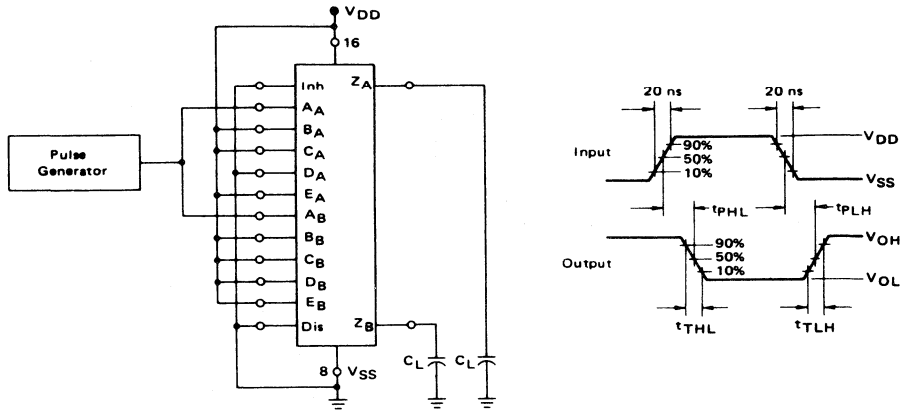
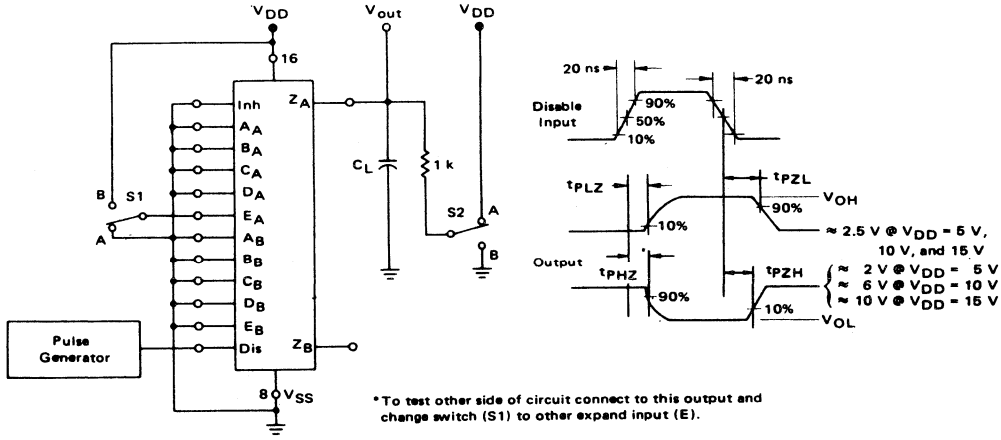


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
t_{PLZ}	A	A
t_{PHZ}	B	B
t_{PZL}	A	A
t_{PZH}	B	B

6

MOTOROLA

MC14508B

DUAL 4-BIT LATCH

The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

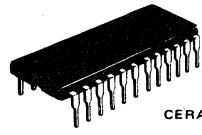
These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

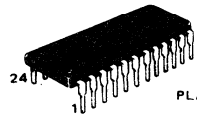
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

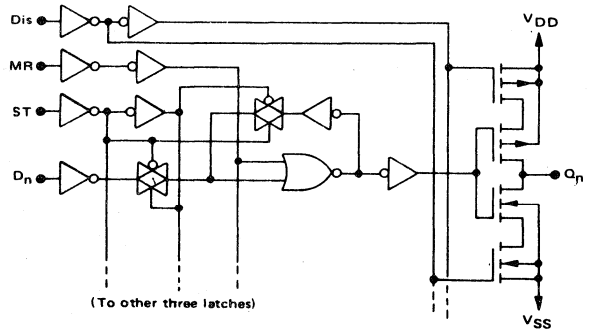
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

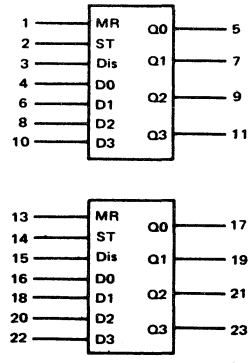
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

CIRCUIT DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.91 μA/kHz) f + I_{DD}							
		15	I_T = (4.37 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ #	All Types Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, Dn or MR to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Master Reset Removal Time	t_{rem}	5.0	30	−15	—	ns
		10	25	0	—	
		15	20	0	—	
Strobe Pulse Width	$t_{WH(S)}$	5.0	140	70	–	ns
		10	70	35	–	
		15	40	20	–	
Setup Time	t_{su}	5.0	50	25	–	ns
Data to Strobe		10	20	10	–	
		15	10	5.0	–	
Hold Time	t_h	5.0	50	20	–	ns
Strobe to Data		10	35	10	–	
		15	35	10	–	
3-State Propagation Delay Time	t_{PHZ}					ns
Output "1" to High Impedance		5.0	–	55	170	
		10	–	35	100	
		15	–	30	70	
Output "0" to High Impedance	t_{PLZ}	5.0	–	75	170	
		10	–	40	100	
		15	–	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	–	80	170	
		10	–	35	100	
		15	–	30	70	
High Impedance to "0" Level	t_{PZL}	5.0	–	105	210	
		10	–	50	100	
		15	–	35	70	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

PIN ASSIGNMENT

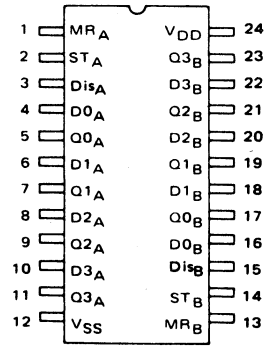


FIGURE 1 – AC WAVEFORMS

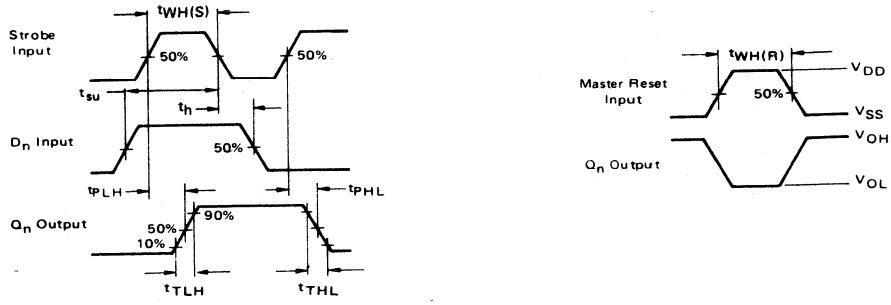
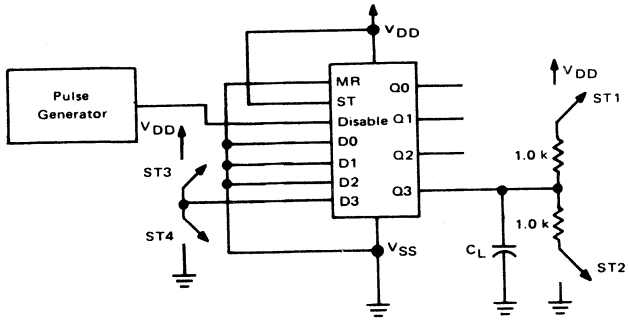
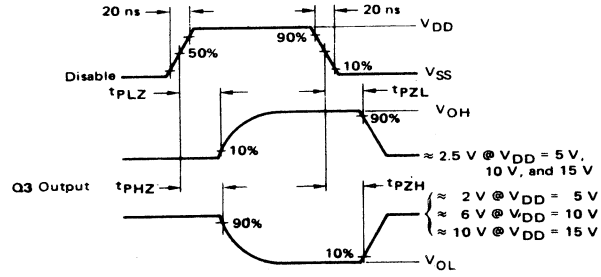


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

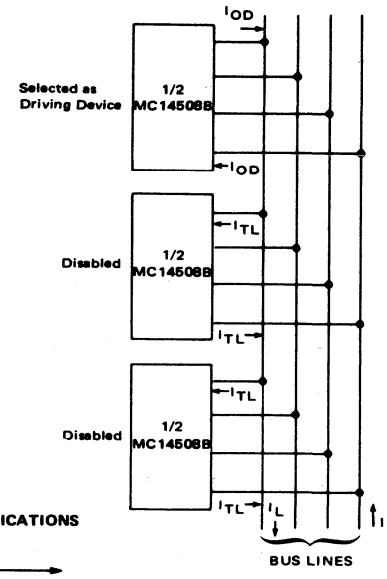


3-STATE MODE OF OPERATION

The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

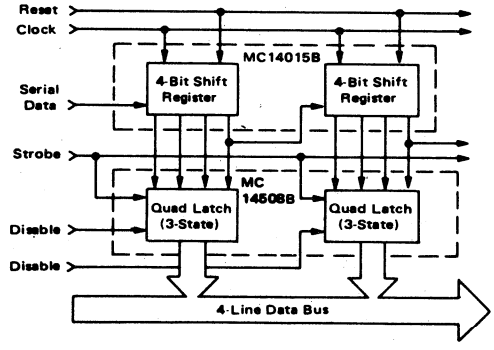
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

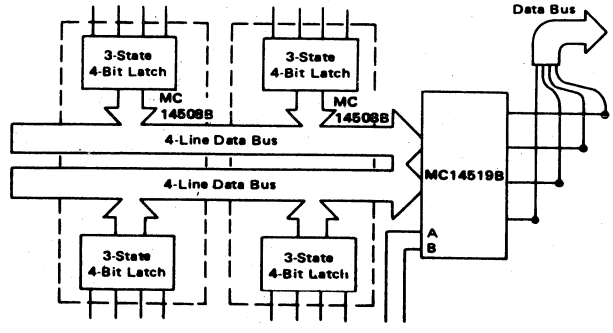


TYPICAL 3-STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



MOTOROLA

MC14510B

BCD UP/DOWN COUNTER

The MC14510B synchronous up/down BCD counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability.

This counter can be preset by applying the desired value in BCD to the Preset inputs (P1, P2, P3, P4) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the $\overline{\text{Carry Out}}$ to the $\overline{\text{Carry In}}$ of the next stage while clocking each counter in parallel. The ouputs (Q1, Q2, Q3, Q4) can be reset to a low state by applying a high to the Reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0	⎍	Count Up
0	0	0	0	⎍	Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

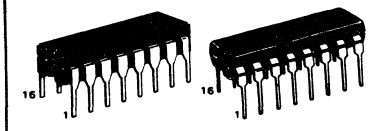
X = Don't Care

Note: When counting up, the $\overline{\text{Carry Out}}$ signal is normally high, and is low only when Q1 and Q4 are high and $\overline{\text{Carry In}}$ is low. When counting down, $\overline{\text{Carry Out}}$ is low only when Q1 through Q4 and $\overline{\text{Carry In}}$ are low.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

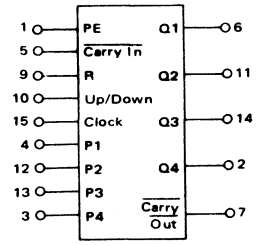
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.70	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

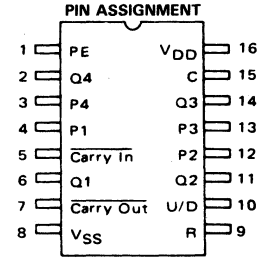
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C, See Figure 2)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	—	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	—	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
Preset or Reset to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	—	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	—	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	—	150	300	
Reset Pulse Width	$t_{w(H)}$	5.0	360	180	—	ns
		10	210	105	—	
		15	160	80	—	
Clock Pulse Width	$t_{w(H)}$	5.0	350	200	—	ns
		10	170	100	—	
		15	140	75	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Preset or Reset Removal Time	t_{rem}	5.0	650	325	—	ns
The Preset or Reset Signal must be low prior to a positive-going transition of the clock.		10	230	115	—	
		15	180	90	—	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Setup Time $\overline{\text{Carry In}}$ to Clock	t_{su}	5.0	260	130	—	ns
		10	120	60	—	
		15	100	50	—	
Hold Time Clock to $\overline{\text{Carry In}}$	t_h	5.0	0	−50	—	ns
		10	10	−15	—	
		15	10	−5	—	
Setup Time Up/Down to Clock	t_{su}	5.0	500	250	—	ns
		10	200	100	—	
		15	175	75	—	
Hold Time Clock to Up/Down	t_h	5.0	−70	−140	—	ns
		10	−30	−80	—	
		15	−20	−50	—	
Setup Time Pn to PE	t_{su}	5.0	−50	−100	—	ns
		10	−30	−65	—	
		15	−25	−55	—	
Hold Time PE to Pn	t_h	5.0	480	240	—	ns
		10	410	205	—	
		15	410	205	—	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

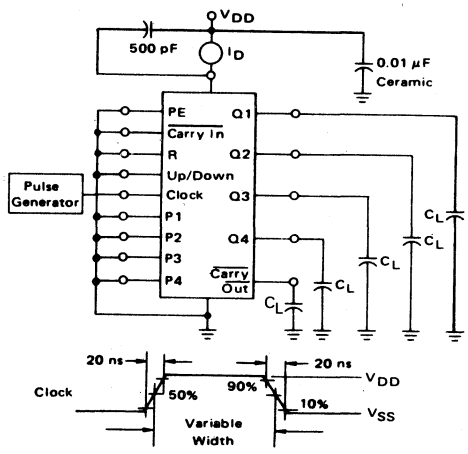
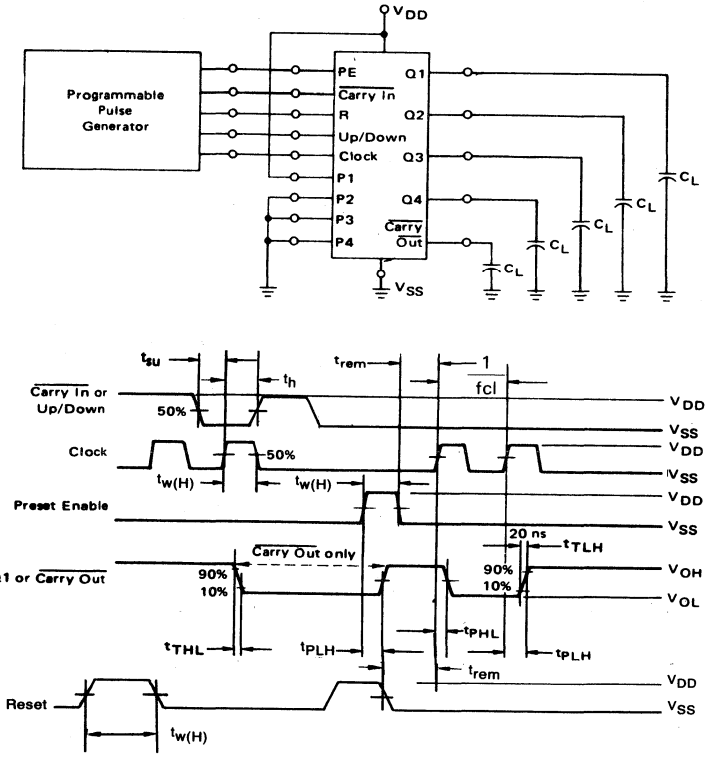
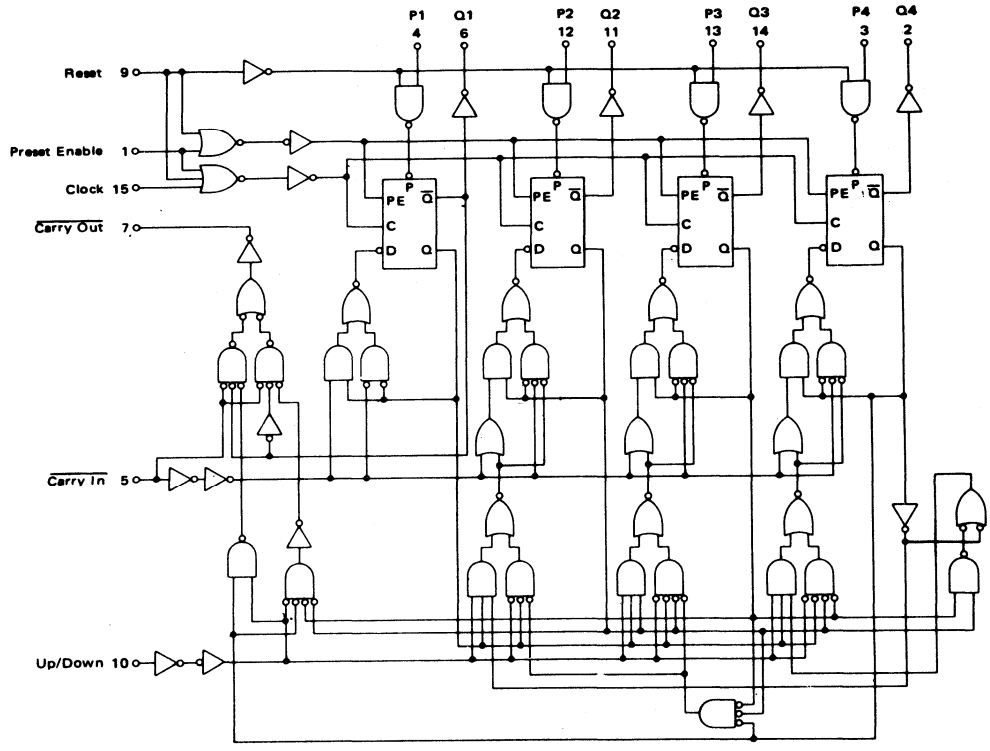


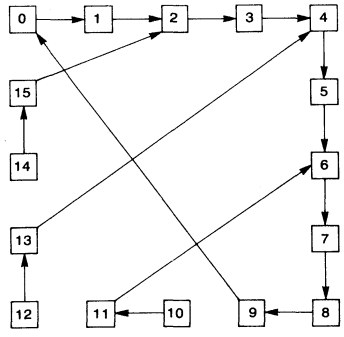
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



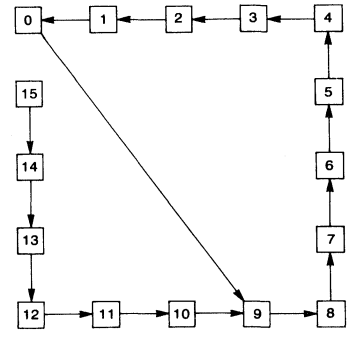
LOGIC DIAGRAM



STATE DIAGRAM FOR UP COUNTING



STATE DIAGRAM FOR DOWN COUNTING



6

PIN DESCRIPTIONS

INPUTS

P1, P2, P3, P4, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

$\overline{\text{Carry In}}$, (Pin 5) — Active-low input used when cascading stages. Usually connected to $\overline{\text{Carry Out}}$ of the previous stage. While high, clock is inhibited.

Clock, (Pin 15) — BCD data is incremented or decremented, depending on the direction of count, on the positive transition of this signal.

OUTPUTS

Q1, Q2, Q3, Q4, BCD outputs (Pins 6, 11, 14, 2) — BCD data is present on these outputs with Q1 corresponding to the least significant bit.

$\overline{\text{Carry Out}}$, (Pin 7) — Used when cascading stages, this pin is usually connected to $\overline{\text{Carry In}}$ of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and will inhibit the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and will inhibit the clock when high.

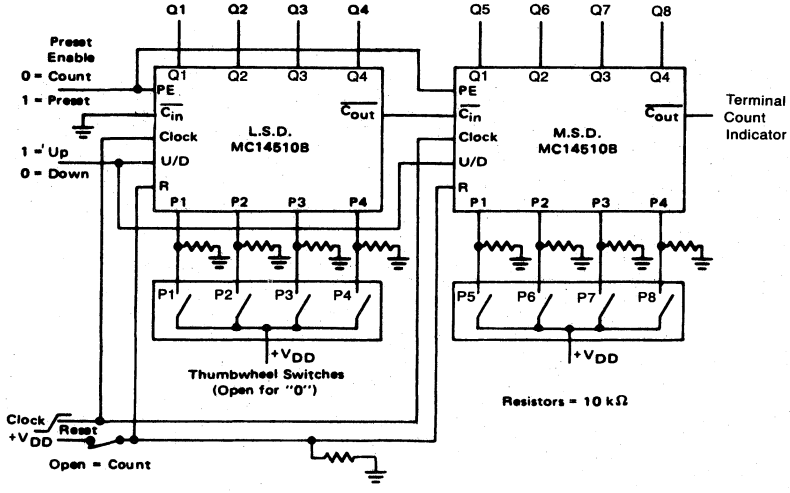
Up/Down, (Pin 10) — Controls the direction of count: high for up count, low for down count.

SUPPLY PINS

V_{SS}, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

V_{DD}, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 Vdc to 18.0 Vdc.

FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



Note: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) does not change while $\overline{C}_{in}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 9 (count up mode), $\overline{C}_{out}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. The L.S.D. now counts through another cycle (10 clock pulses) and the above cycle is repeated.

TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER

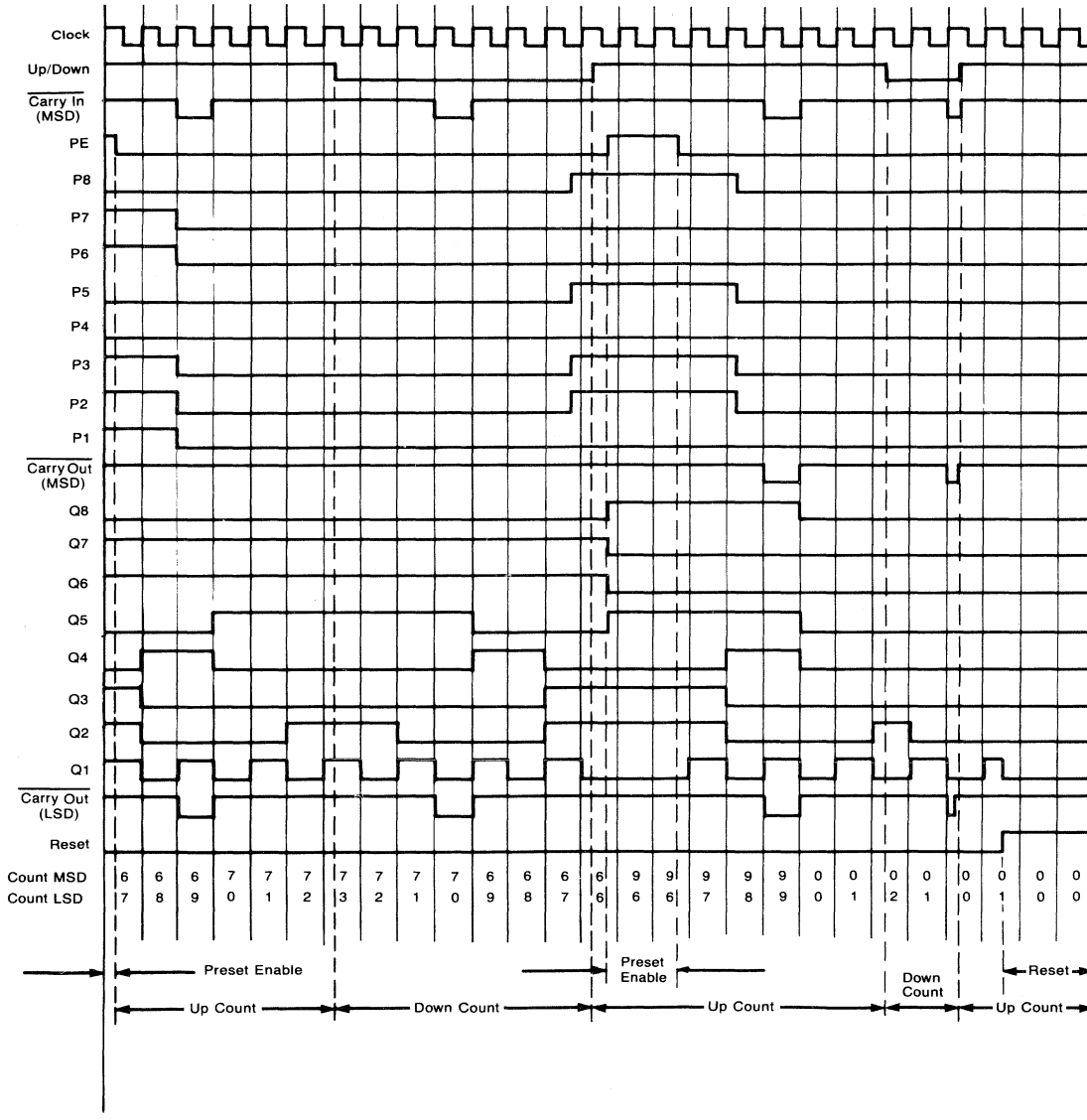
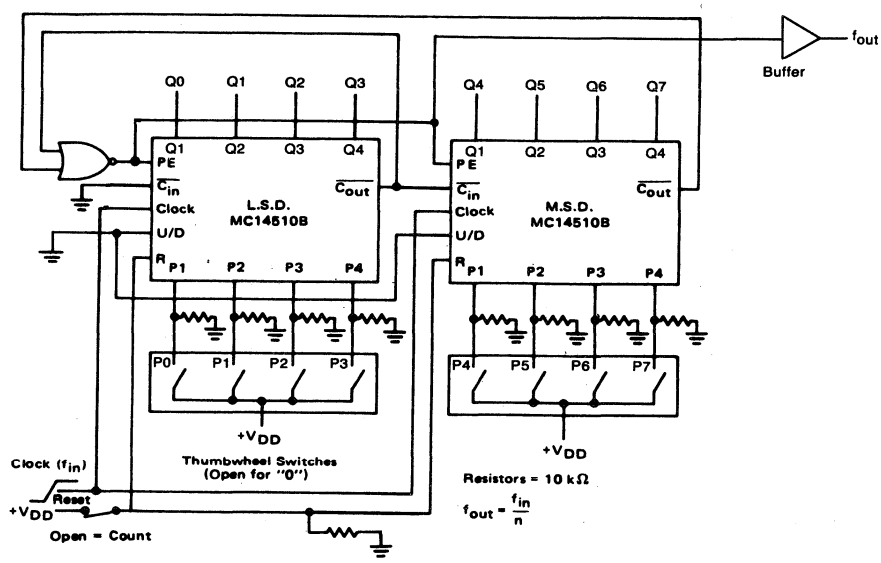


FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Note: The programmable frequency divider can be set by applying the desired divide ratio, in BCD, to the preset inputs. For example, the maximum divide ratio of 99 may be obtained by applying a 10011001 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

6

MOTOROLA

MC14512B

8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

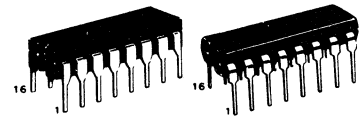
C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
X	X	X	1	0	0
X	X	X	X	1	High Impedance

X = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

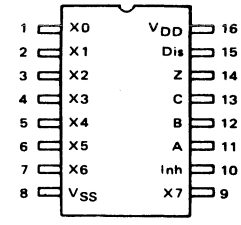
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)			10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)			15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)			10	–	40	–	0.010	40	–	300	
			15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	$I_T = (0.8\ \mu A/kHz)f + I_{DD}$							µAdc
			10	$I_T = (1.6\ \mu A/kHz)f + I_{DD}$							
			15	$I_T = (2.4\ \mu A/kHz)f + I_{DD}$							
Three-State Leakage Current (AL Device)		I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)		I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, See Figure 1)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ #	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 100 50 40	 200 100 80	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PLH}	 5.0 10 15	 330 125 85	 650 250 170	ns
Propagation Delay Time (Figure 2) Inhibit, Control, or Data to Z	t_{PHL}	 5.0 10 15	 330 125 85	 650 250 170	ns
3-State Output Delay Times (Figure 3) "1" or "0" to High Z, and High Z to "1" or "0"	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	5.0 10 15	60 35 30	150 100 75	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

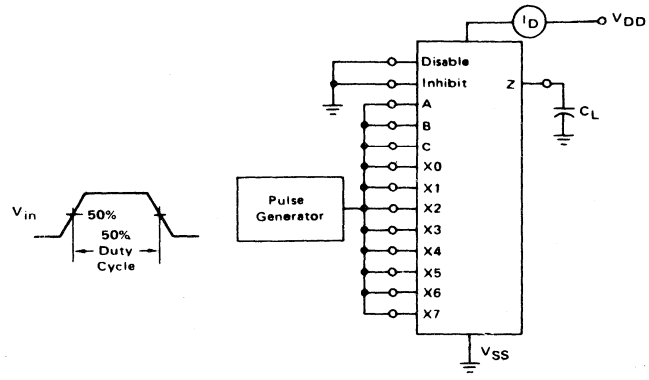
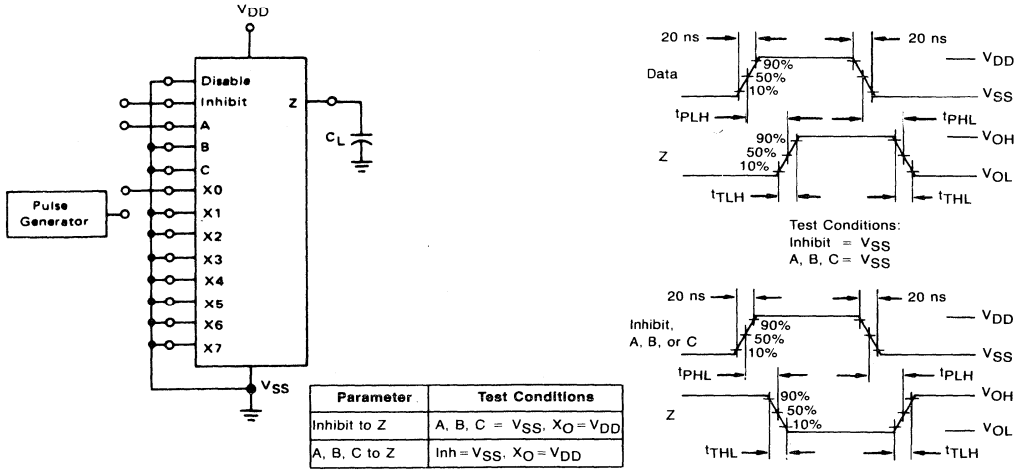
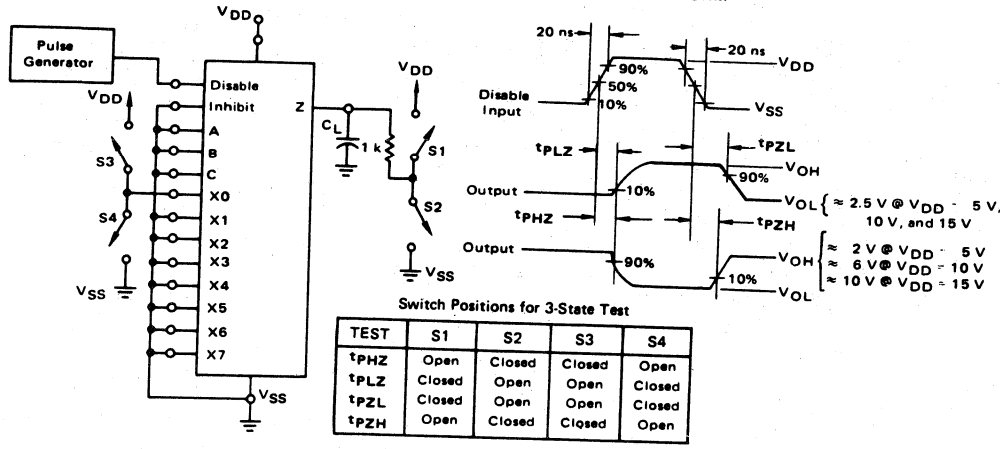


FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Parameter	Test Conditions
Inhibit to Z	A, B, C = V_{SS}, X_O = V_{DD}
A, B, C to Z	Inh = V_{SS}, X_O = V_{DD}

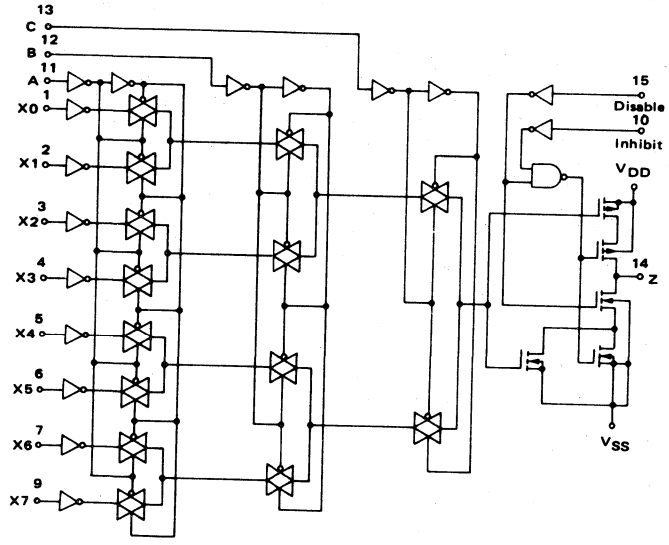
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM

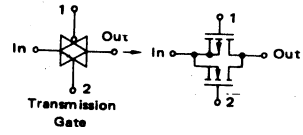


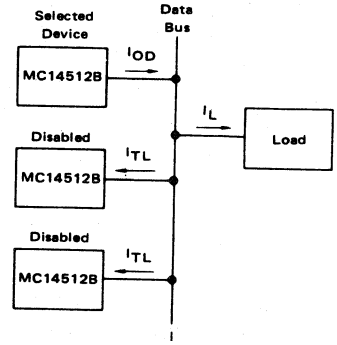
Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

LOGIC DIAGRAM







3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MOTOROLA

MC14514B
MC14515B

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

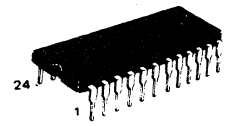
These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

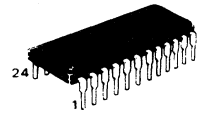
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

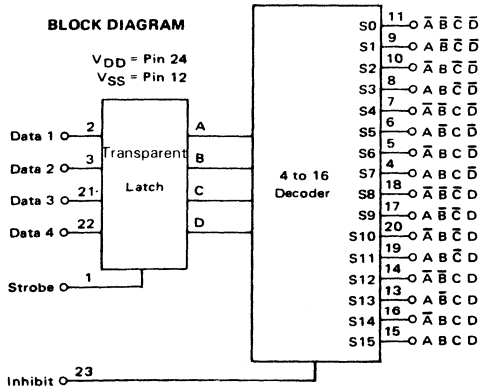
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

BLOCK DIAGRAM

V_{DD} = Pin 24
V_{SS} = Pin 12



DECODE TRUTH TABLE (Strobe = 1)*

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care
*Strobe = 0, Data is latched

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.35 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.70 μA/kHz) f + I_{DD}							
		15	I_T = (4.05 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

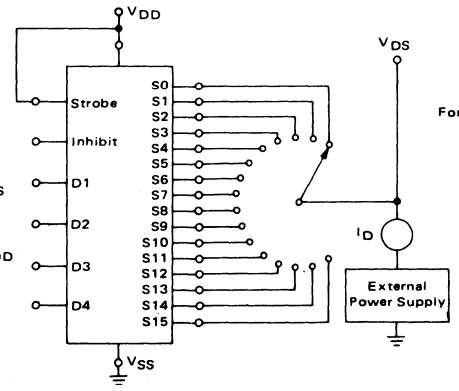
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time; Data, Strobe to S	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Inhibit Propagation Delay Times	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Setup Time	t_{su}					ns
Data to Strobe		5.0	250	125	–	
		10	100	50	–	
		15	75	38	–	
Hold Time	t_h					ns
Strobe to Data		5.0	−20	−100	—	
		10	0	−40	—	
		15	10	−30	—	
Strobe Pulse Width	t_{WH}					ns
		5.0	350	175	–	
		10	100	50	–	
		15	75	38	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT



For MC14514B

1. For P-channel: Inhibit = V_{SS} and D1–D4 constitute binary code for "output under test."
2. For N-channel: Inhibit = V_{DD}

For MC14515B

1. For P-channel: Inhibit = V_{DD}
2. For N-channel: Inhibit = V_{SS} and D1–D4 constitute binary code for "output under test."

6

FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

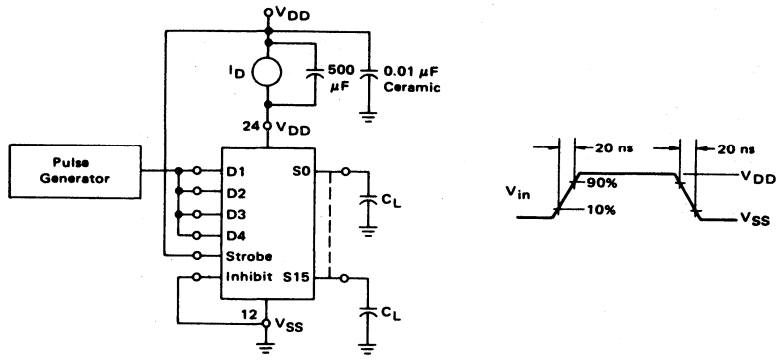
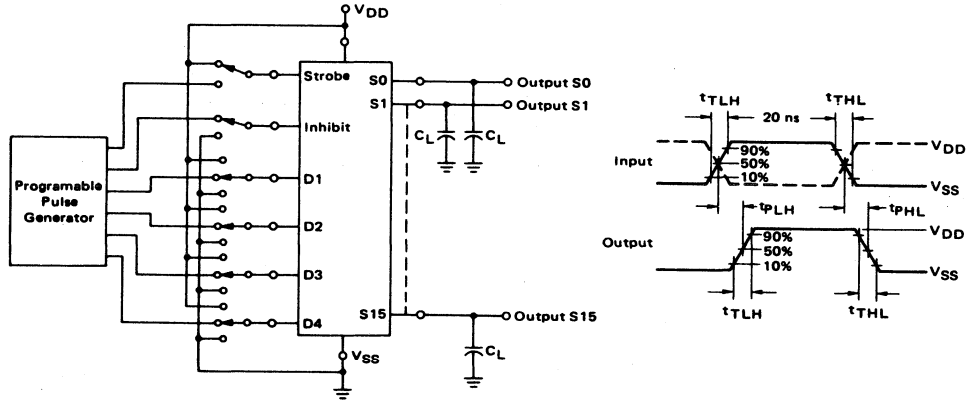
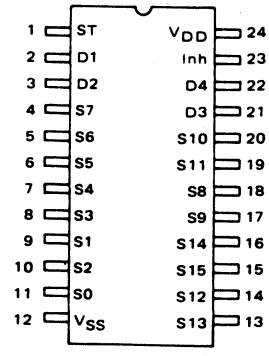


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

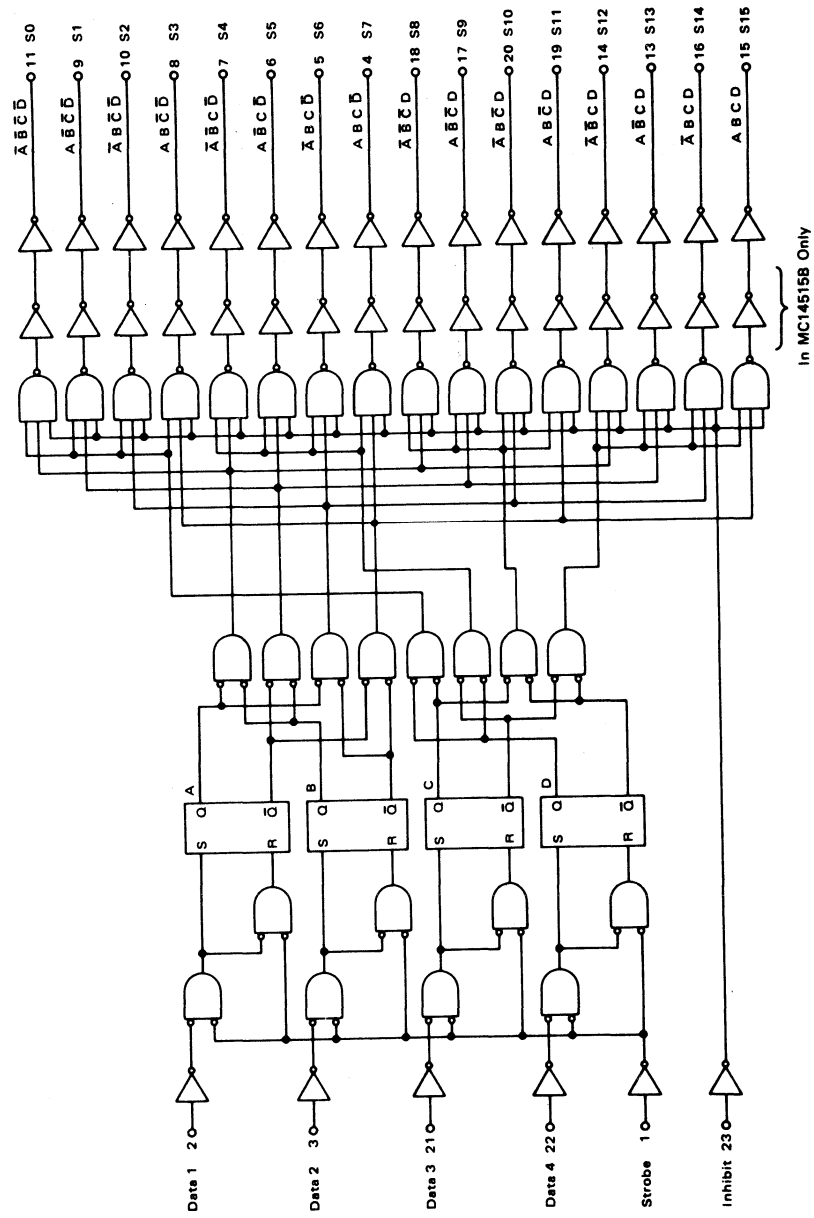


6

PIN ASSIGNMENT



LOGIC DIAGRAM



6

COMPLEX DATA ROUTING

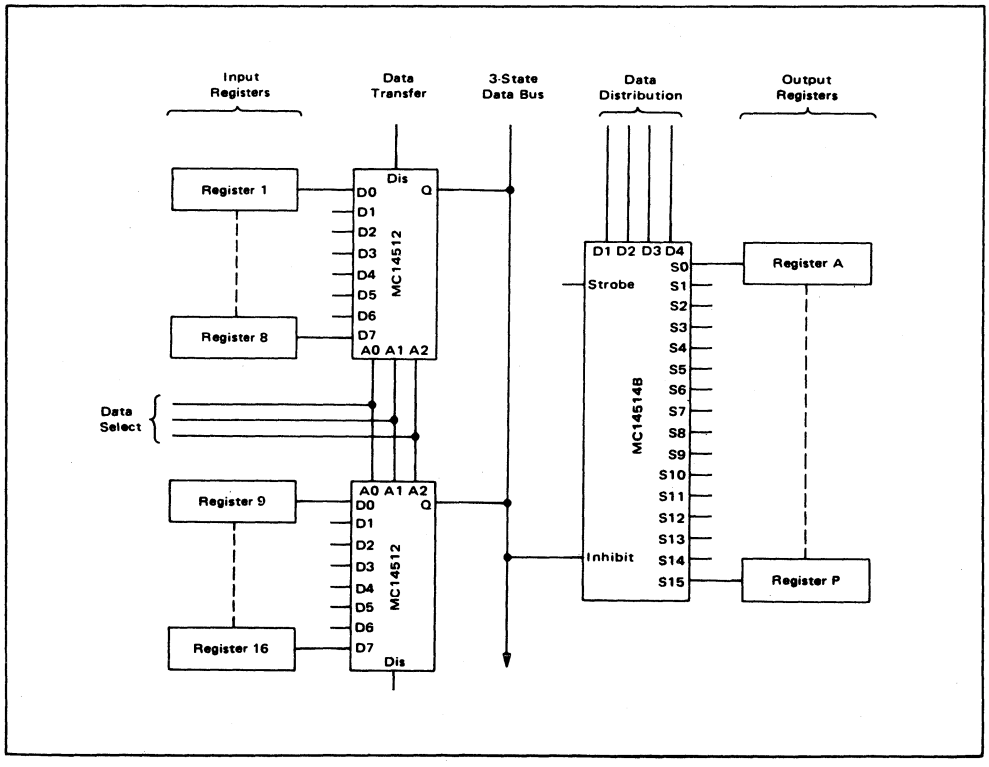
Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



MOTOROLA

MC14516B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY UP/DOWN COUNTER

BINARY UP/DOWN COUNTER

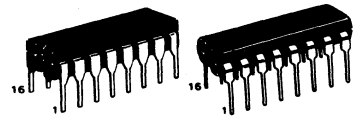
The MC14516B synchronous up/down binary counter is constructed with MOS P-channel and N-channel enhancement mode deivces in a monolithic structure.

This counter can be preset by applying the desired value, in binary, to the Preset inputs (P0, P1, P2, P3) and then bringing the Preset Enable (PE) high. The direction of counting is controlled by applying a high (for up counting) or a low (for down counting) to the UP/DOWN input. The state of the counter changes on the positive transition of the clock input.

Cascading can be accomplished by connecting the $\overline{\text{Carry Out}}$ to the $\overline{\text{Carry In}}$ of the next stage while clocking each counter in parallel. The outputs (Q0, Q1, Q2, Q3) can be reset to a low state by applying a high to the reset (R) pin.

This CMOS counter finds primary use in up/down and difference counting. Other applications include: (1) Frequency synthesizer applications where low power dissipation and/or high noise immunity is desired, (2) Analog-to-digital and digital-to-analog conversions, and (3) Magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

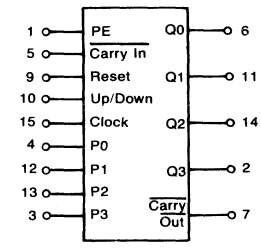
C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Reset	Clock	Action
1	X	0	0	X	No Count
0	1	0	0	⎍	Count Up
0	0	0	0	⎍	Count Down
X	X	1	0	X	Preset
X	X	X	1	X	Reset

X = Don't Care

Note: When counting up, the $\overline{\text{Carry Out}}$ signal is normally high and is low only when Q0 through Q3 are high and $\overline{\text{Carry In}}$ is low. When counting down, $\overline{\text{Carry Out}}$ is low only when Q0 through Q3 and $\overline{\text{Carry In}}$ are low.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

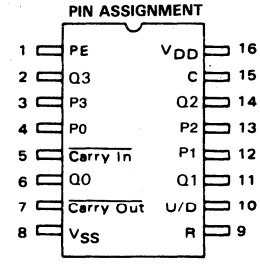
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

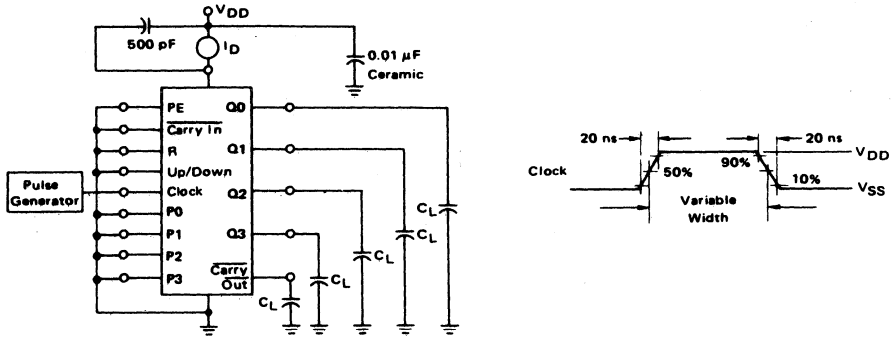
Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ #	All Types Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	—	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	60	120	
Preset or Reset to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	—	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	—	100	200	
Preset or Reset to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	—	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	—	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	—	150	300	
Reset Pulse Width	t_w	5.0	380	190	—	ns
		10	200	100	—	
		15	160	80	—	
Clock Pulse Width	t_{WH}	5.0	350	200	—	ns
		10	170	100	—	
		15	140	75	—	
Clock Pulse Frequency	f_{cl}	5.0	—	3.0	1.5	MHz
		10	—	6.0	3.0	
		15	—	8.0	4.0	
Preset or Reset Removal Time	t_{rem}	5.0	650	325	—	ns
The Preset or Reset signal must be low prior to a positive-going transition of the clock.		10	230	115	—	
		15	180	90	—	
Clock Rise and Fall Time	t_{TLH},	5.0	—	—	15	μs
	t_{THL}	10	—	—	5	
		15	—	—	4	
Setup Time	t_{su}	5.0	260	130	—	ns
$\overline{\text{Carry In}}$ to Clock		10	120	60	—	
		15	100	50	—	
Hold Time	t_h	5.0	0	−60	—	ns
Clock to $\overline{\text{Carry In}}$		10	20	−20	—	
		15	20	0	—	
Setup Time	t_{su}	5.0	500	250	—	ns
Up/Down to Clock		10	200	100	—	
		15	150	75	—	
Hold Time	t_h	5.0	−70	−160	—	ns
Clock to Up/Down		10	−10	−60	—	
		15	0	−40	—	
Setup Time	t_{su}	5.0	−40	−120	—	ns
Pn to PE		10	−30	−70	—	
		15	−25	−50	—	
Hold Time	t_h	5.0	480	240	—	ns
PE to Pn		10	420	210	—	
		15	420	210	—	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	—	ns
		10	100	50	—	
		15	80	40	—	

*The formulas given are for the typical characteristics only at 25°C.

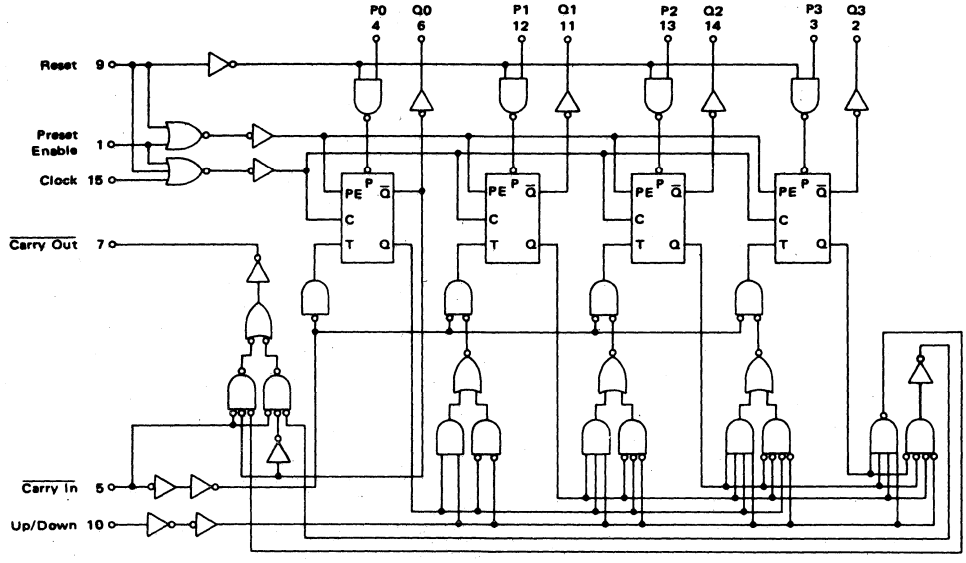
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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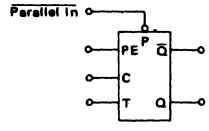
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



TOGGLE FLIP-FLOP

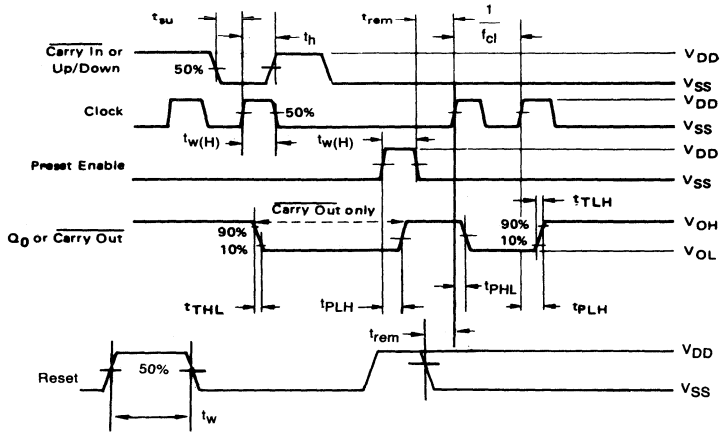


FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	T	Q_{n+1}
1	X	X	Parallel In
0	⌐⌐	0	Q_n
0	⌐⌐	1	$\overline{Q}_n$
0	⌐⌐	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS



PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3, Preset Inputs (Pins 4, 12, 13, 3) — Data on these inputs is loaded into the counter when PE is taken high.

Carry In, (Pin 5) — This active-low input is used when cascading stages. Carry In is usually connected to Carry Out of the previous stage. While high, Clock is inhibited.

Clock, (Pin 15) — Binary data is incremented or decremented, depending on the direction of count, on the positive transition of this input.

OUTPUTS

Q0, Q1, Q2, Q3, Binary outputs (Pins 6, 11, 14, 2) — Binary data is present on these outputs with Q0 corresponding to the least significant bit.

Carry Out, (Pin 7) — Used when cascading stages, Carry Out is usually connected to Carry In of the next stage. This synchronous output is active low and may also be used to indicate terminal count.

CONTROLS

PE, Preset Enable, (Pin 1) — Asynchronously loads data on the Preset Inputs. This pin is active high and inhibits the clock when high.

R, Reset, (Pin 9) — Asynchronously resets the Q outputs to a low state. This pin is active high and inhibits the clock when high.

Up/Down, (Pin 10) — Controls the direction of count, high for up count, low for down count.

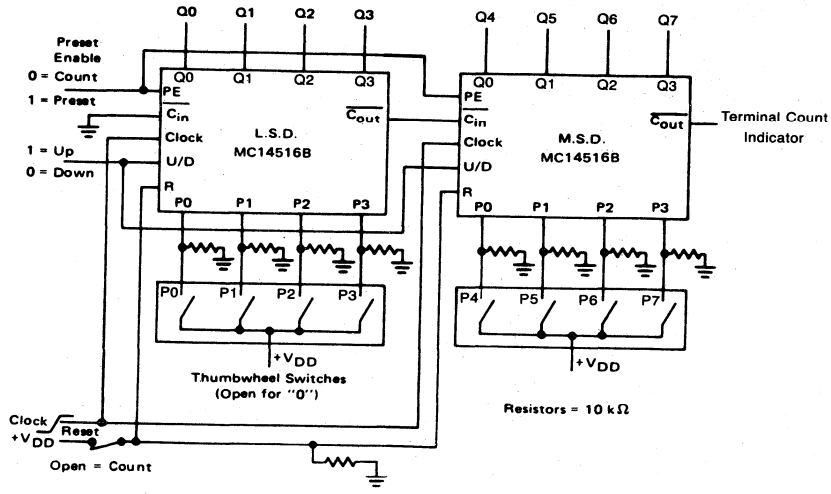
SUPPLY PINS

V_{SS}, Negative Supply Voltage, (Pin 8) — This pin is usually connected to ground.

V_{DD}, Positive Supply Voltage, (Pin 16) — This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

6

FIGURE 3 — PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER



Note: The Least Significant Digit (L.S.D.) counts from a preset value once Preset Enable (PE) goes low. The Most Significant Digit (M.S.D.) is disabled while $\overline{C_{in}}$ is high. When the count of the L.S.D. reaches 0 (count down mode) or reaches 15 (count up mode), $\overline{C_{out}}$ goes low for one complete clock cycle, thus allowing the next counter to decrement/increment one count. (See Timing Diagram) The L.S.D. now counts through another cycle (15 clock pulses) and the above cycle is repeated.

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TIMING DIAGRAM FOR THE PRESETTABLE CASCADED 8-BIT UP/DOWN COUNTER

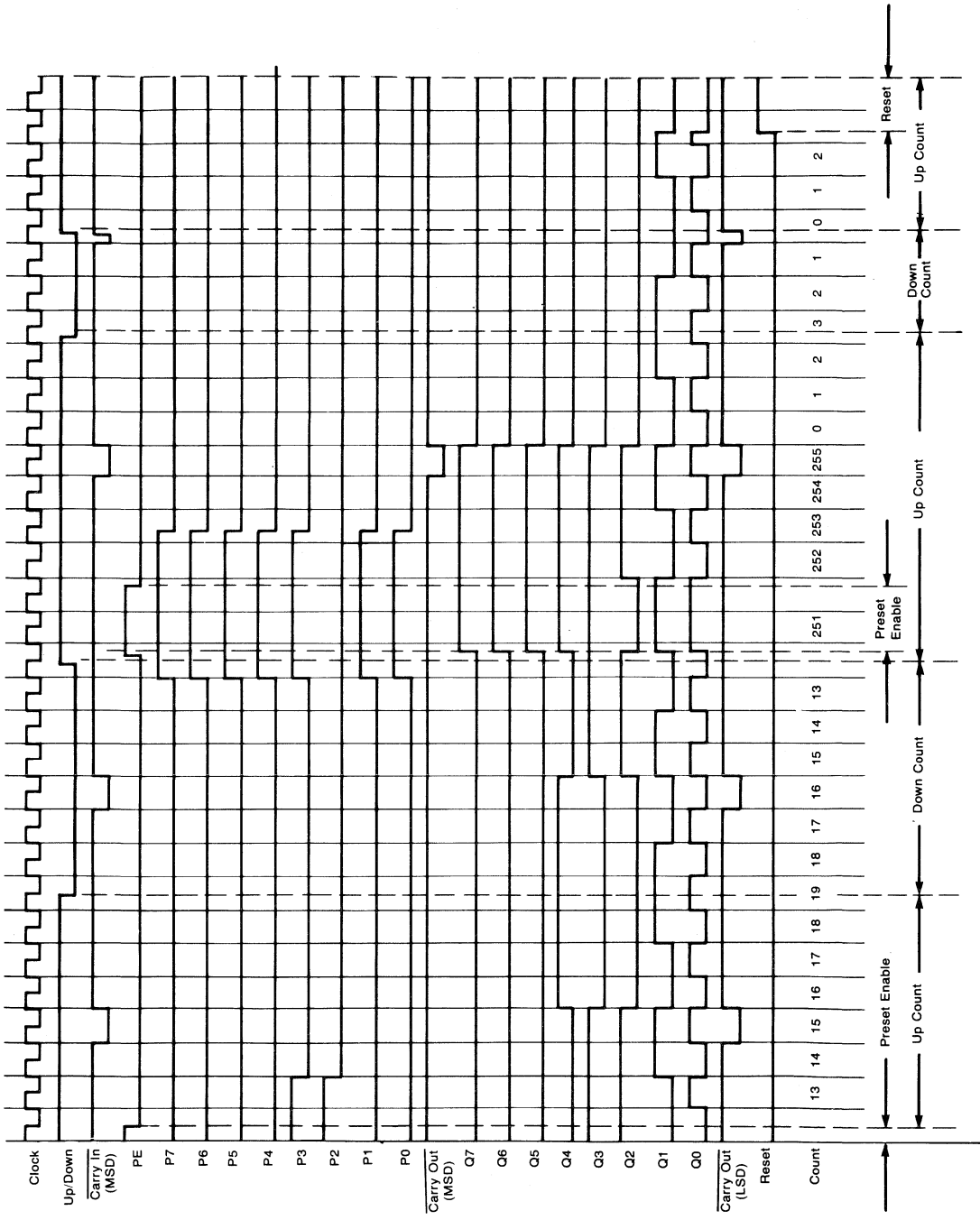
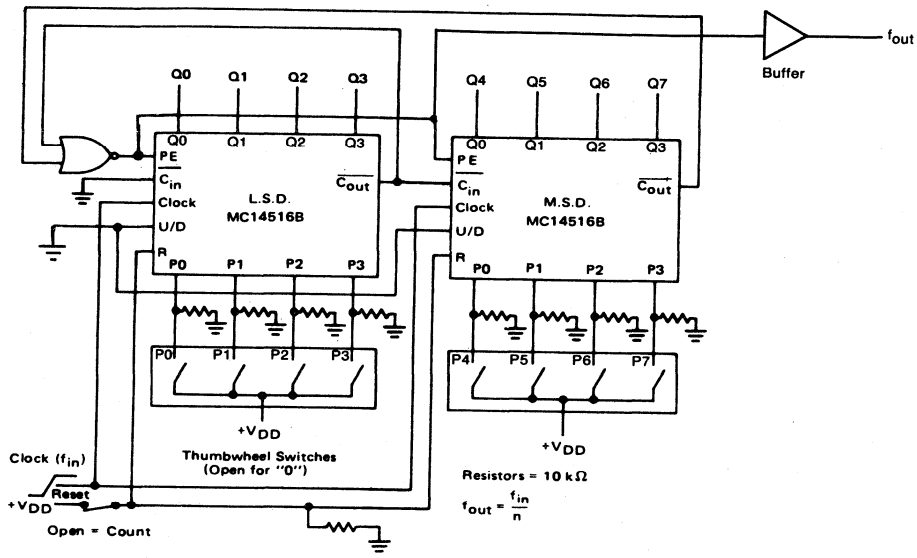


FIGURE 4 — PROGRAMMABLE CASCADED FREQUENCY DIVIDER



Note: The programmable frequency divider can be set by applying the desired divide ratio, in binary, to the preset inputs. For example, the maximum divide ratio of 255 may be obtained by applying a 1111 1111 to the preset inputs P0 to P7. For this divide operation, both counters should be configured in the count down mode. The divide ratio of zero is an undefined state and should be avoided.

6

MOTOROLA

MC14517B

CMOS LSI

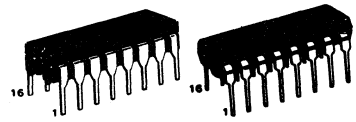
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

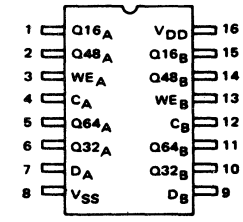
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⌐	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⌐	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
¬	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
¬	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (8.8 μA/kHz) f + I_{DD}							
		15	I_T = (13.7 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns	t_{PHL}	5.0	–	475	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	215	
Clock Pulse Width	t_{WH}	5.0	330	170	–	ns
		10	125	75	–	
		15	100	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.7	4.0	
		15	–	8.3	5.3	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0				–
		10		**See Note		
		15				
Data to Clock Setup Time	t_{su}	5.0	0	-40	–	ns
		10	10	-15	–	
		15	15	0	–	
Data to Clock Hold Time	t_h	5.0	150	75	–	ns
		10	75	25	–	
		15	35	10	–	
Write Enable to Clock Setup Time	t_{su}	5.0	400	170	–	ns
		10	200	65	–	
		15	110	50	–	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	–	ns
		10	180	55	–	
		15	100	40	–	

* The formulas given are for the typical characteristics only at 25°C.
\# Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
** When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

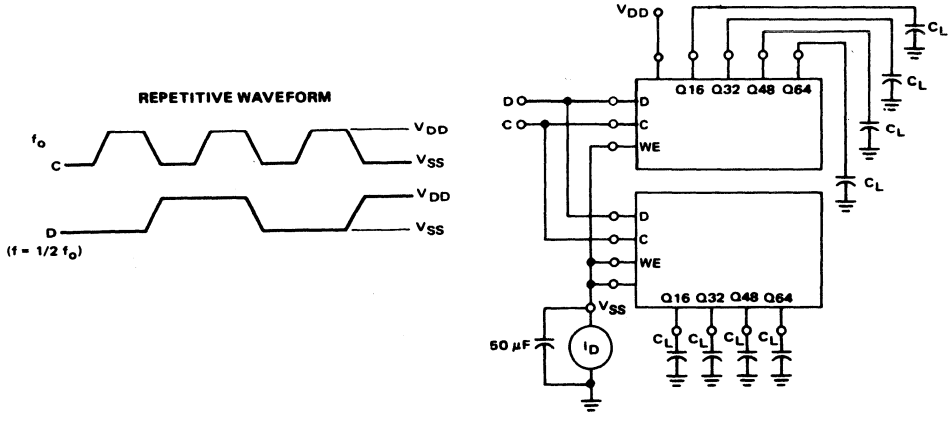
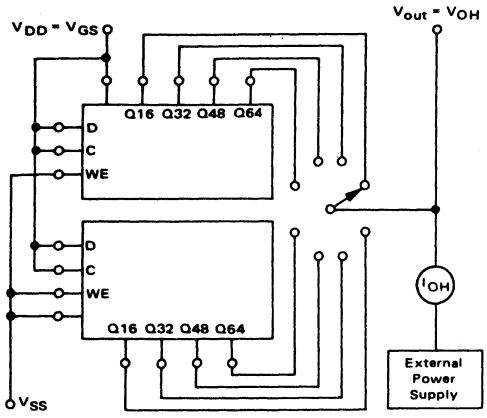
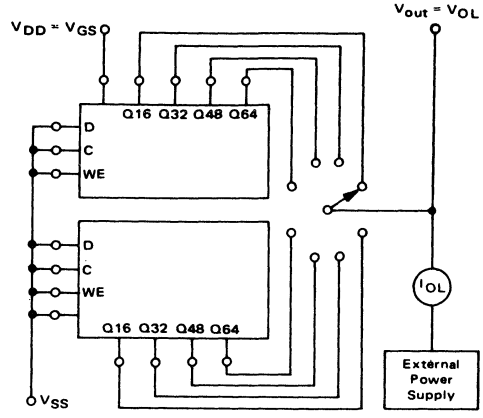


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



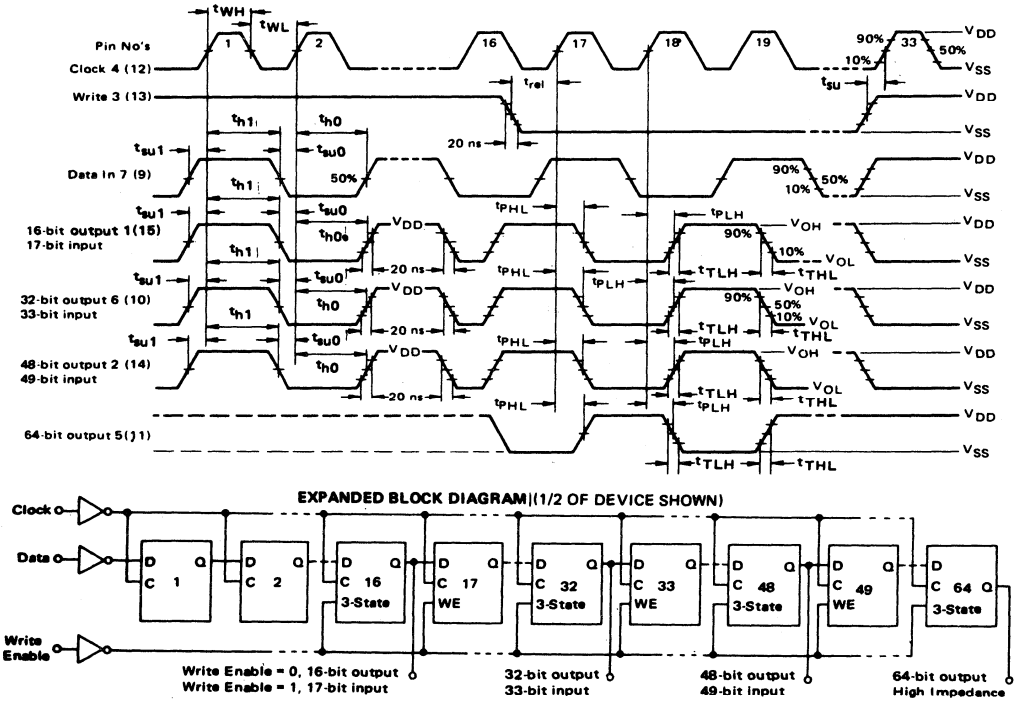
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)

MOTOROLA

MC14518B
MC14520B

CMOS MSI

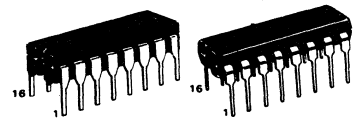
(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

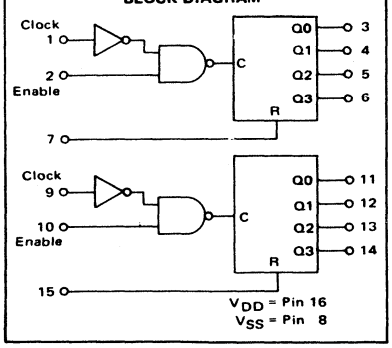
C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

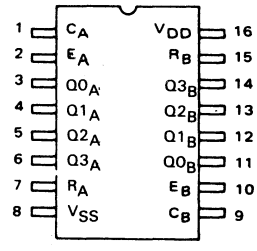
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



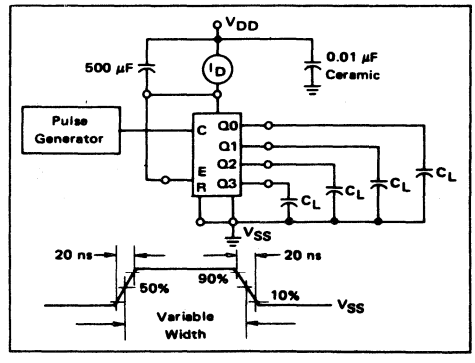
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q/Enable to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	660	
t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	230	
t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	–	90	170	
Clock Pulse Width	$t_{w(H)}$	5.0	200	100	–	ns
	$t_{w(L)}$	10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	
		15	140	70	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	125	–	ns
		10	120	55	–	
		15	90	40	–	
Reset Removal Time	t_{rem}	5.0	−5	−45	–	ns
		10	15	−15	–	
		15	20	−5	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



6

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

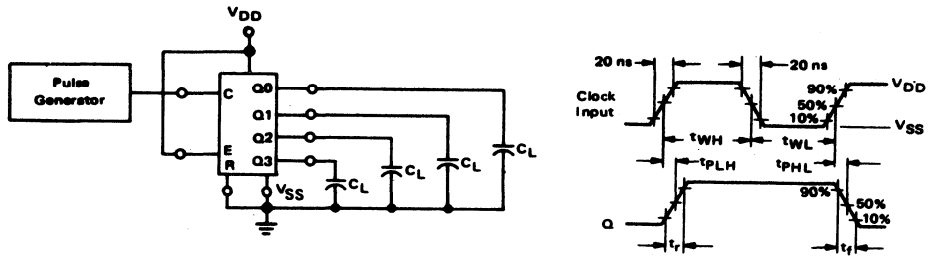


FIGURE 3 – TIMING DIAGRAM

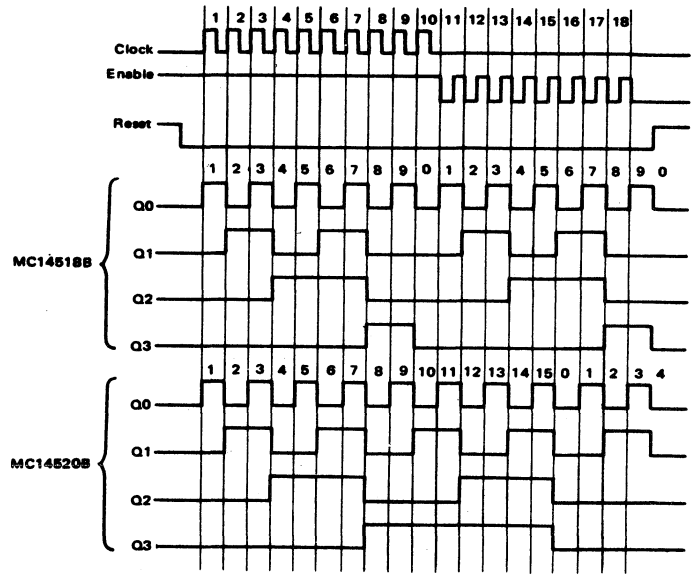


FIGURE 4 – DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

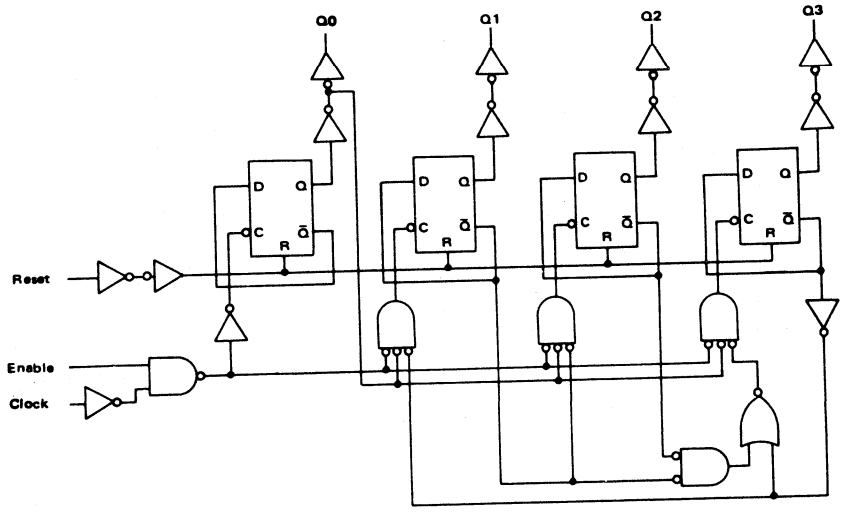
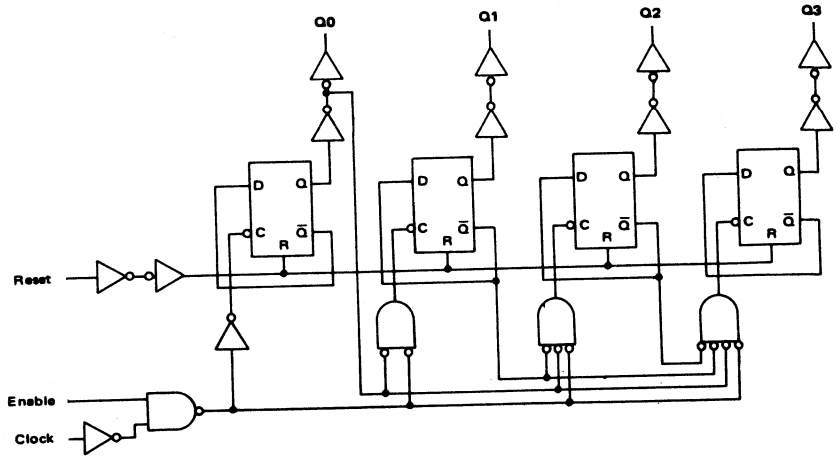


FIGURE 5 – BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



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MOTOROLA

MC14519B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

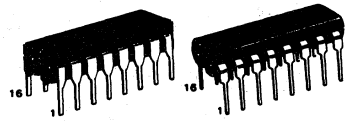
4-BIT AND/OR SELECTOR

4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications



L SUFFIX
CERAMIC PACKAGE
CASE 620

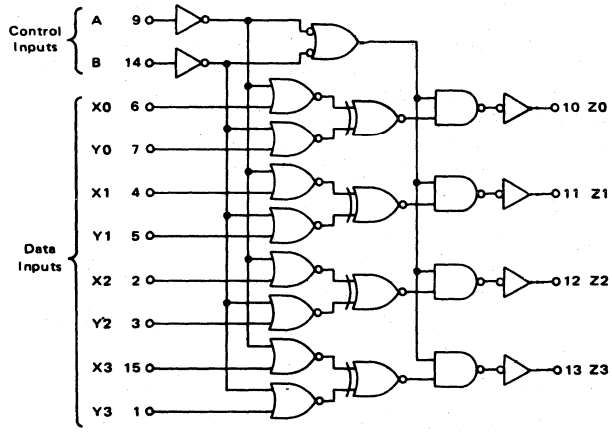
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

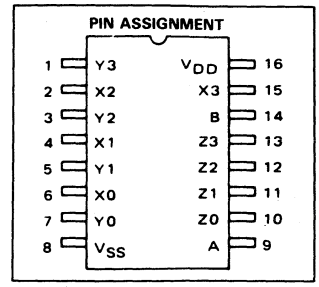
Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, 40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 hs	t_{PHL}	5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82		10	–	115	225	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	165	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

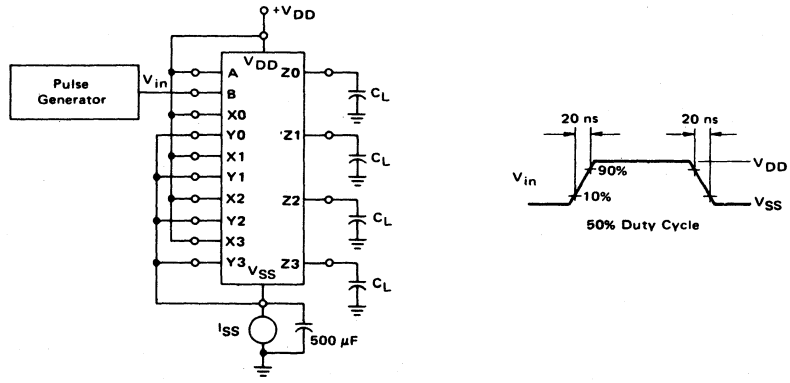
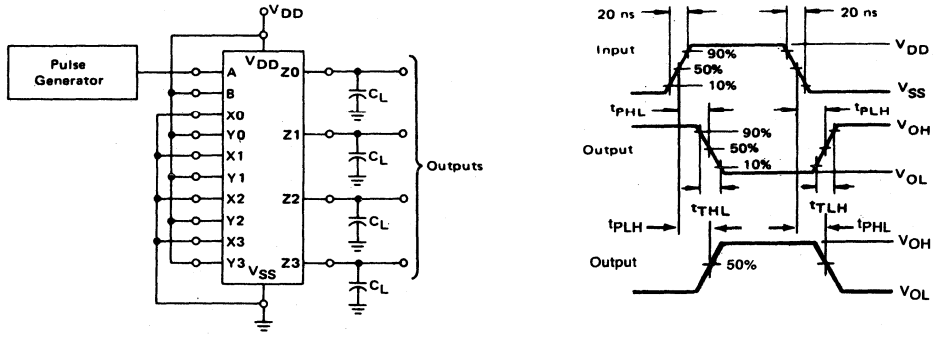
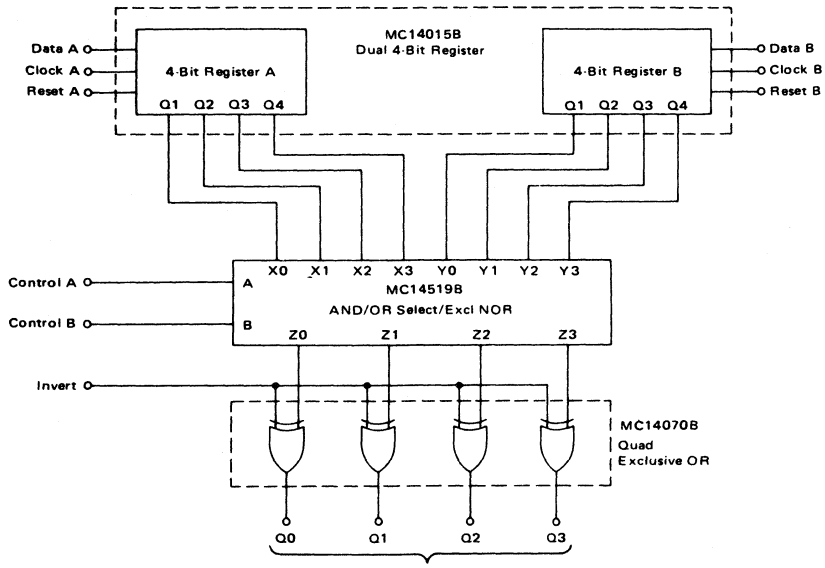


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14520B

FOR COMPLETE DATA
SEE MC14518B

DUAL BINARY UP COUNTER

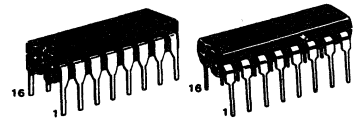
The MC14520B dual binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure. The device consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. The counter can be cleared by applying a high level on the Reset line. This complementary MOS up counter finds primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY UP COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: –55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

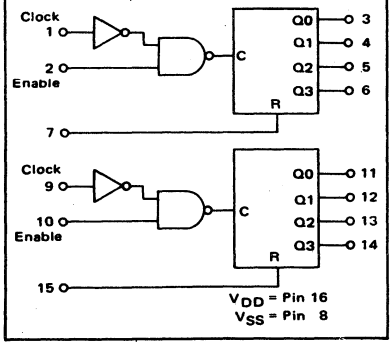
C Series: –40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	–0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: –12mW/°C from 65°C to 85°C
Ceramic "L" Package: –12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

MOTOROLA

MC14521B

CMOS MSI

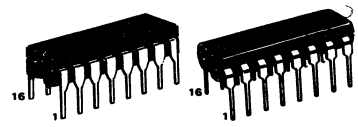
(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER

24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

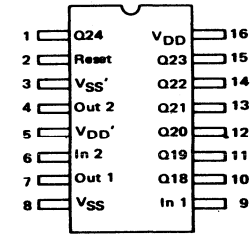
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

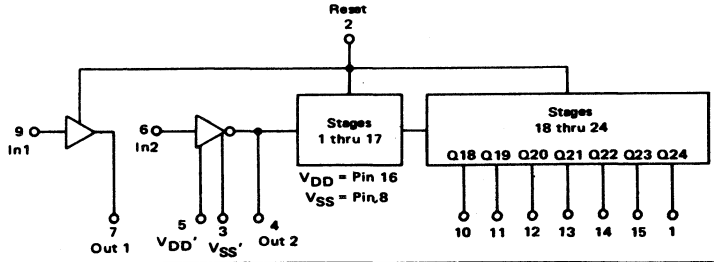
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

PIN ASSIGNMENT



BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.5	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 7		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pins 1, 10,		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc) 11, 12, 13, 14		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc) and 15		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 7		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pins 1, 10,		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc) 11, 12, 13, 14		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc) and 15		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	± 0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	± 0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.4 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time (Counter Outputs)	t_{PLH}, t_{PHL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					μs
Clock to Q18						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	–	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	–	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	–	1.3	2.7	
Clock to Q24						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	–	2.2	4.5	
t_{PHL}, t_{PHL} = (0.5 ns/pF) C_L + 1675 ns		15	–	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	–	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	–	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	–	ns
		10	150	55	–	
		15	120	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.0	MHz
		10	–	9.0	5.0	
		15	–	12	6.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	–	ns
		10	600	300	–	
		15	450	225	–	
Reset Removal Time	t_{rem}	5.0	30	−200	—	ns
		10	0	−160	—	
		15	−40	−110	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

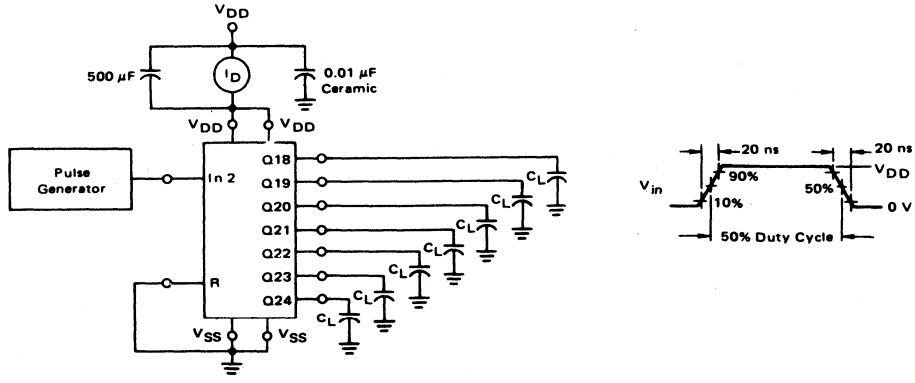


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

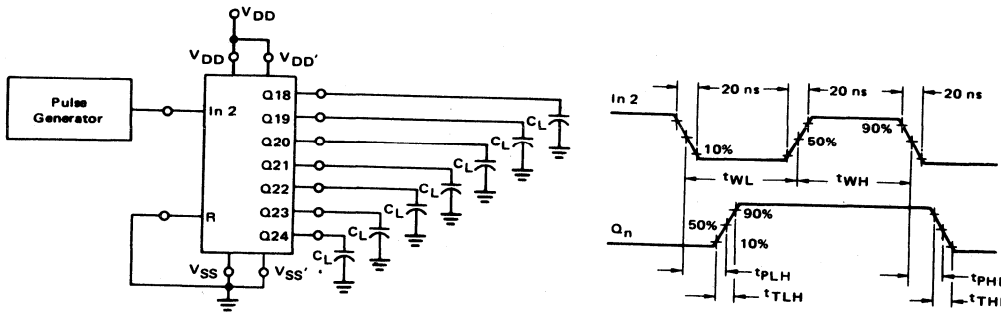
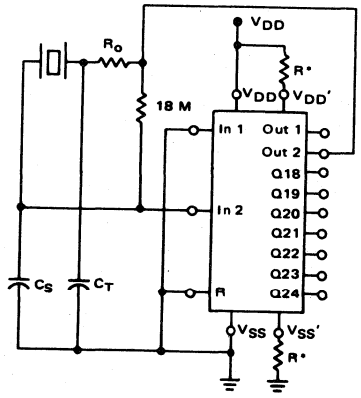


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.
10 kΩ ≤ R ≤ 70 kΩ

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

6

FIGURE 5 – RC OSCILLATOR STABILITY

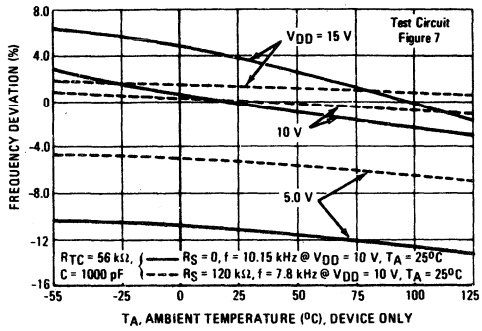


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

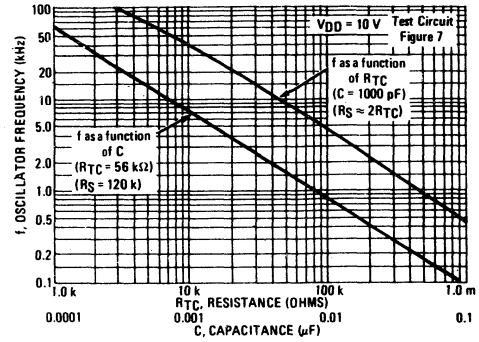


FIGURE 7 – RC OSCILLATOR CIRCUIT

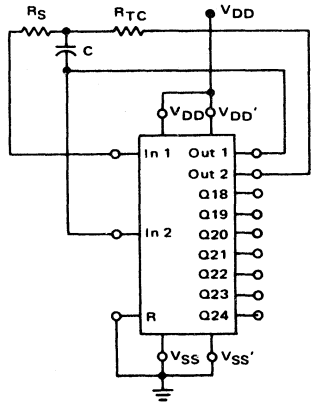
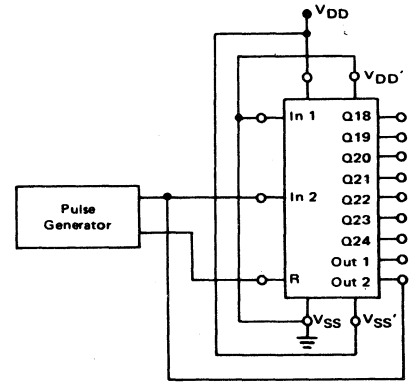


FIGURE 8 – FUNCTIONAL TEST CIRCUIT



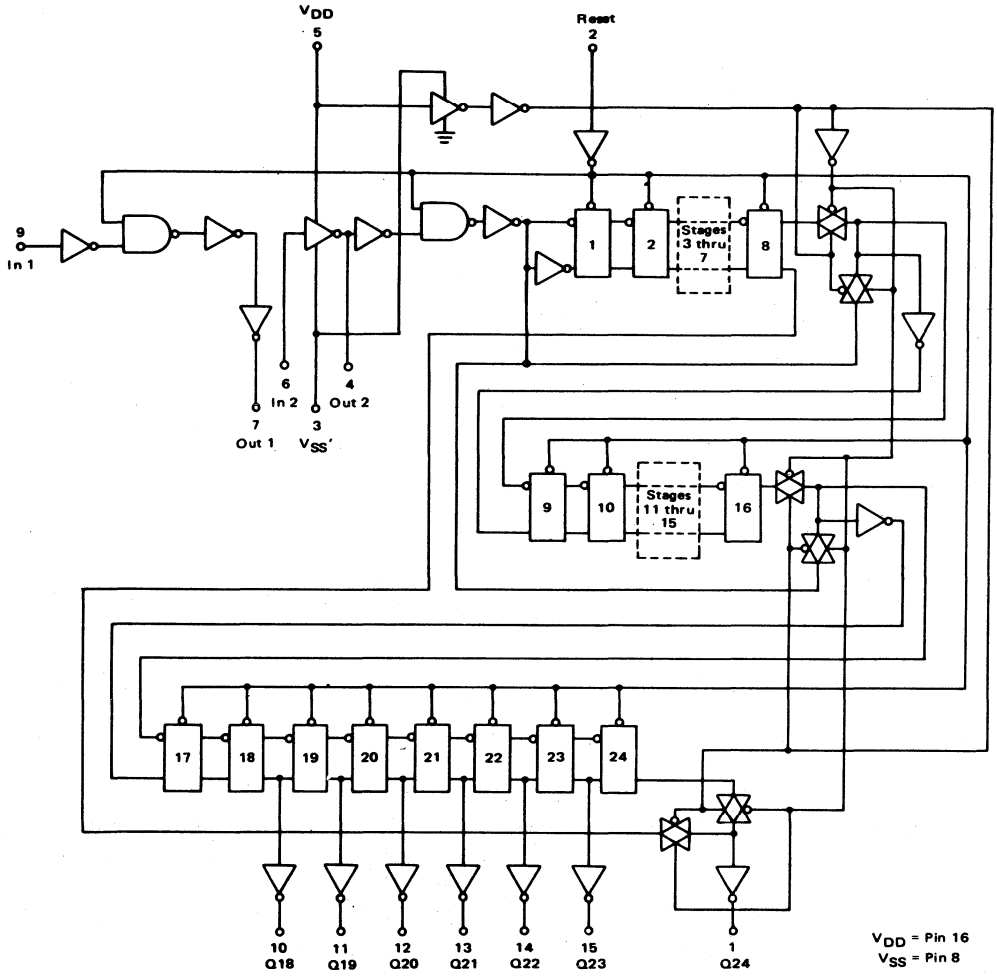
FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode. Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1				
	–	–				
	–	–				
	–	–				
	1	1			1	The 255th "0" to "1" transition.
	0	0			1	
	0	0	Gnd		1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1	0			1	Out 2 converts back to an output.
	0	1			0	Counter ripples from an all "1" state to an all "0" stage.

6

LOGIC DIAGRAM



MOTOROLA

MC14522B
MC14526B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE 4-BIT DOWN COUNTERS

BCD – MC14522B
Binary – MC14526B

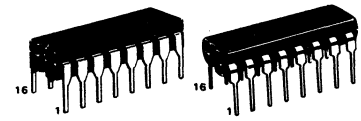
PRESETTABLE 4-BIT DOWN COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a monolithic structure.

These devices are presettable, cascadable, synchronous down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Inhibit input allows disabling of the pulse counting function. Inhibit may also be used as a negative edge clock.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Inhibit
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

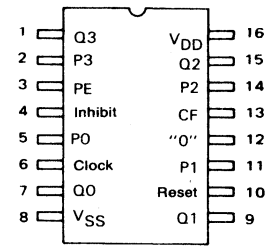
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Output	Resulting Function
Clock	Reset	Inhibit	Preset Enable	Cascade Feedback	"0"	
X	H	X	L	L	L	Asynchronous reset*
X	H	X	H	L	H	Asynchronous reset
X	H	X	X	H	H	Asynchronous reset
X	L	X	H	X	L	Asynchronous preset
⌐	L	H	L	X	L	Decrement inhibited
L	L	⌐	L	X	L	Decrement inhibited
¬	L	L	L	L	L	No change** (inactive edge)
H	L	⌐	L	L	L	No change** (inactive edge)
⌐	L	L	L	L	L	Decrement**
H	L	¬	L	L	L	Decrement**

X = Don't Care

Notes:
* Output "0" is low when reset goes high only if PE and CF are low.
** Output "0" is high when reset is low, only if CF is high and count is 0000.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0'	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.4 µA/kHz) f + I_{DD}							
		15	I_T = (5.1 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns	(Figures 4, 5)	10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time (Inhibit Used as Negative-Edge Clock)	t_{PLH},					ns
Clock or Inhibit to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	(Figures 4, 5, 6)	5.0	—	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	—	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	—	160	320	
Clock or Inhibit to "0"						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns		5.0	—	240	480	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	100	200	
Propagation Delay Time	t_{PLH},	5.0	—	260	520	ns
Pn to Q	t_{PHL}	10	—	120	240	
	(Figures 4, 7)	15	—	100	200	
Propagation Delay Time	t_{PHL}	5.0	—	250	500	ns
Reset to Q		10	—	110	220	
	(Figure 8)	15	—	80	160	
Propagation Delay Time	t_{PHL},	5.0	—	220	440	ns
Preset Enable to "0"	t_{PLH}	10	—	100	200	
	(Figures 4, 9)	15	—	80	160	
Clock or Inhibit Pulse Width	t_w	5.0	250	125	—	ns
		10	100	50	—	
	(Figures 5, 6)	15	80	40	—	
Clock Pulse Frequency (with PE = low)	f_{max}	5.0	—	2.0	1.5	MHz
		10	—	5.0	3.0	
	(Figures 4, 5, 6)	15	—	6.6	4.0	
Clock or Inhibit Rise and Fall Time	t_r,	5.0	—	—	15	μs
	t_f	10	—	—	5	
	(Figures 5, 6)	15	—	—	4	
Setup Time	t_{su}	5.0	90	40	—	ns
Pn to Preset Enable		10	50	15	—	
	(Figure 10)	15	40	10	—	
Hold Time	t_h	5.0	30	−15	—	ns
Preset Enable to Pn		10	30	−5	—	
	(Figure 10)	15	30	0	—	
Preset Enable Pulse Width	t_w	5.0	250	125	—	ns
		10	100	50	—	
	(Figure 10)	15	80	40	—	
Reset Pulse Width	t_w	5.0	350	175	—	ns
		10	250	125	—	
	(Figure 8)	15	200	100	—	
Reset Removal Time	t_{rem}	5.0	10	−110	—	ns
		10	20	−30	—	
	(Figure 8)	15	30	−20	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

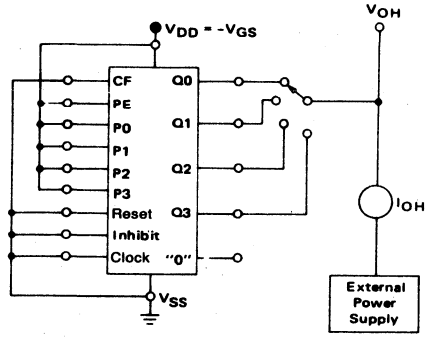


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

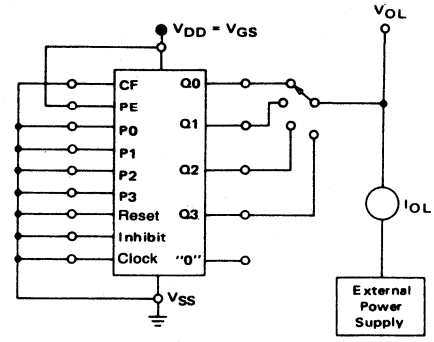


FIGURE 3 – POWER DISSIPATION

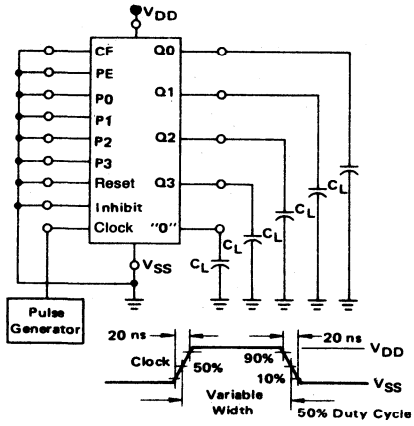
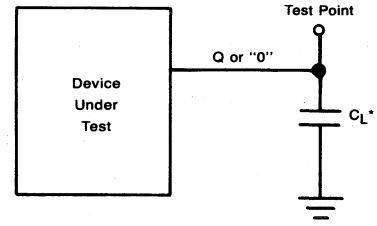


FIGURE 4 — TEST CIRCUIT



*Includes all probe and jig capacitance.

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SWITCHING WAVEFORMS

FIGURE 5

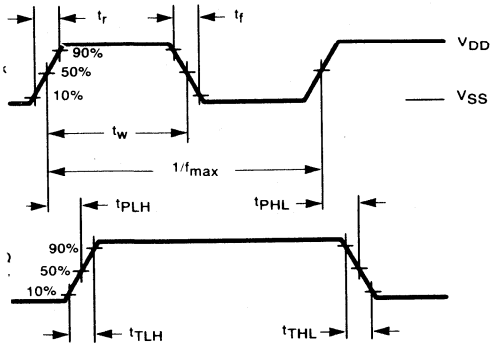


FIGURE 6

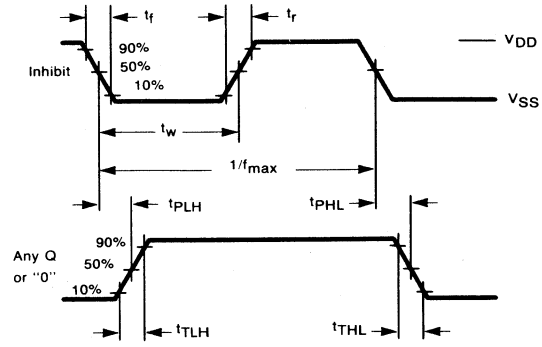


FIGURE 7

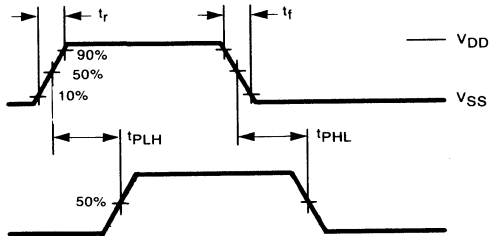


FIGURE 8

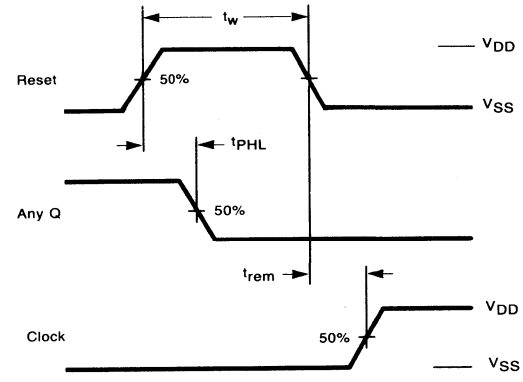


FIGURE 9

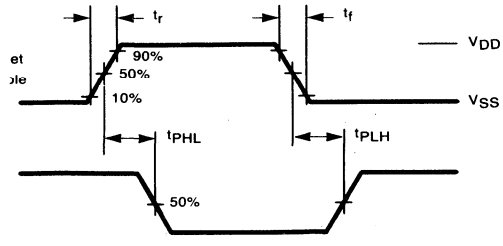
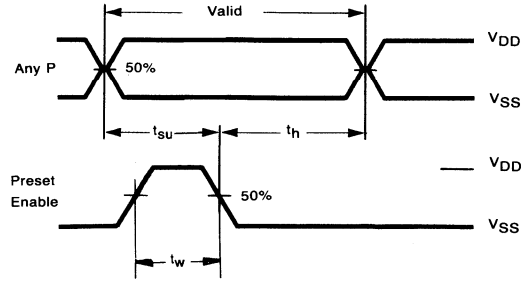


FIGURE 10



6

PIN DESCRIPTIONS

Preset Enable (Pin 3) — If Reset is low, a high level on the Preset Enable input asynchronously loads the counter with the programmed values on P0, P1, P2, and P3.

Inhibit (Pin 4) — A high level on the Inhibit input prevents the Clock from decrementing the counter. With Clock (pin 6) held high, Inhibit may be used as a negative edge clock input.

Clock (Pin 6) — The counter decrements by one for each rising edge of Clock. See the Function Table for level requirements on the other inputs.

Reset (Pin 10) — A high level on Reset asynchronously forces Q0, Q1, Q2, and Q3 low and, if Cascade Feedback is high, causes the "0" output to go high.

"0" (Pin 12) — The "0" (Zero) output issues a pulse one clock period wide when the counter reaches terminal count (Q0 = Q1 = Q2 = Q3 = low) if Cascade Feedback is high and Preset Enable is low. When presetting the counter to a value other than all zeroes, the "0" output is valid after the rising edge of Preset Enable (when Cascade Feedback is high). See the Function Table.

Cascade Feedback (Pin 13) — If the Cascade Feedback input is high, a high level is generated at the "0" output when the count is all zeroes. If Cascade Feedback is low, the "0" output depends on the Preset Enable input level. See the Function Table.

P0, P1, P2, P3 (Pins 5, 11, 14, 2) — These are the preset data inputs. P0 is the LSB.

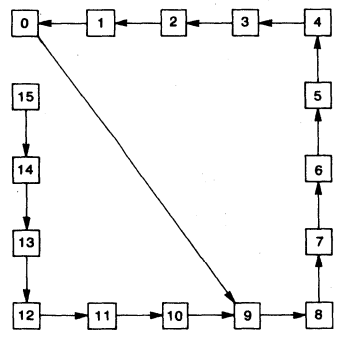
Q0, Q1, Q2, Q3 (Pins 7, 9, 15, 1) — These are the synchronous counter outputs. Q0 is the LSB.

V_{SS} (Pin 8) — The most negative power supply potential. This pin is usually ground.

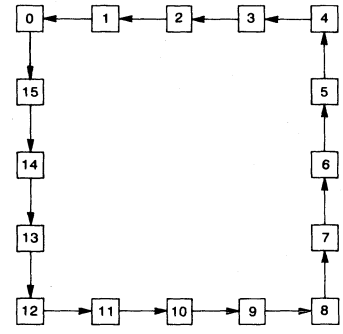
V_{DD} (Pin 16) — The most positive power supply potential. V_{DD} may range from 3 to 18 V with respect to V_{SS}.

STATE DIAGRAMS

MC14522B

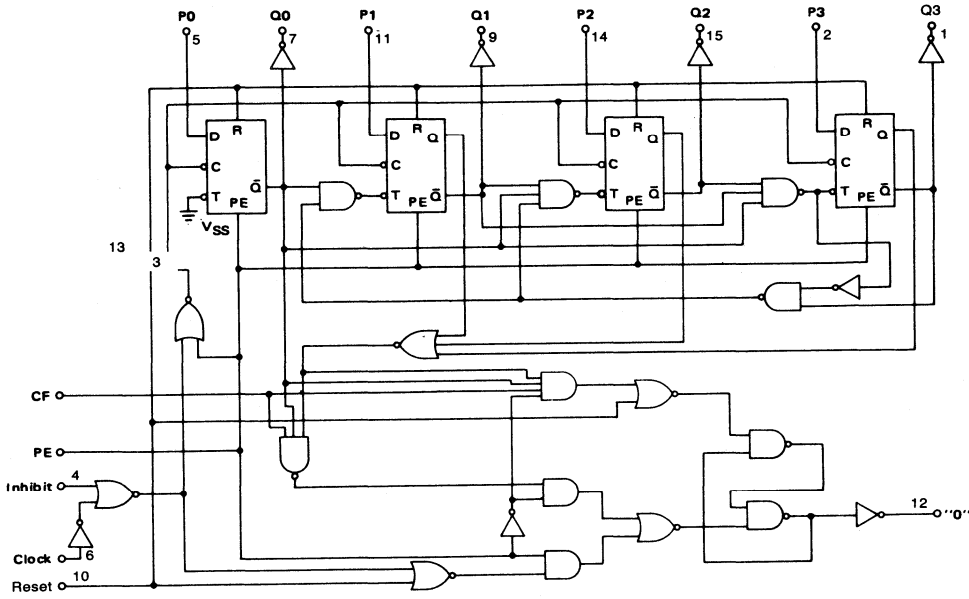


MC14526B

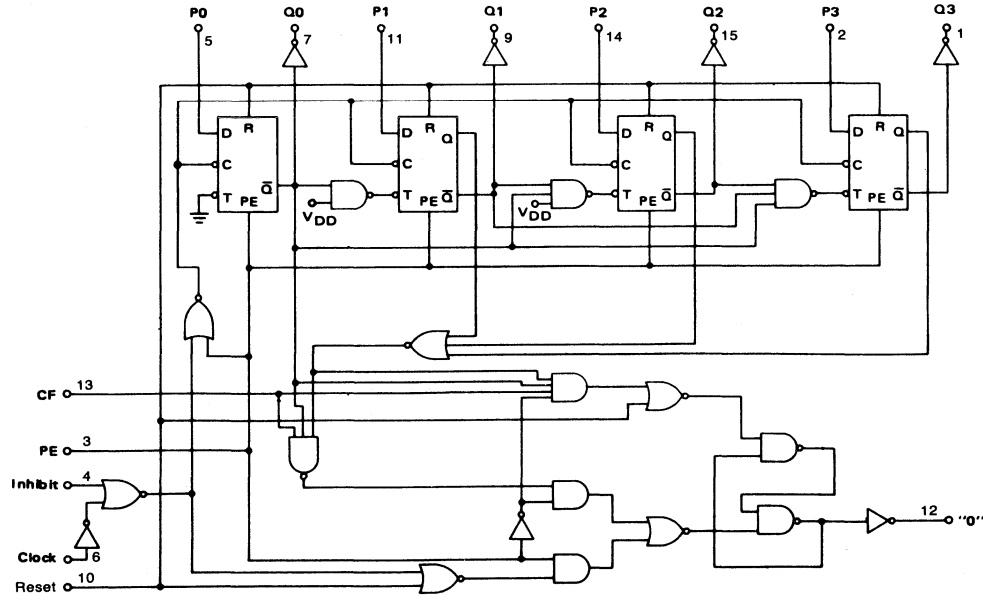


6

MC14522B LOGIC DIAGRAM (BCD Down Counter)



MC14526B LOGIC DIAGRAM (Binary Down Counter)



6

APPLICATIONS INFORMATION

Divide-By-N, Single Stage

Figure 11 shows a single stage divide-by-N application. The MC14522B (BCD version) can accept a number greater than 9 and count down in binary fashion. Hence, the BCD and binary single stage divide-by-N counters (as shown in Figure 11) function the same.

To initialize counting a number, N is set on the parallel inputs (P0, P1, P2, and P3) and reset is taken high asynchronously. A zero is forced into the master and slave of each bit and, at the same time, the "0" output goes high. Because Preset Enable is tied to the "0" output, preset is enabled. Reset must be released while the Clock is high so the slaves of each bit may receive N before the Clock goes low. When the Clock goes low and Reset is low, the "0" output goes low (if P0 through P3 are unequal to zero).

The counter downcounts with each rising edge of the Clock. When the counter reaches the zero state, an output pulse occurs on "0" which presets N. The propagation delays from the Clock's rising and falling edges to the "0" output's rising and falling edges are about equal, making the "0" output pulse approximately equal to that of the Clock pulse.

The Inhibit pin may be used to stop pulse counting. When this pin is taken high, decrementing is inhibited.

Cascaded, Presettable Divide-By-N

Figure 12 shows a three stage cascade application. Taking Reset high loads N. Only the first stage's Reset pin (least significant counter) must be taken high to cause the preset for all stages, but all pins could be tied together, as shown.

When the first stage's Reset pin goes high, the "0" output is latched in a high state. Reset must be released while Clock is high and time allowed for Preset Enable to load N into all stages before Clock goes low.

When Preset Enable is high and Clock is low, time must be allowed for the zero digits to propagate a Cascade Feedback to the first non-zero stage. Worst case is from the most significant bit (M.S.B.) to the L.S.B., when the L.S.B. is equal to one (i.e. N = 1).

After N is loaded, each stage counts down to zero with each rising edge of Clock. When any stage reaches zero and the leading stages (more significant bits) are zero, the "0" output goes high and feeds back to the preceding stage. When all stages are zero, the Preset Enable automatically loads N while the Clock is high and the cycle is renewed.

FIGURE 11 — ÷N COUNTER

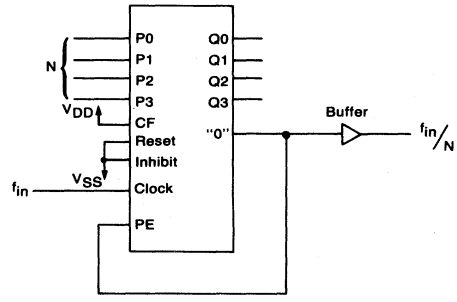
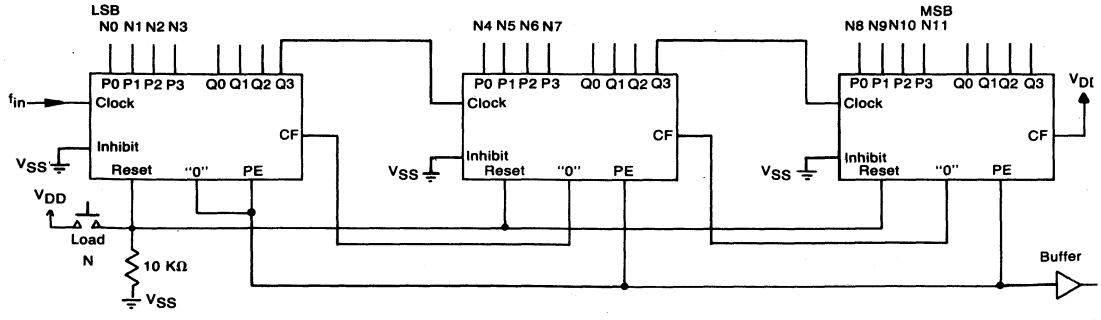


FIGURE 12 — 3 STAGES CASCADED



MOTOROLA

MC14527B

CMOS MSI

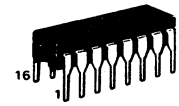
(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER

BCD RATE MULTIPLIER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

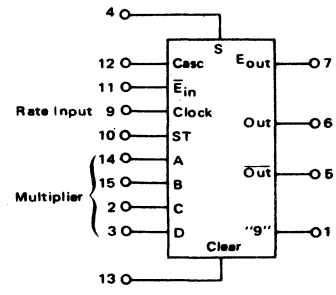
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUTS									OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D*	C	B	A	No. of Clock Pulses	$\overline{E}_{in}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	0	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	0	1	0	1	1	0
X	X	X	X	10	0	0	0	1	1	0	1	0	1

X = Don't Care
*D = Most Significant Bit

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.75 µA/kHz) f + I_{DD}							
		15	I_T = (2.6 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

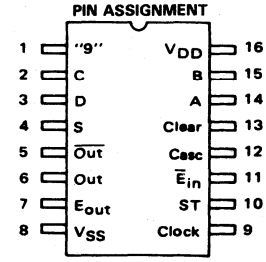
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0012.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PHL}, t_{PHL}					ns
Clock to Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock to $\overline{Out}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Clock to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 210 ns		5.0	–	295	590	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
Clock to "9"	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Set or Clear to Out	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	760	
t_{PHL} = (0.66 ns/pF) C_L + 132 ns		10	–	165	330	
t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Cascade to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Strobe to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 145 ns		5.0	–	230	260	
t_{PHL} = (0.66 ns/pF) C_L + 72 ns		10	–	105	210	
t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	200	110	–	
		15	150	80	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.2	MHz
		10	–	4.5	2.5	
		15	–	6.0	3.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Set or Clear Pulse Width	t_{WH}	5.0	240	80	–	ns
		10	100	35	–	
		15	75	30	–	
Set Removal Time	t_{rem}	5.0	0	-20	–	ns
		10	0	-10	–	
		15	0	-7.5	–	
$\overline{Enable\ In}$ Setup Time	t_{su}	5.0	400	175	–	ns
		10	150	60	–	
		15	120	45	–	

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

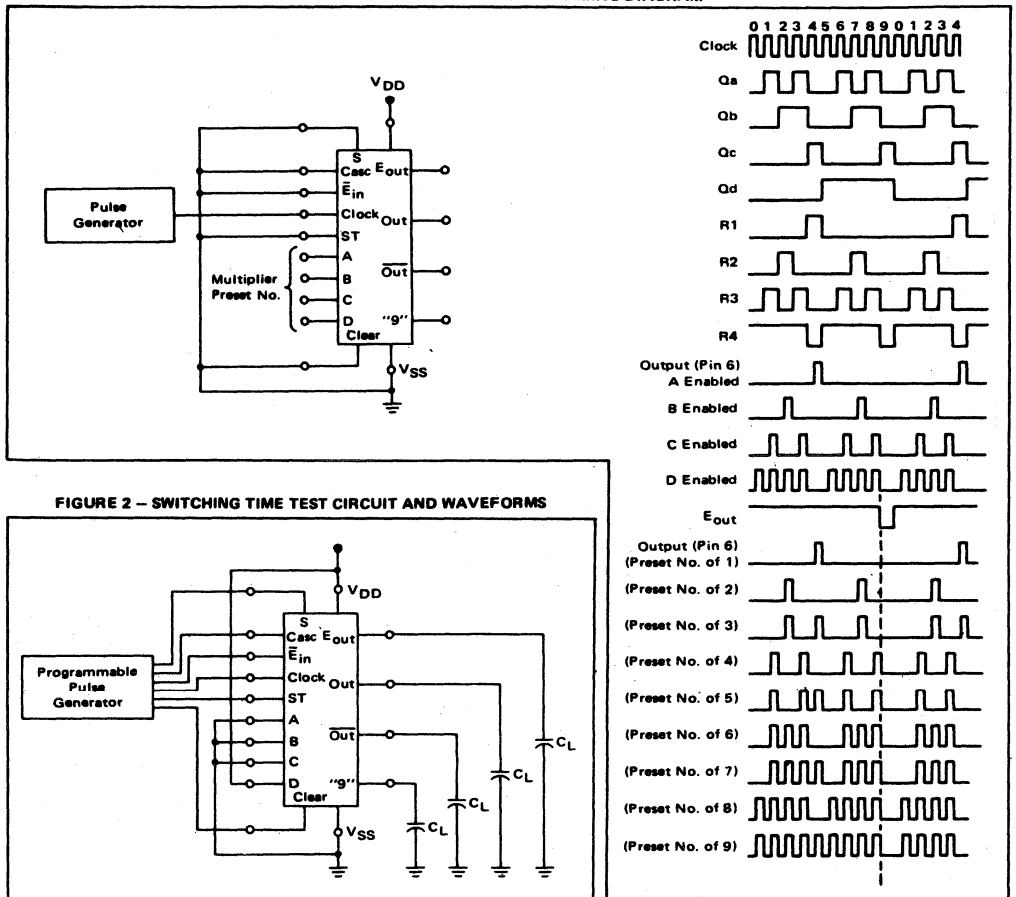
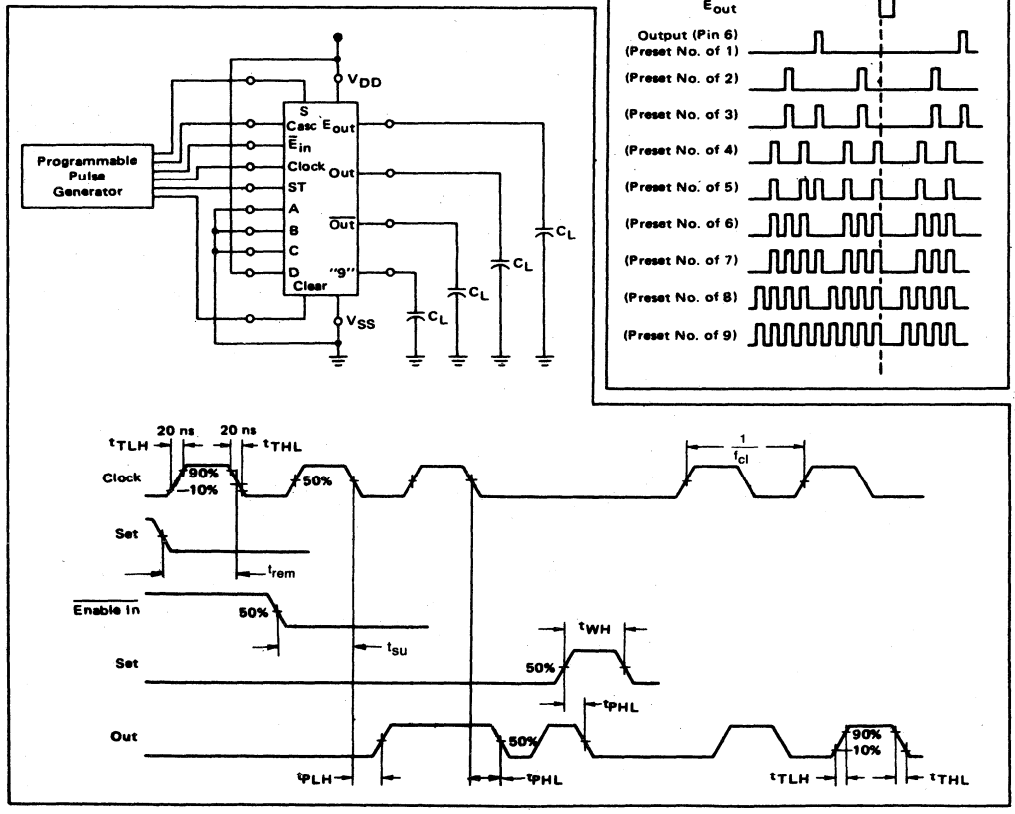
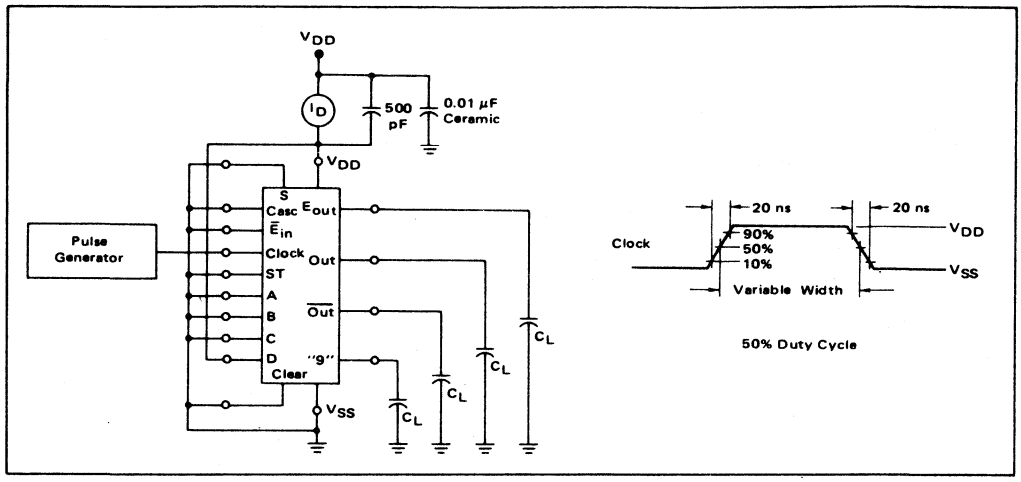


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

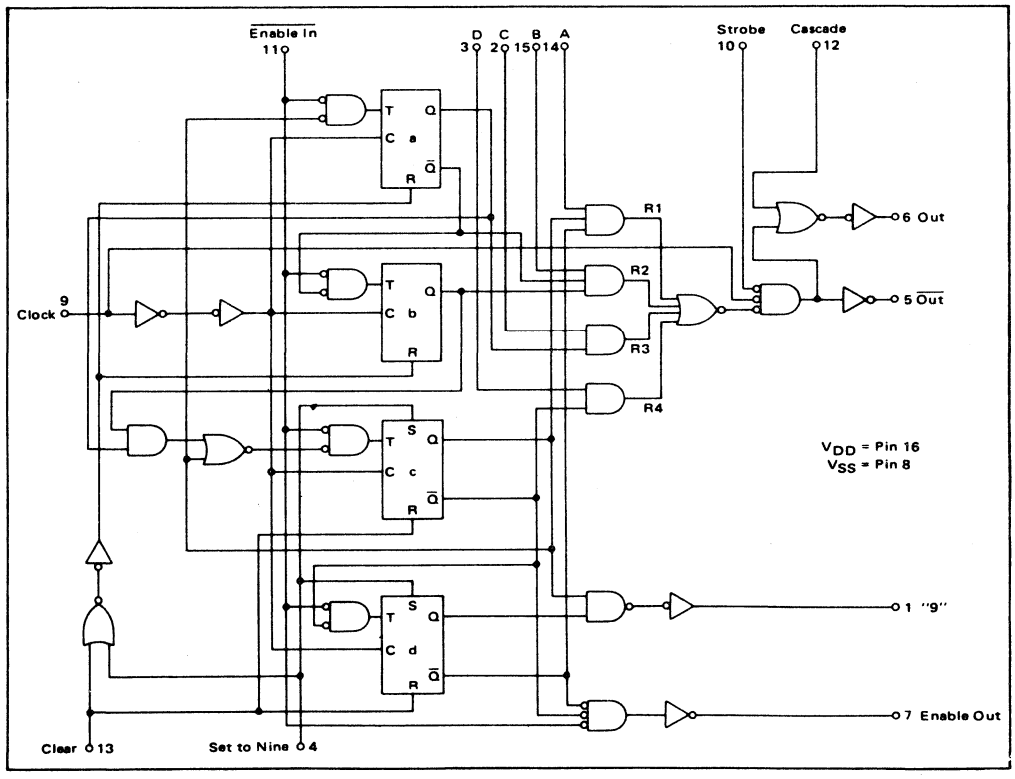


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FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

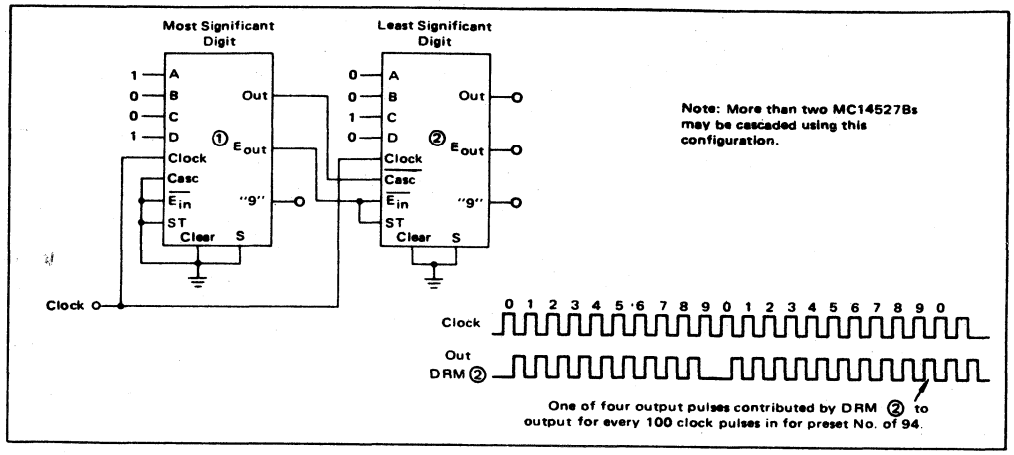


LOGIC DIAGRAM



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FIGURE 4 – TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94



MOTOROLA

MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

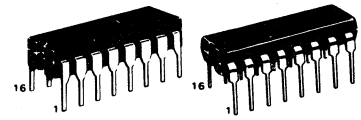
The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B and MC14548B.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

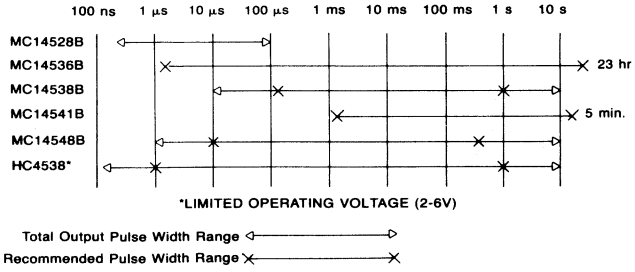
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

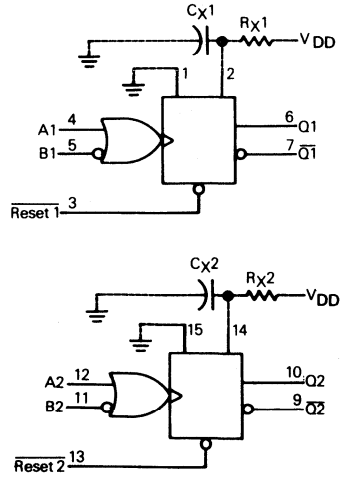
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

THE MC14528B IS
NOT RECOMMENDED FOR NEW DESIGNS

ONE-SHOT SELECTION GUIDE



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−0.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula –	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2x10^{-8} R_X C_X (V_{DD}-2)^2 f] \times 10^{-3}$ where: I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

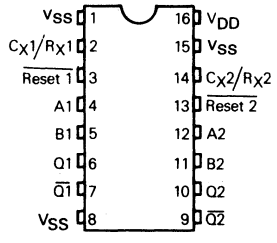
** The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}	–	–					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	–	40	80	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	–	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	–	90	180	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	–	705	–	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	–	290	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	–	210	–	
Input Pulse Width – A or B	t_{WH}	15	5.0	5.0	150	70	–	ns
				10	75	30	–	
				15	55	30	–	
	t_{WL}	1000	10	5.0	–	70	–	ns
				10	–	30	–	
				15	–	30	–	
Output Pulse Width – Q or $\overline{Q}$	t_W	15	5.0	5.0	–	550	–	ns
(For C_X < 0.01 μF use graph for appropriate V_{DD} level.)				10	–	350	–	
				15	–	300	–	
Output Pulse Width – Q or $\overline{Q}$	t_W	10,000	10	5.0	15	30	45	μs
(For C_X > 0.01 μF use formula:				10	10	50	90	
$t_W = 0.2\ R_X\ C_X\ \text{Ln}\ [V_{DD} - V_{SS}]$)†				15	15	55	95	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	–	6.0	25	%
				10	–	8.0	35	
				15	–	8.0	35	
Reset Propagation Delay — $\overline{\text{Reset}}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	–	325	600	ns
				10	–	90	225	
				15	–	60	170	
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	
				15	–	250	–	
Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
		1000	10	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
External Timing Resistance	R_X	–	–	–	5.0	–	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits *			μF

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.
* If C_X > 15 μF, Use Discharge Protection Diode D_X, per Fig. 9.

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{Q}$
H	⌐	H	⌐⌐	⌐⌐
H	L	⌐	⌐⌐	⌐⌐
H	⌐ ¬	L	Not Triggered	
H	H	⌐ ¬	Not Triggered	
H	L, H, ¬	H	Not Triggered	
H	L	L, H, ⌐	Not Triggered	
L	X	X	L	H
¬ ⌐	X	X	Not Triggered	

6

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

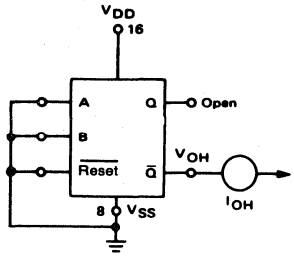


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

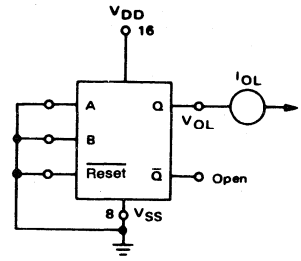
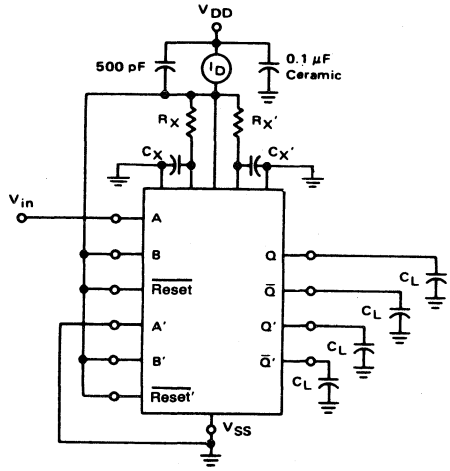
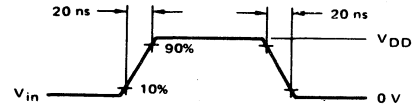


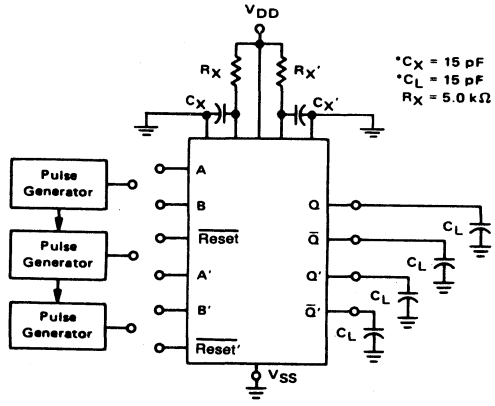
FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS





Duty Cycle = 50%

FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	Reset	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

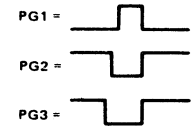


FIGURE 5 — AC TEST WAVEFORMS

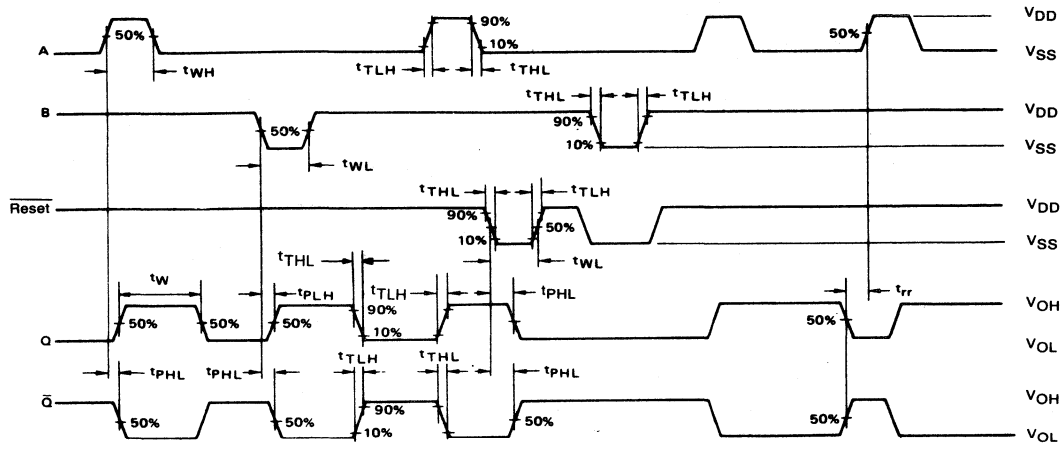
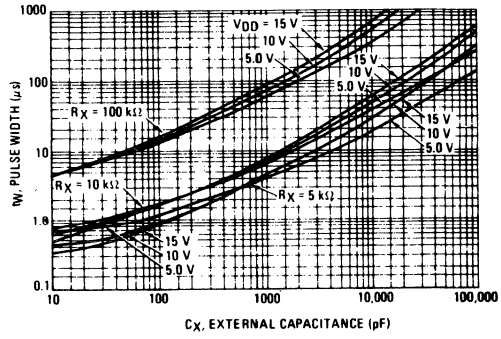


FIGURE 6 — PULSE WIDTH versus C_X



6

TYPICAL APPLICATIONS

FIGURE 7 — RETRIGGERABLE MONOSTABLES CIRCUITRY

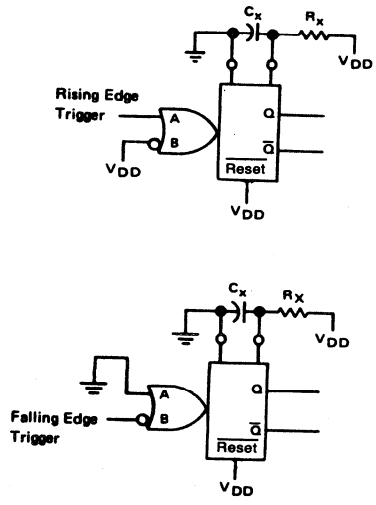


FIGURE 8 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

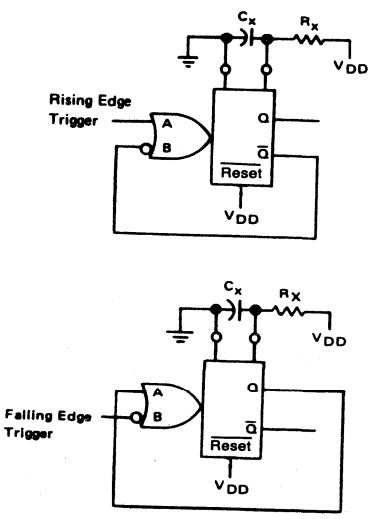


FIGURE 9 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE

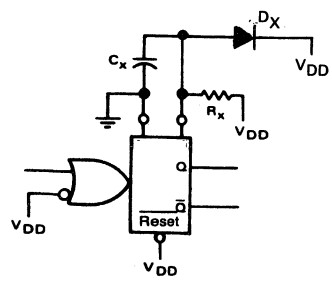
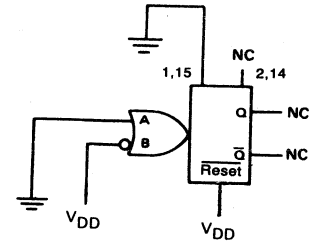


FIGURE 10 — CONNECTION OF UNUSED SECTIONS



6

MOTOROLA

MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

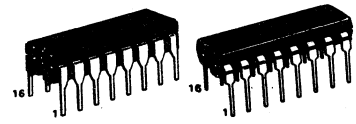
The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR OR 8-CHANNEL ANALOG DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

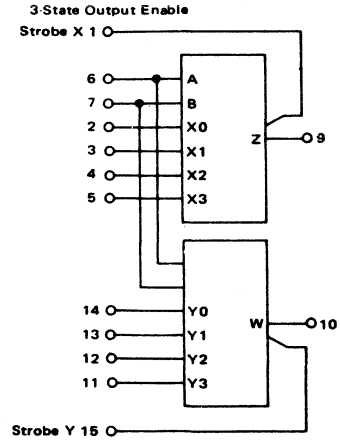
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance		

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	1	V_{OL}	0.0	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0					10	–	0.05	–	0	0.05	–	0.05	
					15	–	0.05	–	0	0.05	–	0.05	
	"1" Level		V_{OH}	0.0	5.0	4.95	–	4.95	5.0	–	4.95	–	
					10	9.95	–	9.95	10	–	9.95	–	
V_{in} = V_{DD}					15	14.95	–	14.95	15	–	14.95	–	
Input Voltage	"0" Level	2	V_{IL}	0.0									Vdc
(V_O = 4.5 or 0.5 Vdc)					5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)					10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)					15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 4.5 Vdc)	"1" Level		V_{IH}	0.0	5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)					10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)					15	11	–	11	8.25	–	11	–	
Input Current (AL Device) Control			I_{in}	0.0	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device) Control			I_{in}	0.0	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)			C_{in}	0.0									pF
Control						–	–	–	5.0	7.5	–	–	
Switch Input						–	–	–	8.0	–	–	–	
Switch Output						–	–	–	20	–	–	–	
Feed Through						–	–	–	0.3	–	–	–	
Quiescent Current (AL Device)		3	I_{DD}	–	5.0	–	1.0	–	0.001	1.0	–	60	μAdc
(Per Package)					10	–	1.0	–	0.002	1.0	–	60	
					15	–	2.0	–	0.003	2.0	–	120	
Quiescent Current (CL/CP Device)		3	I_{DD}	–	5.0	–	5.0	–	0.001	5.0	–	70	μAdc
(Per Package)					10	–	5.0	–	0.002	5.0	–	70	
					15	–	10	–	0.003	10	–	140	
"ON" Resistance (AL Device)		4,5,6	R_{ON}										Ω
(V_C = V_{DD}, R_L = 10 kΩ)													
(V_{in} = +5.0 Vdc)				-5.0	5.0	–	400	–	200	480	–	640	
(V_{in} = −5.0 Vdc)						–	400	–	200	480	–	640	
(V_{in} = ±0.25 Vdc)						–	400	–	190	480	–	640	
(V_{in} = +7.5 Vdc)				-7.5	7.5	–	240	–	160	270	–	400	
(V_{in} = −7.5 Vdc)						–	240	–	160	270	–	400	
(V_{in} = ±0.25 Vdc)						–	240	–	120	270	–	400	
(V_{in} = +10 Vdc)				0	10	–	400	–	180	480	–	640	
(V_{in} = +0.25 Vdc)						–	400	–	180	480	–	640	
(V_{in} = +5.6 Vdc)						–	400	–	220	480	–	640	
(V_{in} = +15 Vdc)				0	15	–	250	–	180	270	–	400	
(V_{in} = +0.25 Vdc)						–	250	–	180	270	–	400	
(V_{in} = +9.3 Vdc)						–	250	–	215	270	–	400	
"ON" Resistance (CL/CP Device)		4,5,6	R_{ON}										Ω
(V_C = V_{DD}, R_L = 10 kΩ)													
(V_{in} = +5.0 Vdc)				-5.0	5.0	–	410	–	200	480	–	560	
(V_{in} = −5.0 Vdc)						–	410	–	200	480	–	560	
(V_{in} = +0.25 Vdc)						–	410	–	190	480	–	560	
(V_{in} = +7.5 Vdc)				-7.5	7.5	–	250	–	160	270	–	350	
(V_{in} = −7.5 Vdc)						–	250	–	160	270	–	350	
(V_{in} = ±0.25 Vdc)						–	250	–	120	270	–	350	
(V_{in} = +10 Vdc)				0	10	–	410	–	180	480	–	560	
(V_{in} = +0.25 Vdc)						–	410	–	180	480	–	560	
(V_{in} = +5.6 Vdc)						–	410	–	220	480	–	560	
(V_{in} = +15 Vdc)				0	15	–	250	–	180	270	–	350	
(V_{in} = +0.25 Vdc)						–	250	–	180	270	–	350	
(V_{in} = +9.3 Vdc)						–	250	–	215	270	–	350	
Δ"ON" Resistance		–	ΔR_{ON}										Ω
Between any 2 circuits in a common package													
(V_{in} = ±5.0 Vdc)				-5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)				-7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device
*T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Min	Typ #	Max	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 50 pF, R_L = 1.0 kΩ)	7	t_{PLH}, t_{PHL}	0.0	5.0 10 15	— — —	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, V_{in} = V_{DD} or V_{SS} (C_L = 50 pF, R_L = 1.0 kΩ)	8	t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH}	0.0	5.0 10 15	— — —	140 70 50	400 160 120	ns
Crosstalk, Control to Output (C_L = 50 pF, R_L = 1.0 kΩ R_{out} = 10 kΩ)	9	—	0.0	5.0 10 15	— — —	5.0 5.0 5.0	— — —	mV
Control Input Pulse Frequency (C_L = 50 pF, R_L = 1.0 kΩ)	10	f_{in}	0.0	5.0 10 15	— — —	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11,12	—	0.0	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	$\frac{nV}{\sqrt{cycle}}$
Sine Wave Distortion (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	—	−5.0	5.0	—	0.36	—	%
Off-Channel Leakage Current	—	I_{off}						nA
(V_{in} = +5.0 Vdc, V_{out} = −5.0 Vdc)			−5.0	5.0	—	±0.001	±125	
(V_{in} = −5.0 Vdc, V_{out} = +5.0 Vdc)			−5.0	5.0	—	±0.001	±125	
(V_{in} = +7.5 Vdc, V_{out} = −7.5 Vdc)			−7.5	7.5	—	±0.0015	±250	
(V_{in} = −7.5 Vdc, V_{out} = +7.5 Vdc)			−7.5	7.5	—	±0.0015	±250	
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz) $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	13	—	−5.0	5.0				dB
(R_L = 1.0 kΩ)					—	2.0	—	
(R_L = 10 kΩ)					—	0.8	—	
(R_L = 100 kΩ)					—	0.25	—	
(R_L = 1.0 MΩ)					—	0.01	—	
Bandwidth (−3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	—	BW	−5.0	5.0				MHz
(R_L = 1.0 kΩ)					—	35	—	
(R_L = 10 kΩ)					—	28	—	
(R_L = 100 kΩ)					—	27	—	
(R_L = 1.0 MΩ)					—	26	—	
Feedthrough and Crosstalk $20 \log_{10} \frac{V_{out}}{V_{in}} = -50$ dB	—	—	−5.0	5.0				MHz
(R_L = 1.0 kΩ)					—	850	—	
(R_L = 10 kΩ)					—	100	—	
(R_L = 100 kΩ)					—	12	—	
(R_L = 1.0 MΩ)					—	1.5	—	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

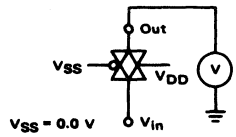
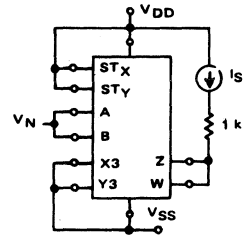


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT



$V_{NL} = V_N$ when $I_S = 10\ \mu A$
$V_{NH} = V_{DD} - V_N$ when $I_S = 10\ \mu A$
Pins 2,3,4,12,13 and 14 are left open.

FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

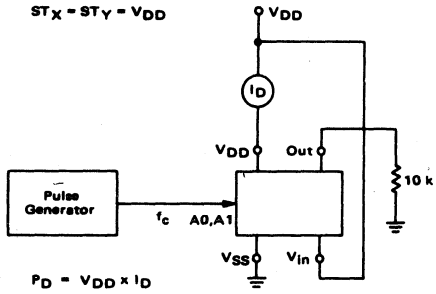
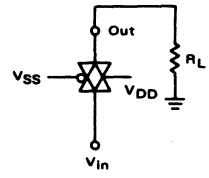


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

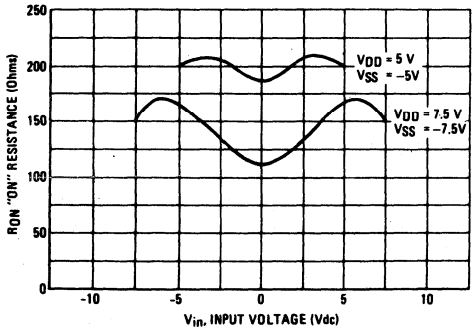
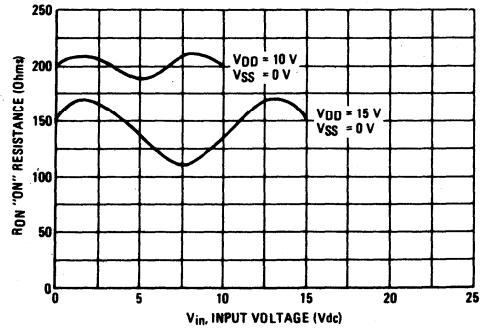


FIGURE 6



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FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

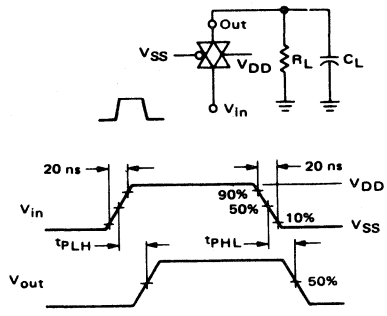


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

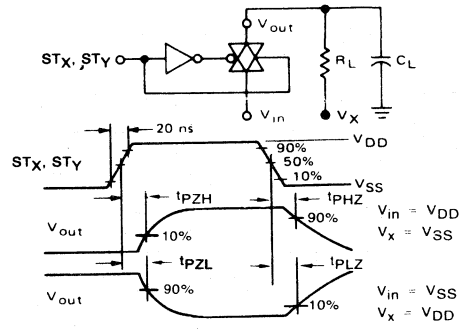


FIGURE 9 – CROSSTALK TEST CIRCUIT

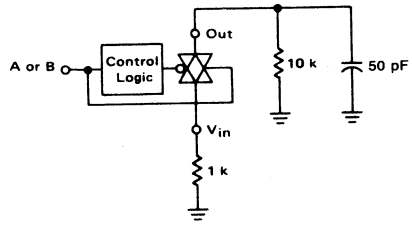


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

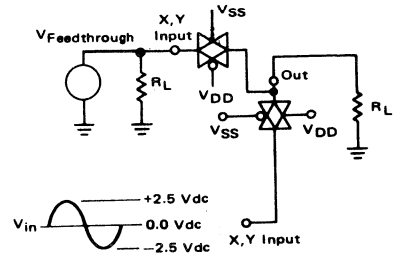


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

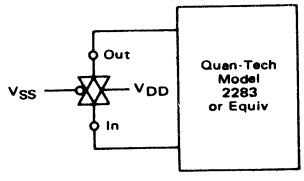
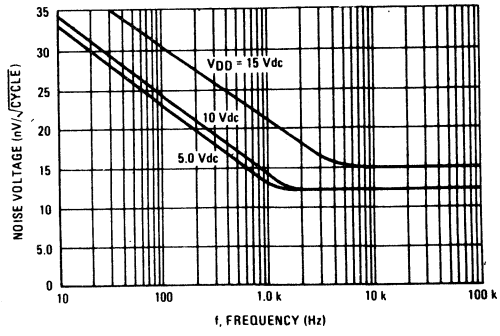
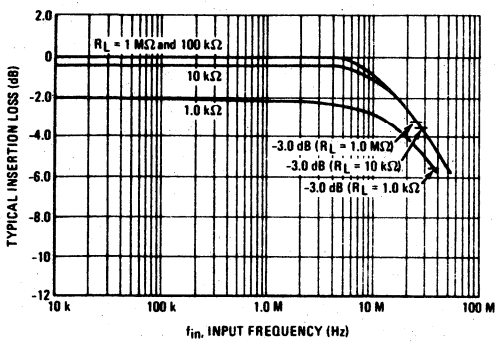


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

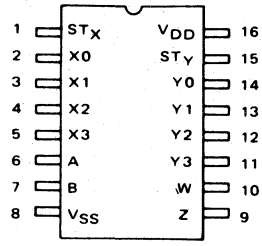


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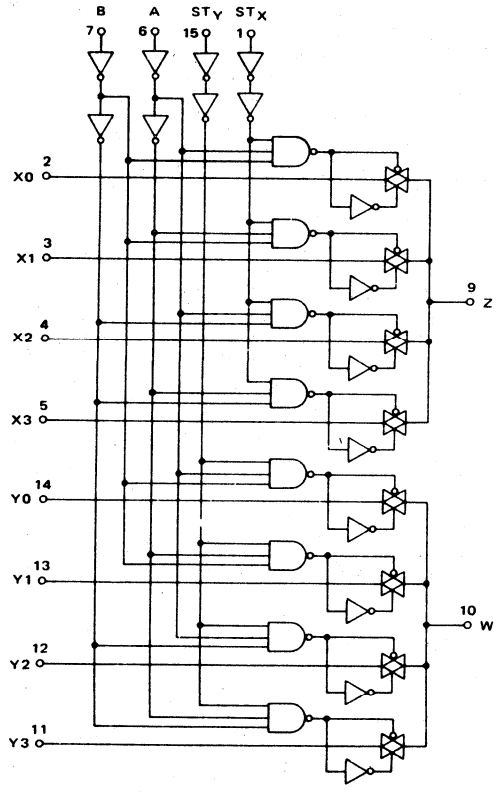
FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



PIN ASSIGNMENT



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

MOTOROLA

MC14530B

CMOS SSI

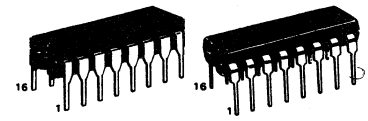
(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE

DUAL 5-INPUT MAJORITY LOGIC GATE

The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

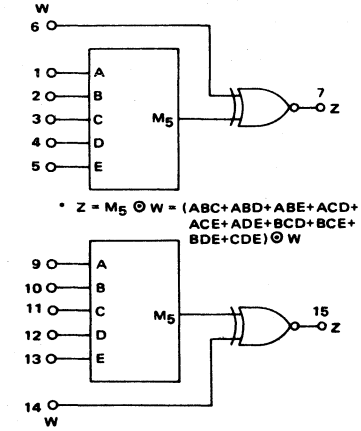
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

⊙ ≡ Exclusive NOR ≡ $\overline{\text{Exclusive OR}}$

LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
	1	1

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.2	–	2.25	1.25	–	1.15	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.5	–	4.50	2.5	–	2.4	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.0	–	6.75	3.0	–	2.9	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.85	–	3.75	2.75	–	3.75	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.6	–	7.5	5.50	–	7.5	–	
(V_O = 1.5 or 13.5 Vdc)		15	12.1	–	12	8.25	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

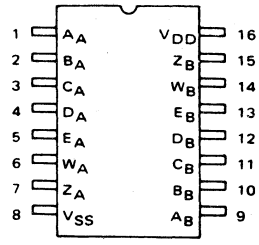
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENT



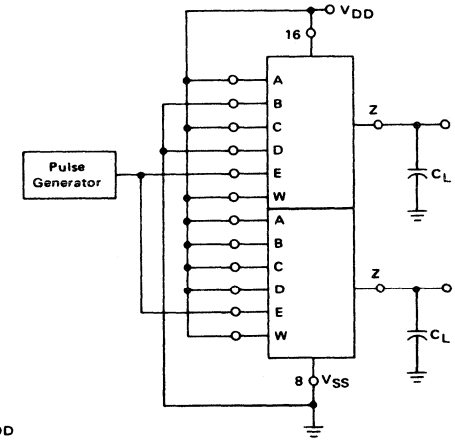
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

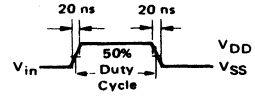
Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	960	
t_{PLH} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH} = (0.5 ns/pF) C_L + 85 ns		15	–	110	300	
t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	1200	ns
t_{PHL} = (0.66 ns/pF) C_L + 162 ns		10	–	195	540	
t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 170 ns		5.0	–	255	640	
t_{PLH} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	210	
t_{PHL} = (1.7 ns/pF) C_L + 195 ns	t_{PHL}	5.0	–	280	750	ns
t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	330	
t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	575	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 72 ns		10	–	105	265	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

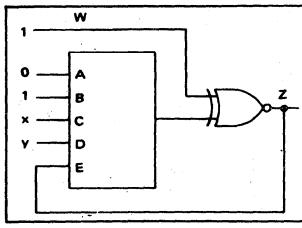




6

SEQUENTIAL LOGIC APPLICATIONS

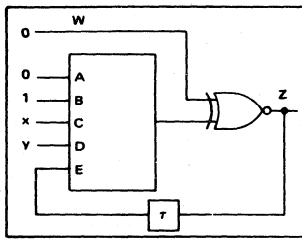
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

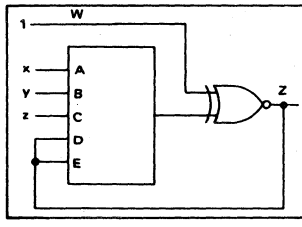
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

COINCIDENT FLIP-FLOP

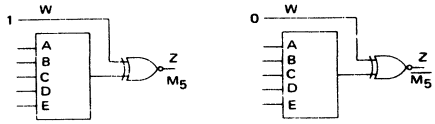


x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

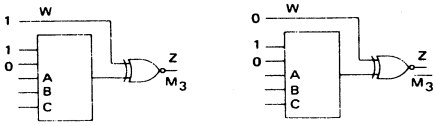
The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

6

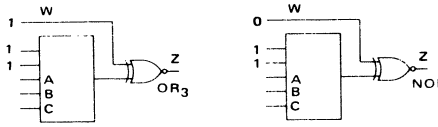
BASIC COMBINATIONAL FUNCTIONS



5-Input Majority Gates

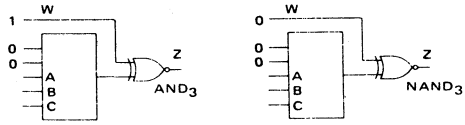


3 Input Majority Gates



3-Input OR Gate

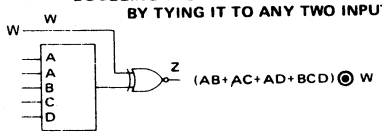
3-Input NOR Gate



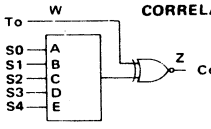
3 Input AND Gate

3-Input NAND Gate

DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS

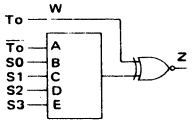


CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT

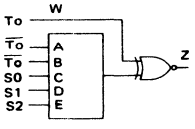


Correlation of 60%, 80%, 100%

The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.



Correlation of 75%, 100%.



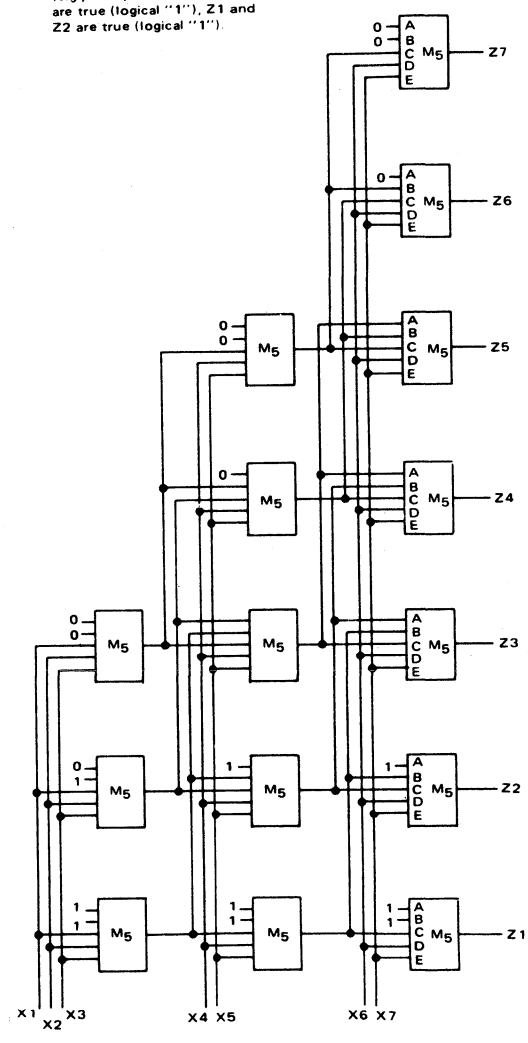
Correlation of 100%

5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



6

MOTOROLA

MC14531B

CMOS MSI

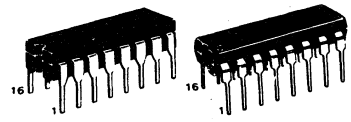
(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE

12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Variable Word Length
- Diode Protection on All Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

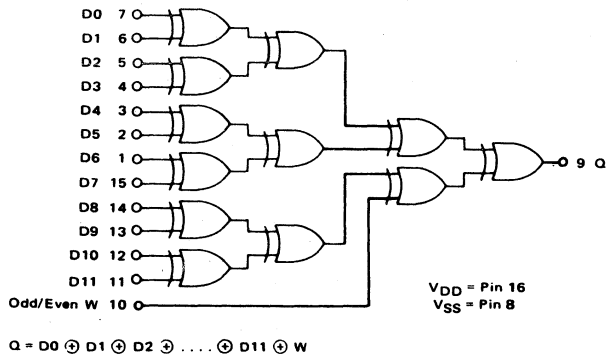
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



Q = D0 ⊕ D1 ⊕ D2 ⊕ .... ⊕ D11 ⊕ W

TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	···	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	···	0	0	0	0 (0)	0
0	0	0	···	0	0	1	1 (1)	1
0	0	0	···	0	1	0	2 (2)	1
0	0	0	···	0	1	1	3 (3)	0
0	0	0	···	1	0	0	4 (4)	1
0	0	0	···	1	0	1	5 (5)	0
0	0	0	···	1	1	0	6 (6)	0
0	0	0	···	1	1	1	7 (7)	1
.	.	.	···	.	.	.	.	.
.	.	.	···	.	.	.	.	.
1	1	1	···	0	0	0	8184 (17770)	0
1	1	1	···	0	0	1	8185 (17771)	1
1	1	1	···	0	1	0	8186 (17772)	1
1	1	1	···	0	1	1	8187 (17773)	0
1	1	1	···	1	0	0	8188 (17774)	1
1	1	1	···	1	0	1	8189 (17775)	0
1	1	1	···	1	1	0	8190 (17776)	0
1	1	1	···	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity
Note: May redefine to suit application by manipulating W and/or other available D's.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.25 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.50 μA/kHz) f + I_{DD}							
		15	I_T = (0.75 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

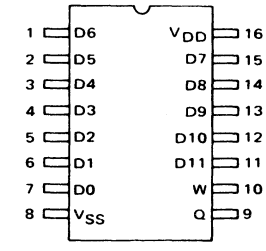
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

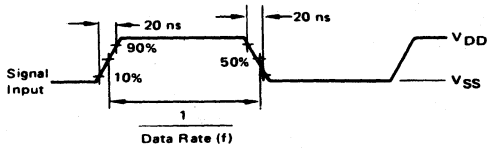
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Data to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 355 ns		5.0	–	440	1320	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	525	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	360	
Odd/Even to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 ns		5.0	–	250	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	210	

*The formulas given are for the typical characteristics only at 25°C.

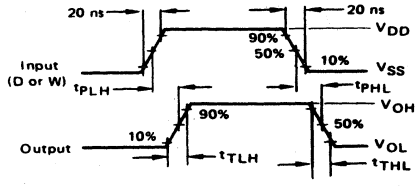
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM



f in respect to system clock

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



6

MOTOROLA

MC14532B

8-BIT PRIORITY ENCODER

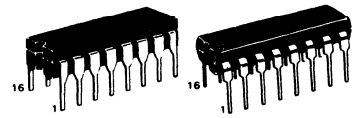
The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

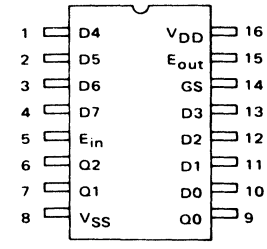
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−2.4	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.74 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.65 μA/kHz) f + I_{DD}							
		15	I_T = (5.73 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

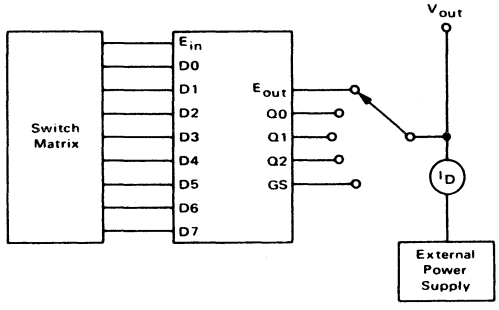
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time – E_{in} to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 120 ns		5.0	–	205	410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Propagation Delay Time (E_{in} to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} - (0.5 ns/pF) C_L + 40 ns		15	–	65	130	
Propagation Delay Time – E_{in} to Q_n	t_{PHL}, t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Propagation Delay Time – D_n to Q_n	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Propagation Delay Time – D_n to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	V_{GS} = V_{DD}, V_{DS} = V_{out} Sink Current		V_{GS} = -V_{DD}, V_{DS} = V_{out} -V_{DD} Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

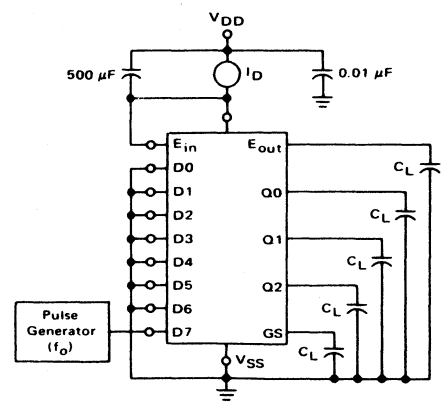
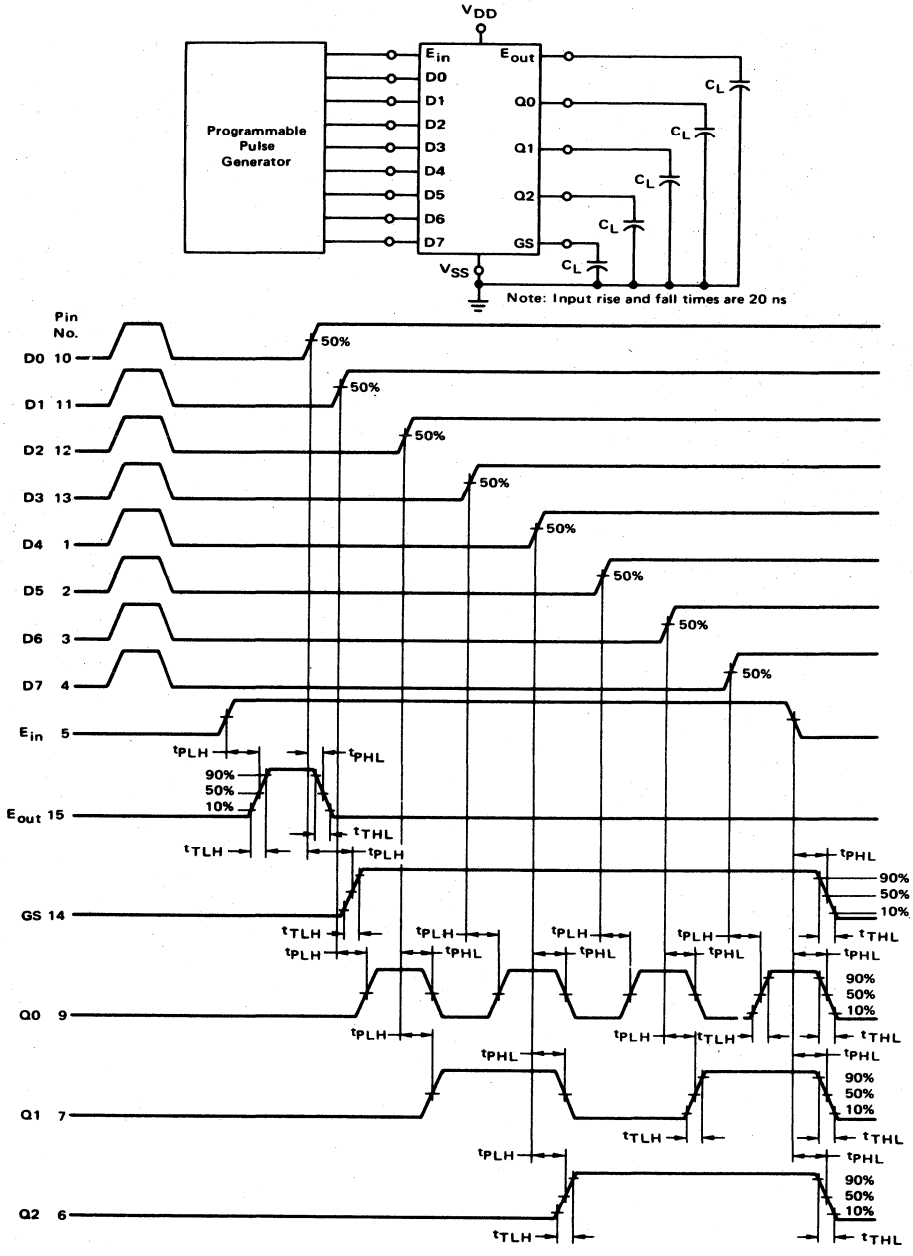


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)

LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \bar{D}0 \bullet \bar{D}1 \bullet \bar{D}2 \bullet \bar{D}3 \bullet \bar{D}4 \bullet \bar{D}5 \bullet \bar{D}6 \bullet \bar{D}7$
$Q0 = E_{in} \bullet (D1 \bullet \bar{D}2 \bullet \bar{D}4 \bullet \bar{D}6 + D3 \bullet \bar{D}4 \bullet \bar{D}6 + D5 \bullet \bar{D}6 + D7)$
$Q1 = E_{in} \bullet (D2 \bullet \bar{D}4 \bullet \bar{D}5 + D3 \bullet \bar{D}4 \bullet \bar{D}5 + D6 + D7)$
$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$
$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$

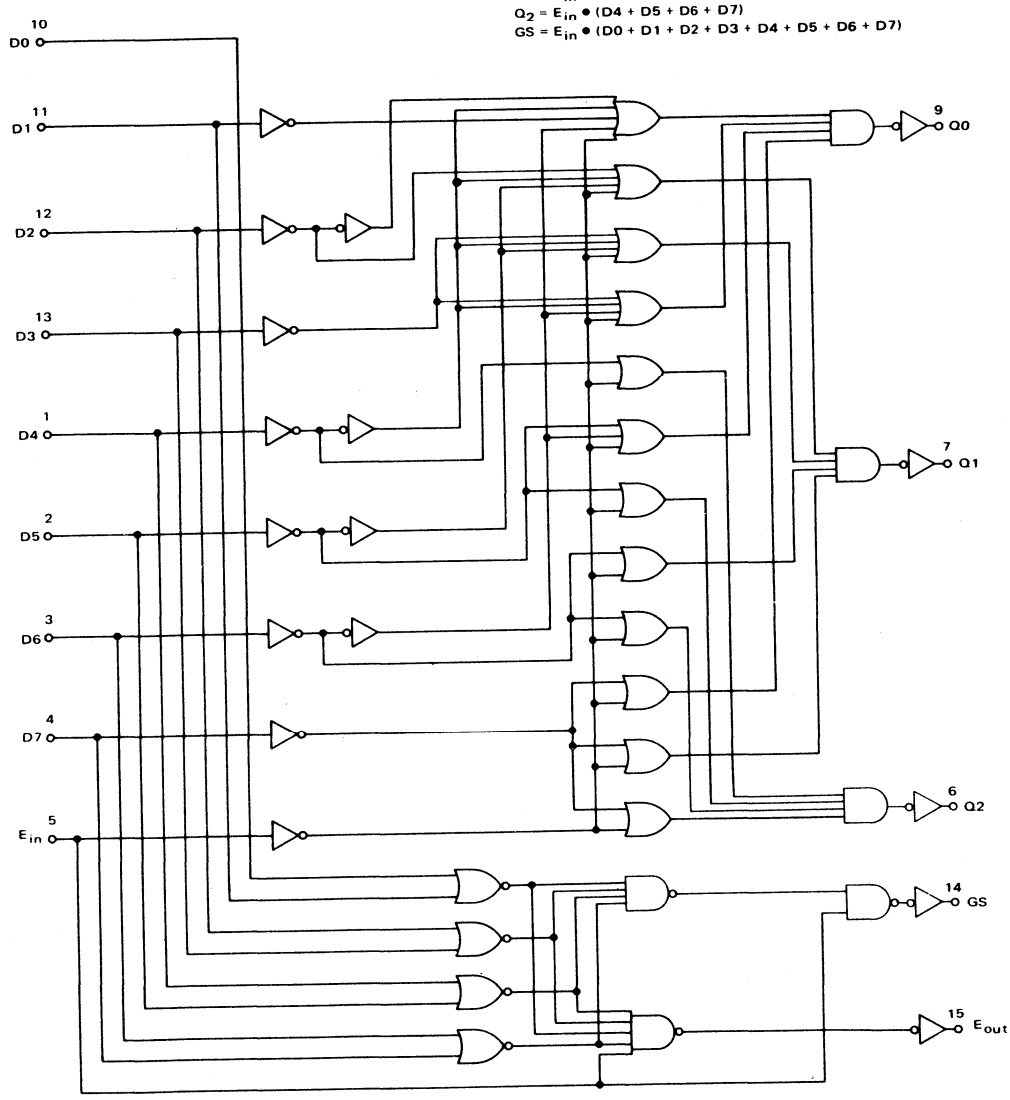


FIGURE 4 – TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

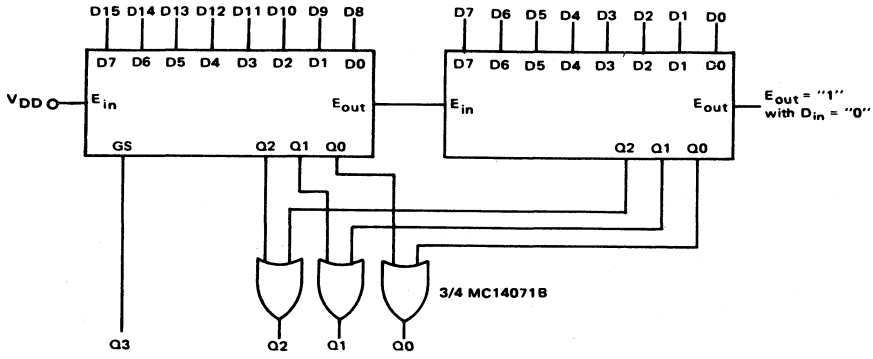
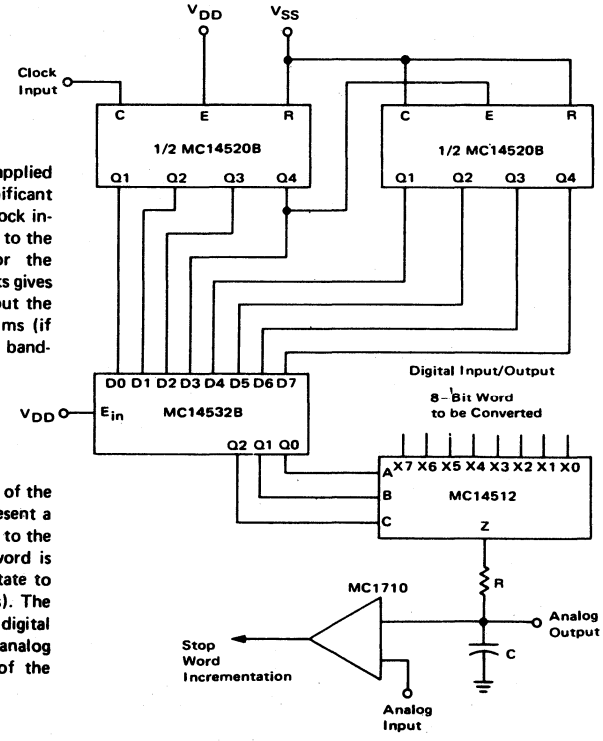


FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C ≈ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

6

MOTOROLA

MC14534B

CMOS LSI

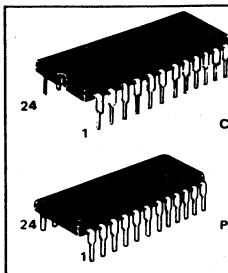
(LOW-POWER COMPLEMENTARY MOS)

5 CASCADED BCD COUNTERS

5 CASCADED BCD COUNTERS

The MC14534B is composed of five BCD ripple counters that have their respective outputs multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four (BCD) pins. Selection is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 623

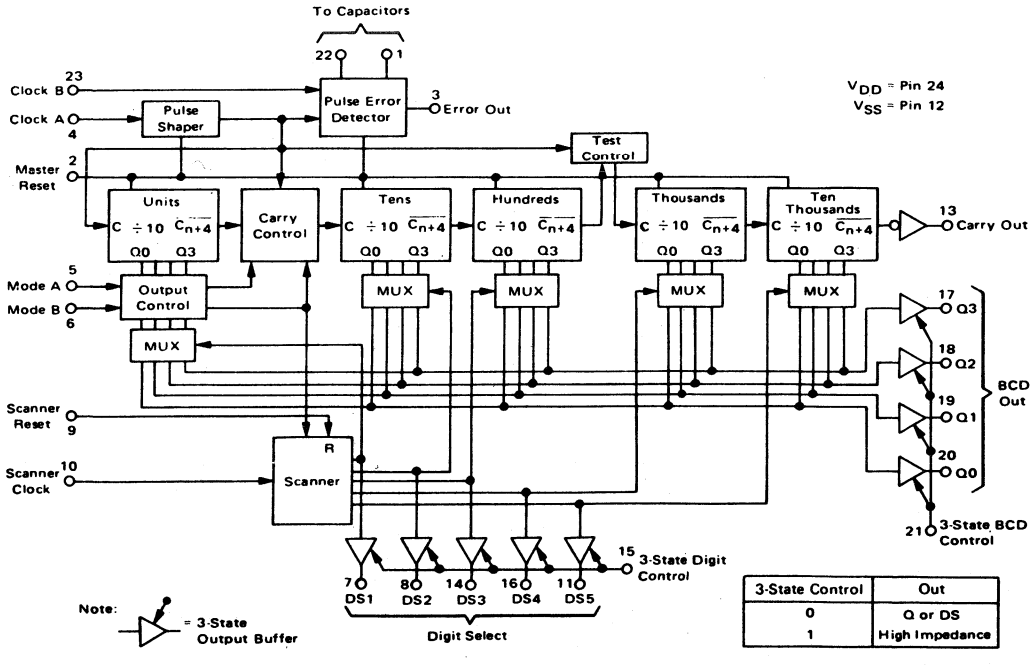
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



3-State Control	Out
0	Q or DS
1	High Impedance

6

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.0	–	1.5	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.0	–	3.0	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.0	–	4.5	3.0	–	3.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	4.0	–	4.0	3.5	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	7.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12	–	12	11	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current – Pins 1 and 22 (AL Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.31	–	-0.25	-0.8	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.31	–	-0.25	-0.4	–	-0.17	–	
(V_{OH} = 13.5 Vdc)		15	-0.9	–	-0.75	-1.6	–	-0.51	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024	–	0.02	0.03	–	0.014	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.06	–	0.05	0.09	–	0.035	–	
(V_{OL} = 1.5 Vdc)		15	1.3	–	0.25	1.63	–	0.175	–	
Output Drive Current – Pins 1 and 22 (CL/CP Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.11	–	-0.10	-0.8	–	-0.08	–	
(V_{OH} = 9.5 Vdc)		10	-0.11	–	-0.10	-0.4	–	-0.08	–	
(V_{OH} = 13.5 Vdc)		15	-0.33	–	-0.30	-1.6	–	-0.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.012	–	0.01	0.02	–	0.008	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.03	–	0.025	0.05	–	0.02	–	
(V_{OL} = 1.5 Vdc)		15	0.14	–	0.12	1.35	–	0.10	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}) (continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.5\ \mu A/kHz)\ f + I_{DD}$ Scan Oscillator Frequency = 1 kHz							μAdc
		10	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C, See Figure 1)

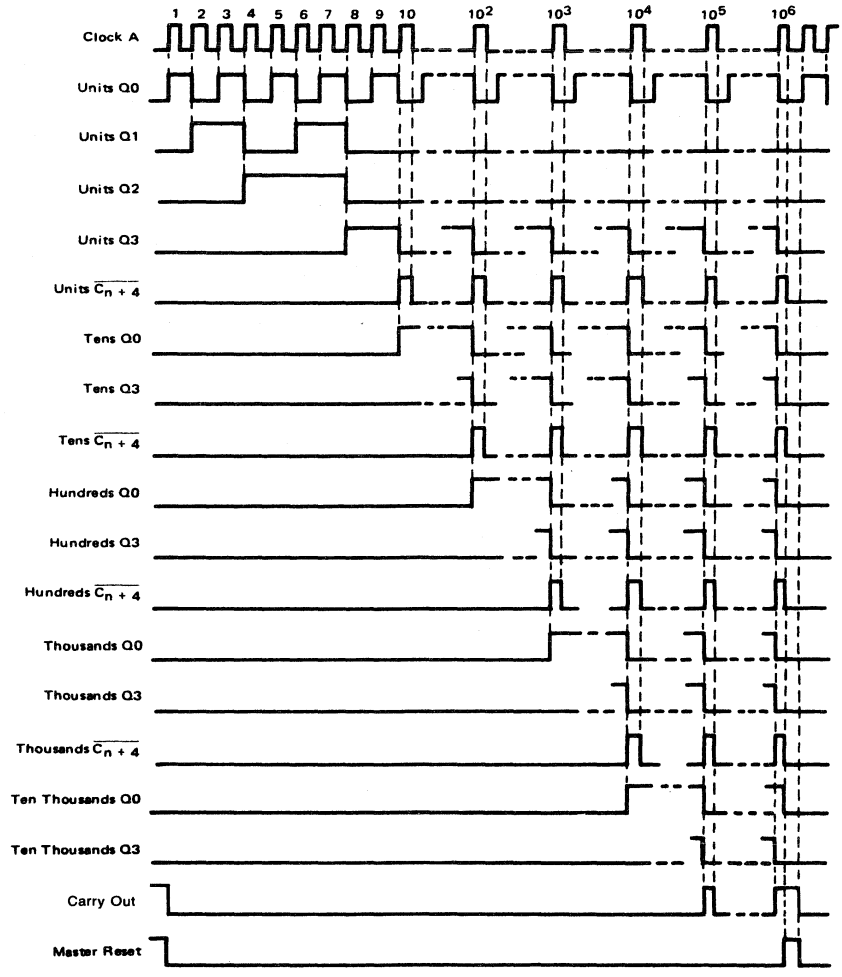
Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
		5.0	—	180	360	
		10	—	90	180	
		15	—	65	130	
Output Fall Time	t_{THL}					ns
		5.0	—	180	360	
		10	—	100	180	
		15	—	75	130	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 μs		5.0	—	4.0	8.0	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 μs		10	—	1.5	3.0	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 μs		15	—	1.0	2.25	
Clock to Carry Out	t_{PLH}					μs
t_{PLH} = (1.8 ns/pF) C_L + 3.3 μs		5.0	—	3.3	6.6	
t_{PLH} = (0.8 ns/pF) C_L + 1.1 μs		10	—	1.1	2.2	
t_{PLH} = (0.6 ns/pF) C_L + 0.8 μs		15	—	0.8	1.7	
Master Reset to Q	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	—	1.8	3.6	
t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	—	0.6	1.2	
t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	—	0.5	0.9	
Master Reset to Error Out	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 0.57 μs		5.0	—	0.6	1.5	
t_{PHL} = (0.8 ns/pF) C_L + 0.19 μs		10	—	0.2	.5	
t_{PHL} = (0.6 ns/pF) C_L + 0.11 μs		15	—	0.12	0.38	
Scanner Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	—	1.8	3.6	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	—	0.6	1.2	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	—	0.5	0.9	
Scanner Clock to Digit Select	t_{PLH}, t_{PLH}					μs
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 μs		5.0	—	1.5	3.0	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 μs		10	—	0.5	1.0	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 μs		15	—	0.4	0.75	
Propagation Delay Time 3-State Control to Q	t_{PHZ}	5.0	—	75	150	ns
		10	—	45	90	
		15	—	40	80	
	t_{PZH}	5.0	—	120	240	ns
		10	—	55	110	
		15	—	40	80	
	t_{PLZ}	5.0	—	120	240	ns
		10	—	55	110	
		15	—	45	90	
	t_{PZL}	5.0	—	160	320	ns
		10	—	70	140	
		15	—	45	90	
Clock Pulse Frequency	f_{cl}	5.0	—	1.0	0.5	MHz
		10	—	3.0	1.0	
		15	—	5.0	1.2	
Clock or Scanner Clock Pulse Width	t_{WH}	5.0	1000	500	—	ns
		10	500	190	—	
		15	375	125	—	
Scanner Reset Pulse Width	t_w	5.0	320	160	—	ns
		10	130	65	—	
		15	80	40	—	
Scanner Reset Removal Time	t_{rem}	5.0	900	270	—	ns
		10	150	80	—	
		15	100	50	—	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	2000	900	—	ns
		10	600	300	—	
		15	450	250	—	
Master Reset Removal Time	t_{rem}	5.0	1060	550	—	ns
		10	350	205	—	
		15	250	140	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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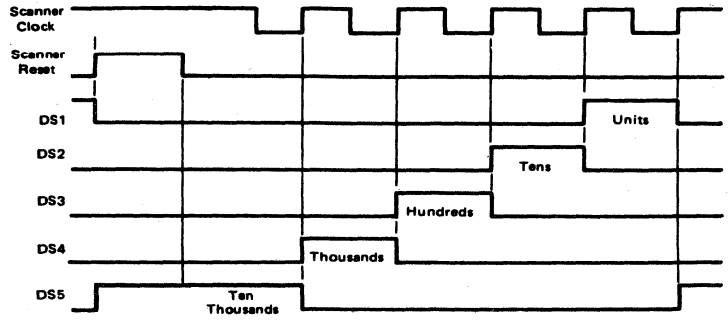
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

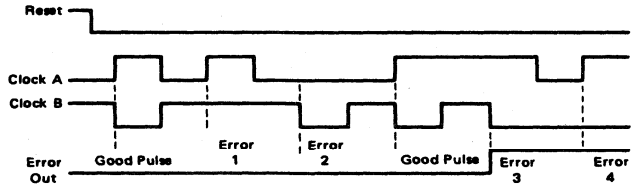
Mode A	Mode B	First Stage Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first stage	5-digit Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first stage	4-digit counter with ÷ 10 and roundoff at front end.
1	0	Counts 3, 4, 5, 6, 7 = 5 Counts 8, 9, 0, 1, 2 = 0	At 7 to 8 transition of first stage	4-digit counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



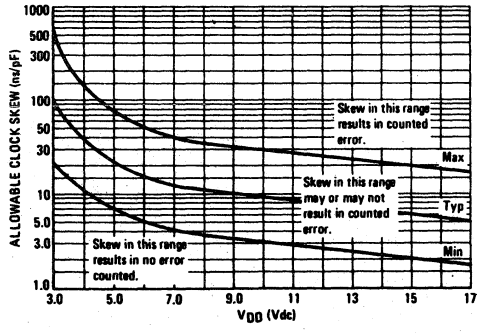
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

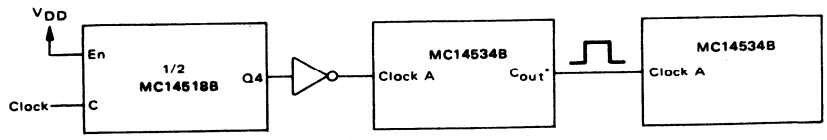


Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geq$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

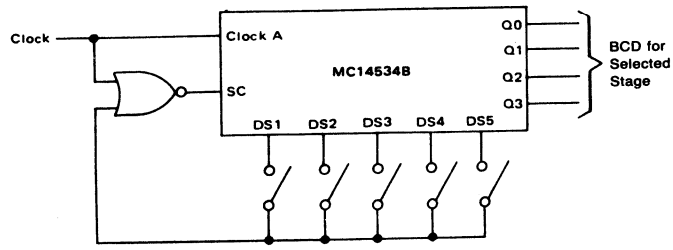
APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



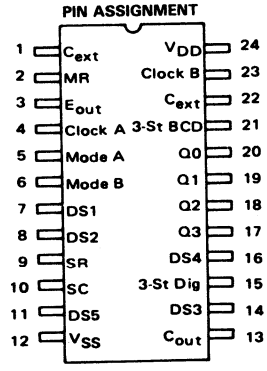
*Carry Out is high for a single clock period when all five BCD stages go to zero. (Carry Out also goes high when MR is applied.)

FIGURE 2 — FORCING A BCD STAGE TO THE Q OUTPUTS



When the Q outputs of a given stage are required, this configuration will lock up the selected stage within four clock cycles. The select line feedback may be hardwired or switched.

PIN ASSIGNMENT



MOTOROLA

MC14536B

PROGRAMMABLE TIMER

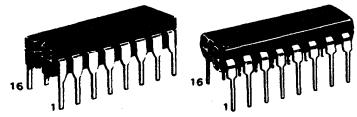
The MC14536B programmable timer is a 24-stage binary ripple counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has been included. By selecting the appropriate counter stage in conjunction with the appropriate input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- 8-Bypass Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit and Oscillator Inhibit Inputs
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

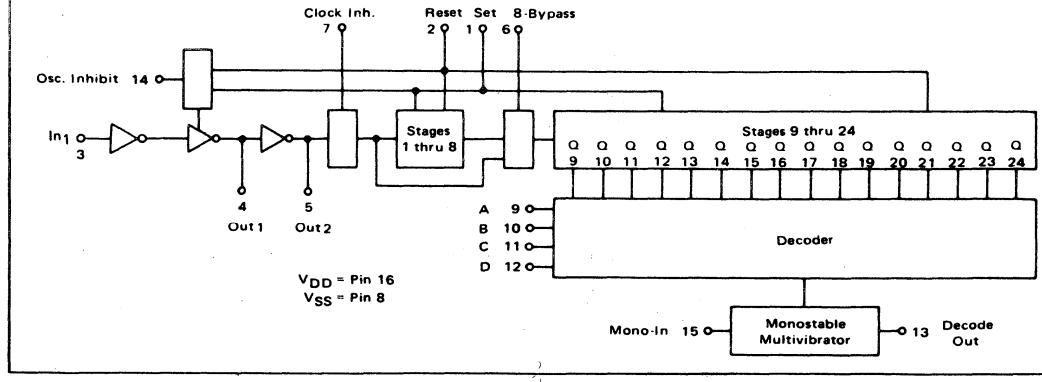
ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

6

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		1.0	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vds)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.15 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.3 µA/kHz) f + I_{DD}							
		15	I_T = (3.55 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

6

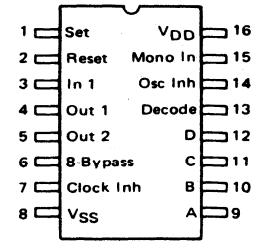
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time (Pin 13)	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1, 8-Bypass (Pin 6) High						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	1000	
Clock to Q1, 8-Bypass (Pin 6) Low	t_{PLH}, t_{PHL}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns		5.0	–	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	1.1	2.3	
Clock to Q16	t_{PLH}, t_{PHL}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns		5.0	–	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	900	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
		10	200	100	–	
		15	170	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.2	0.4	MHz
		10	–	3.0	1.5	
		15	–	5.0	2.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Reset Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	400	200	–	
		15	300	150	–	

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



6

PIN DESCRIPTIONS

INPUTS

SET (Pin 1) — A high on Set asynchronously forces Decode Out to a high level. This is accomplished by setting an output conditioning latch to a high level while at the same time resetting the 24 flip-flop stages. After Set goes low (inactive), the occurrence of the first negative clock transition on IN_1 causes Decode Out to go low. The counter's flip-flop stages begin counting on the second negative clock transition of IN_1. When Set is high, the on-chip RC oscillator is disabled. This allows for very low-power standby operation.

RESET (Pin 2) — A high on Reset asynchronously forces Decode Out to a low level; all 24 flip-flop stages are also reset to a low level. Like the Set input, Reset disables the on-chip RC oscillator for standby operation.

IN_1 (Pin 3) — The device's internal counters advance on the negative-going edge of this input. IN_1 may be used as an external clock input or used in conjunction with OUT_1 and OUT_2 to form an RC oscillator. When an external clock is used, both OUT_1 and OUT_2 may be left unconnected or used to drive 1 LSTTL or several CMOS loads.

8-BYPASS (Pin 6) — A high on this input causes the first 8 flip-flop stages to be bypassed. This device essentially becomes a 16-stage counter with all 16 stages selectable. Selection is accomplished by the A, B, C, and D inputs. (See the truth tables.)

CLOCK INHIBIT (Pin 7) — A high on this input disconnects the first counter stage from the clocking source. This holds the present count and inhibits further counting. However, the clocking source may continue to run. Therefore, when Clock Inhibit is brought low, no oscillator start-up time is required. When Clock Inhibit is low, the counter will start counting on the occurrence of the first negative edge of the clocking source at IN_1.

OSC INHIBIT (Pin 14) — A high level on this pin stops the RC oscillator which allows for very low-power standby operation. May also be used, in conjunction with an external clock, with essentially the same results as the Clock Inhibit input.

MONO-IN (Pin 15) — Used as the timing pin for the on-chip monostable multivibrator. If the Mono-In input is connected to V_{SS}, the monstable circuit is disabled, and Decode Out is directly connected to the selected Q output. The monostable circuit is enabled if a resistor is connected between Mono-In and V_{DD}. This resistor and the device's internal capacitance will determine the minimum output pulse widths. With the addition of an external capacitor to V_{SS}, the pulse width range may be extended. For reliable operation the resistor value should be limited to the range of 5 kΩ to 100 kΩ and the capacitor value should be limited to a maximum of 1000 pf. (See figures 3, 4, 5, and 10).

A, B, C, D (Pins 9, 10, 11, 12) — These inputs select the flip-flop stage to be connected to Decode Out. (See the truth tables.)

OUTPUTS

OUT_1, OUT_2 (Pin 4, 5) — Outputs used in conjunction with IN_1 to form an RC oscillator. These outputs are buffered and may be used for 2^0 frequency division of an external clock.

DECODE OUT (Pin 13) — Output function depends on configuration. When the monostable circuit is disabled, this output is a 50% duty cycle square wave during free run.

TEST MODE

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. The test mode is enabled when 8-Bypass, Set and Reset are at a high level. (See Figure 8.)

TRUTH TABLES

Input					Stage Selected For Decode Out
8-Bypass	D	C	B	A	
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	17
0	1	0	0	1	18
0	1	0	1	0	19
0	1	0	1	1	20
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0	1	1	0	1	22
0	1	1	1	0	23
0	1	1	1	1	24

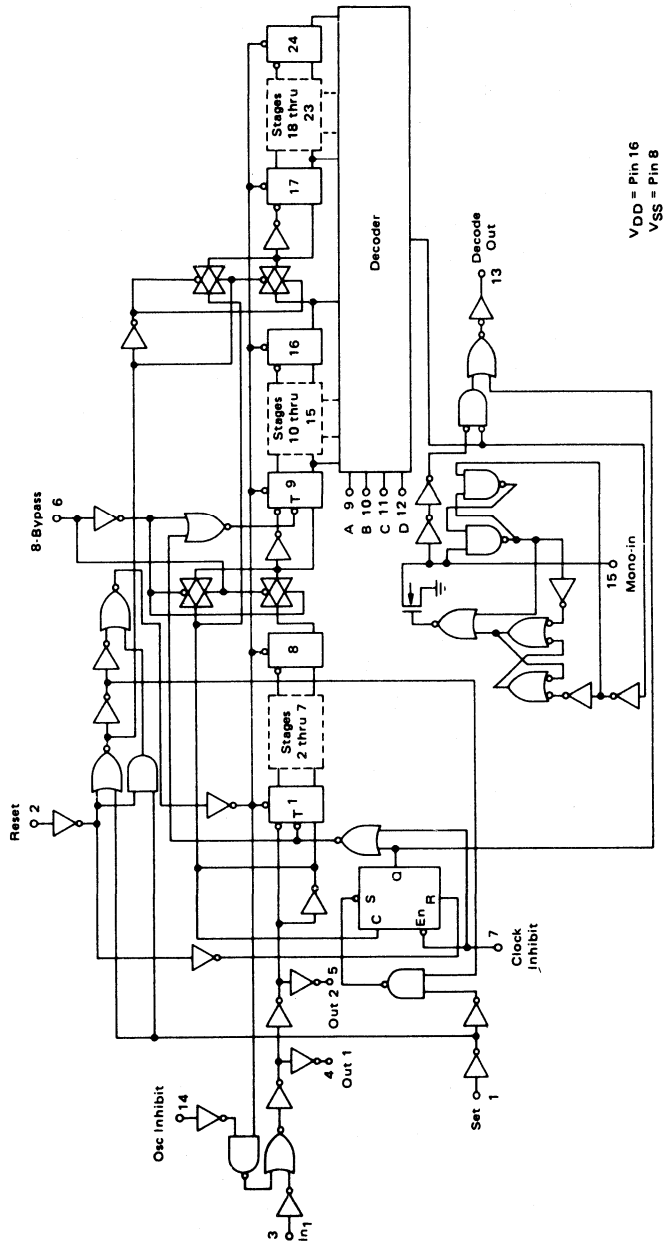
Input					Stage Selected For Decode Out
8-Bypass	D	C	B	A	
1	0	0	0	0	1
1	0	0	0	1	2
1	0	0	1	0	3
1	0	0	1	1	4
1	0	1	0	0	5
1	0	1	0	1	6
1	0	1	1	0	7
1	0	1	1	1	8
1	1	0	0	0	9
1	1	0	0	1	10
1	1	0	1	0	11
1	1	0	1	1	12
1	1	1	0	0	13
1	1	1	0	1	14
1	1	1	1	0	15
1	1	1	1	1	16

FUNCTION TABLE

In_1	Set	Reset	Clock Inh	OSC Inh	Out 1	Out 2	Decode Out
⎍	0	0	0	0	⎍	⎎	No Change
⎎	0	0	0	0	⎎	⎍	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0	—	—	No Change
X	0	0	0	1	0	1	No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⎍	⎎	⎍	Advance to next state

X = Don't Care

LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 11 in Application)

FIGURE 1 — RC OSCILLATOR STABILITY

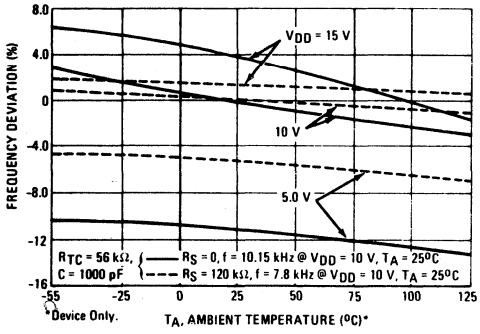
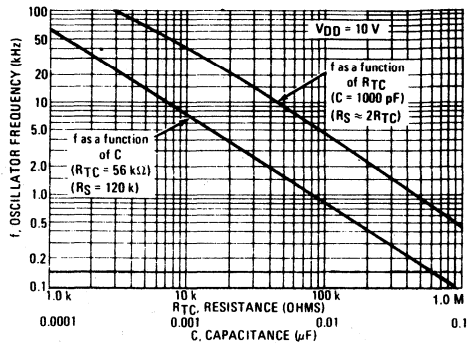


FIGURE 2 — RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 10 in Application)

FIGURE 3 — TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

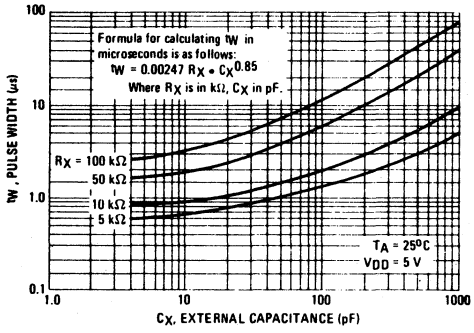


FIGURE 4 — TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 10 V

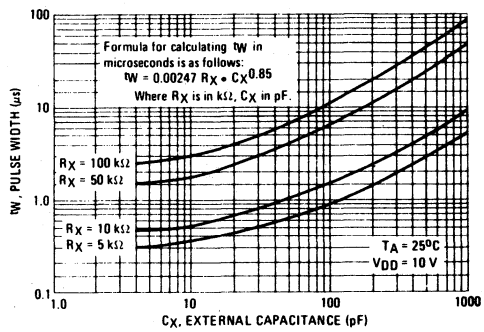
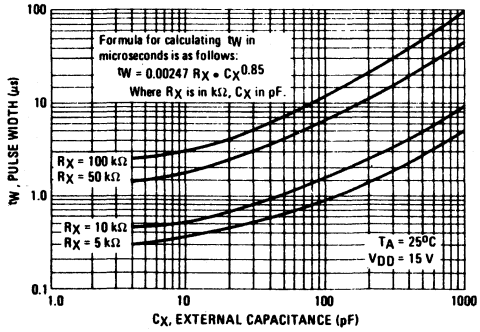


FIGURE 5 — TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 15 V



6

FIGURE 6 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

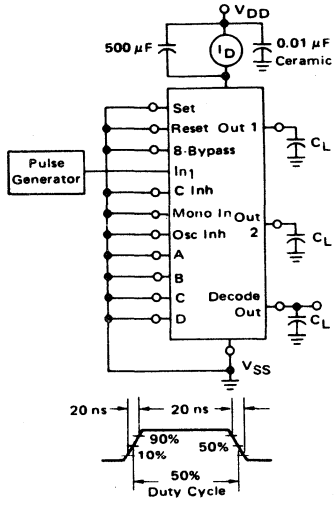


FIGURE 7 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

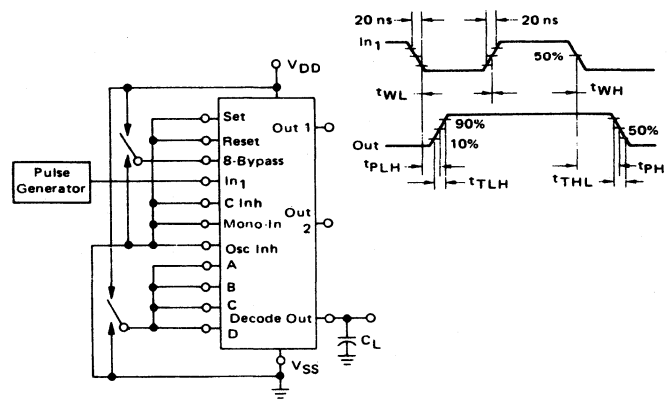
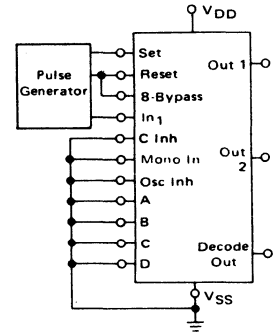


FIGURE 8 — FUNCTIONAL TEST CIRCUIT



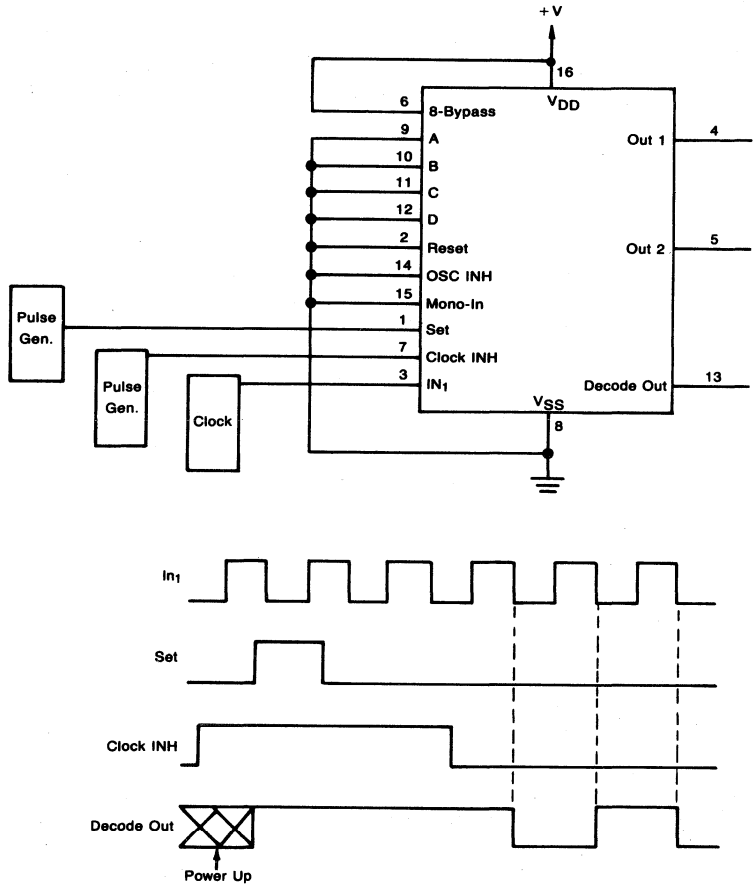
FUNCTIONAL TEST SEQUENCE

Test function (Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

FUNCTIONAL TEST SEQUENCE

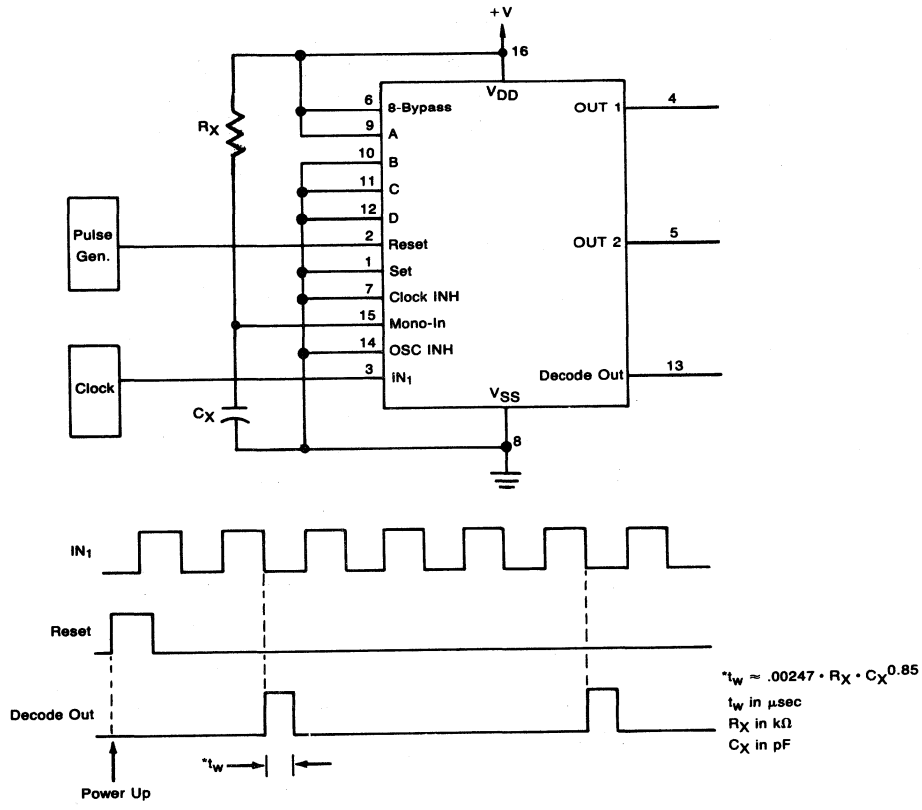
INPUTS				OUTPUTS	COMMENTS
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8-stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 – – –	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In_1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

FIGURE 9 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, SET, AND CLOCK INHIBIT FUNCTIONS (DIVIDE-BY-2 CONFIGURED)



Note: When power is first applied to the device, Decode Out can be either at a high or low state. On the rising edge of a Set pulse the output goes high if initially at a low state. The output remains high if initially at a high state. Because Clock Inh is held high, the clock source on the input pin has no effect on the output. Once Clock Inh is taken low, the output goes low on the first negative clock transition. The output returns high depending on the 8-Bypass, A, B, C, and D inputs, and the clock input period. A 2^n frequency division (where n = the number of stages selected from the truth table) is obtainable at Decode Out. A 2^0 -divided output of IN_1 can be obtained at OUT_1 and OUT_2.

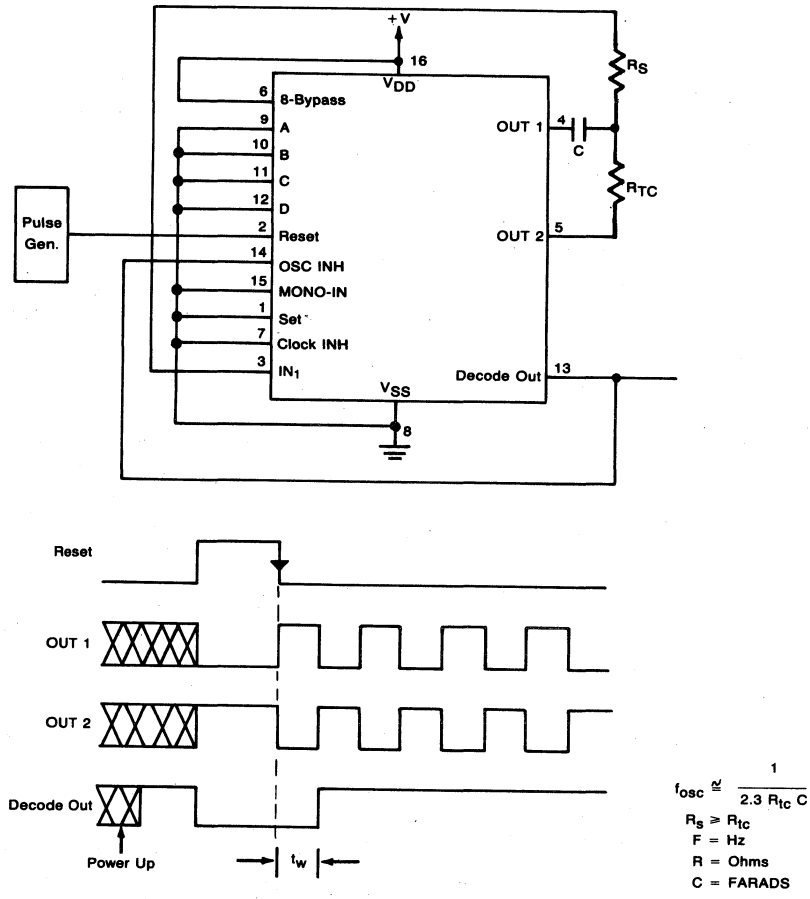
FIGURE 10 — TIME INTERVAL CONFIGURATION USING AN EXTERNAL CLOCK, RESET, AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT. (DIVIDE-BY-4 CONGIFURED).



Note: When Power is first applied to the device with the Reset input going high, Decode Out initializes low. Bringing the Reset input low enables the chip's internal counters. After Reset goes low, the $2^n/2$ negative transition of the clock input causes Decode Out to go high. Since the Mono-In input is being used, the output becomes monostable. The pulse width of the output is dependent on the external timing components. The second and all subsequent pulses occur at $2^n \times$ (the clock period) intervals where n = the number of stages selected from the truth table.

6

FIGURE 11 — TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL (DIVIDE-BY-2 CONFIGURED)



Note: This circuit is designed to use the on-chip oscillation function. The oscillator frequency is determined by the external R and C components. When power is first applied to the device, Decode Out initializes to a high state. Because this output is tied directly to the Osc-Inh input, the oscillator is disabled. This puts the device in a low-current standby condition. The rising edge of the Reset pulse will cause the output to go low. This in turn causes Osc-Inh to go low. However, while Reset is high, the oscillator is still disabled (i.e.: standy condition). After Reset goes low, the output remains low for $2^n/2$ of the oscillator's period. After the part times out, the output again goes high.

MOTOROLA

MC14538B

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

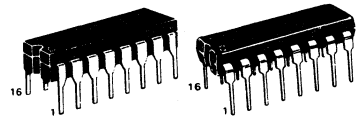
The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative-Going Edge (B-Input)
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- Use the MC54/74HC4538 for Pulse Widths Less Than 10 μs with Supplies Up to 6 V.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

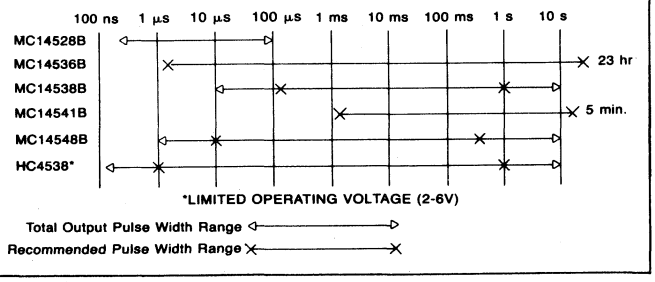
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

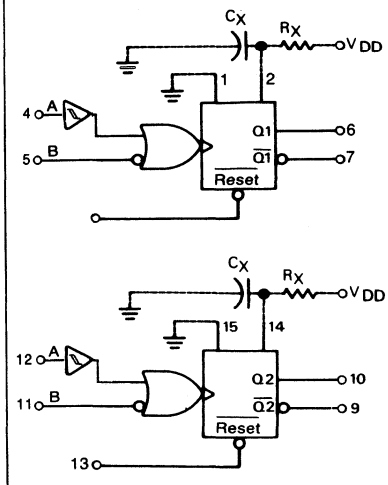
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

ONE-SHOT SELECTION GUIDE



BLOCK DIAGRAM



R_X and C_X are external components.
V_{DD} = Pin 16
V_{SS} = Pin 8, Pin 1, Pin 15

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current, Pin 2 or 14	I_{in}	15	–	±0.05	–	±0.00001	±.05	–	±0.5	µAdc
Input Current, Other Inputs (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current, Other Inputs (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance, Pin 2 or 14	C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
Q = Low, $\overline{Q}$ = High		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
Q = Low, $\overline{Q}$ = High		15	–	80	–	0.015	80	–	600	
Quiescent Current, Active State (Both)	I_{DD}	5	—	2.0	—	.04	.20	—	2.0	mAdc
(Per Package)		10	—	2.0	—	.08	.45	—	2.0	
Q = High, $\overline{Q}$ = Low		15	—	2.0	—	.13	.70	—	2.0	
**Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X)	I_T	5.0	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$							
		10.0	$I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$							
		15.0	$I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$							
			where: I_T in µA (one monostable switching only), C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	All Types Typ #	All Types Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to Q or $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	220	
$\overline{Reset}$ to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Input Rise and Fall Times	t_r, t_f	5	—	—	15	µs
$\overline{Reset}$		10	—	—	5	
		15	—	—	4	
B Input		5	—	300	1.0	ms
		10	—	1.2	0.1	
		15	—	0.4	0.05	
A Input		5	No Limit			—
		10				
		15				
Input Pulse Width	t_{WH}, t_{WL}	5.0	170	85	–	ns
A, B, or Reset		10	90	45	–	
		15	80	40	–	
Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	
		15	0	–	–	
Output Pulse Width — Q or $\overline{Q}$	T					µs
Refer to Figures 8 and 9						
C_X = 0.002 µF, R_X = 100 kΩ		5.0	198	210	230	
		10	200	212	232	
		15	202	214	234	
C_X = 0.1 µF, R_X = 100 kΩ		5.0	9.3	9.86	10.5	ms
		10	9.4	10	10.6	
		15	9.5	10.14	10.7	
C_X = 10 µF, R_X = 100 kΩ		5.0	0.91	0.965	1.03	s
		10	0.92	0.98	1.04	
		15	0.93	0.99	1.06	
Pulse Width Match between circuits in	$\frac{100(T_1 - T_2)}{T_1}$	5.0	–	±1.0	±5.0	%
the same package.		10	–	±1.0	±5.0	
C_X = 0.1 µF, R_X = 100 kΩ		15	–	±1.0	±5.0	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	*	kΩ
External Timing Capacitance	C_X	–	0	–	No Limit†	µF

* The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptability to externally induced noise signals may occur for $R_X \geq$ 1 MΩ.

† If $C_X \geq$ 15 µF, use discharge protection diode per Fig. 11.

6

FIGURE 1 – LOGIC DIAGRAM
(1/2 of Device Shown)

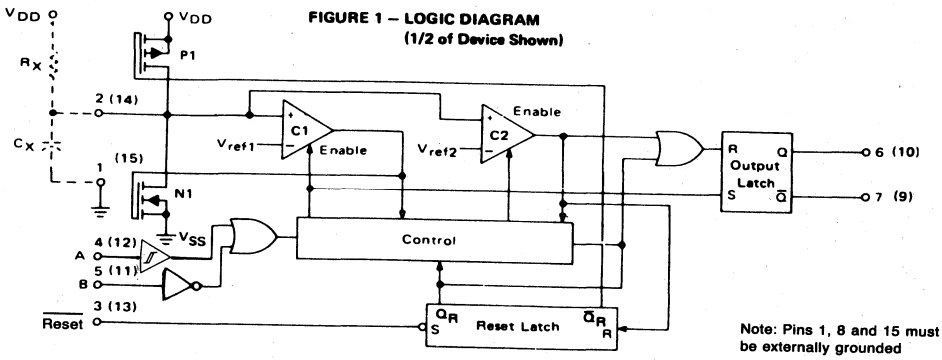


FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

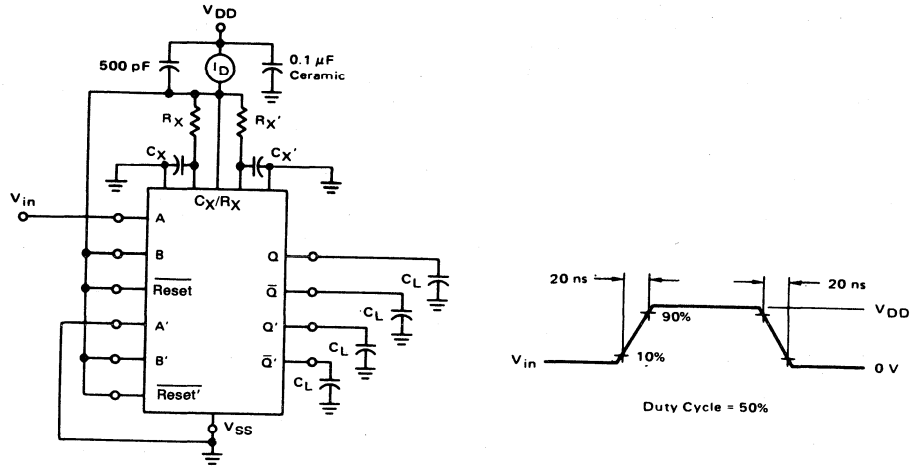
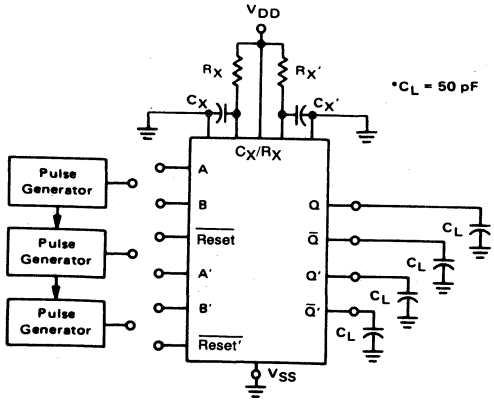


FIGURE 3 – SWITCHING TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	Reset	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

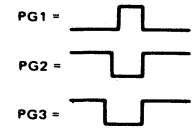


FIGURE 4 – SWITCHING TEST WAVEFORMS

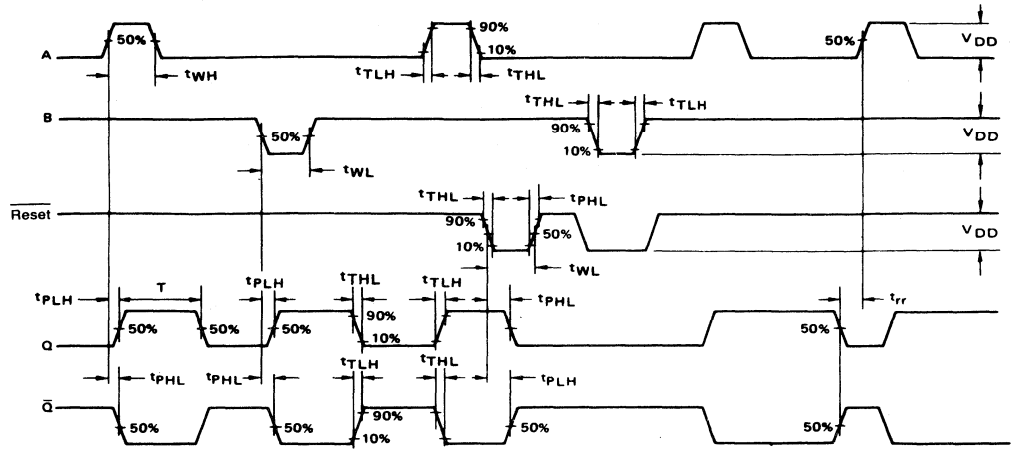


FIGURE 5 – TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

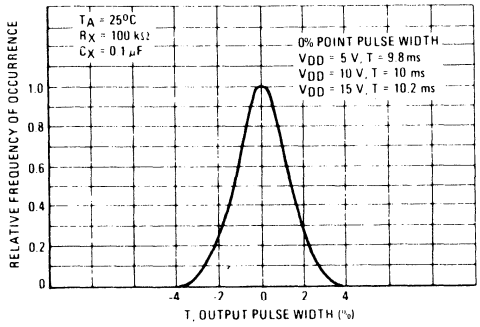


FIGURE 6 – TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

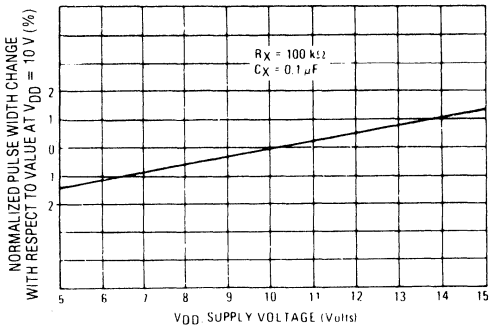
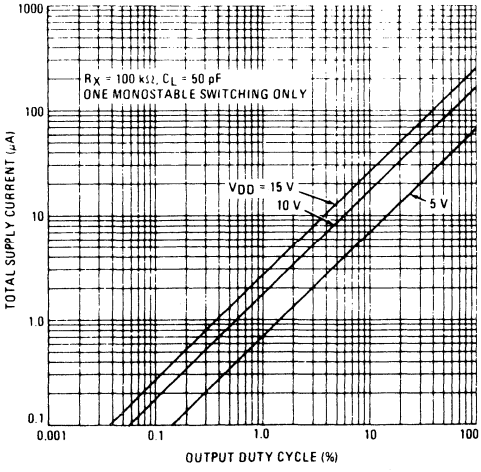


FIGURE 7 – TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE



FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{Q}$
H	↑	H	⊓	⊔
H	L	↓	⊓	⊔
H	↑↓	L	Not Triggered	
H	H	↑↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓↑	X	X	Not Triggered	

6

FIGURE 8 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE

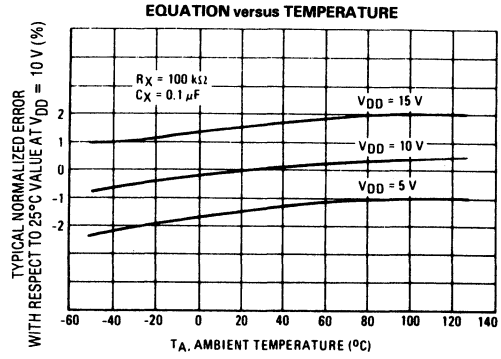
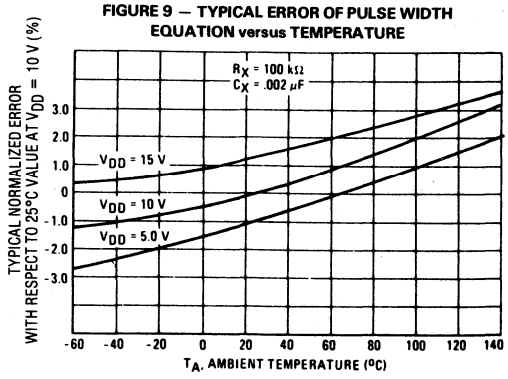
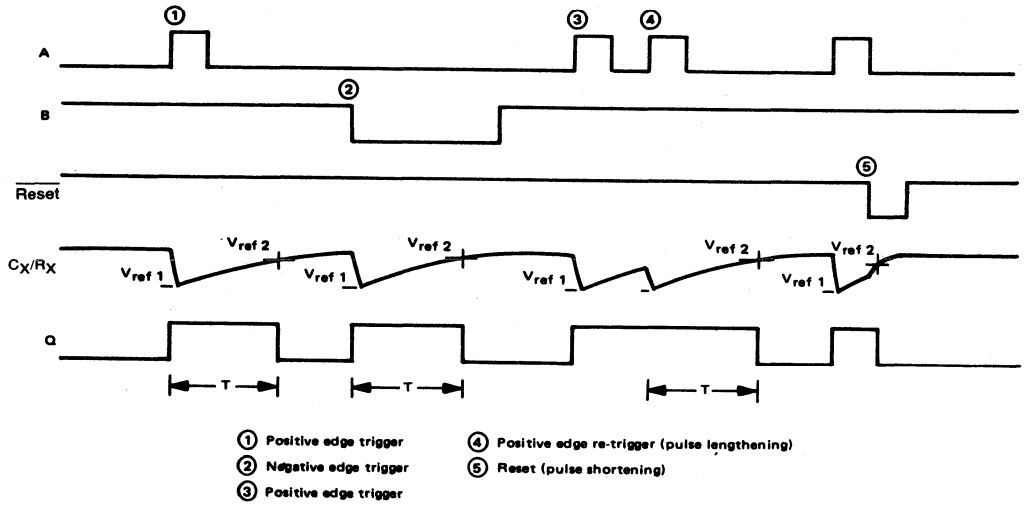


FIGURE 9 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE



THEORY OF OPERATION

FIGURE 10 — Timing Operation



6

TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{Reset}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\ 2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③ followed by another valid trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at C_X/R_X will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

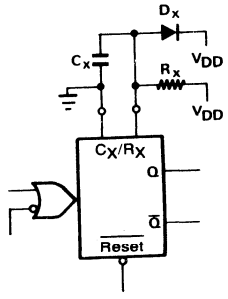
The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{Reset}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the reset latch will clear, and will then be ready to accept another pulse. If the $\overline{Reset}$ input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{Reset}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

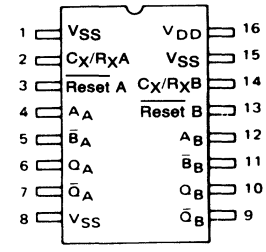
Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than (V_{DD}). (C)/(10 mA). For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) × (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X, connected as shown in Fig. 11.

FIGURE 11 – USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE



PIN ASSIGNMENT



6

TYPICAL APPLICATIONS

FIGURE 12 – RETRIGGERABLE MONOSTABLES CIRCUITRY

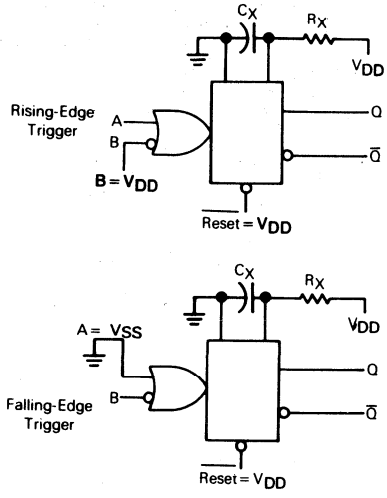


FIGURE 13 – NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

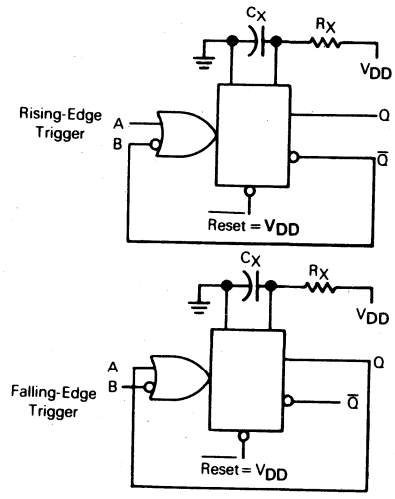
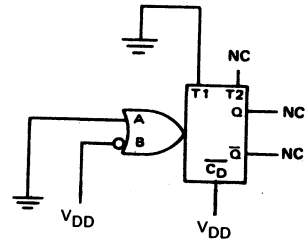


FIGURE 14 — CONNECTION OF UNUSED SECTIONS



6

MOTOROLA

MC14539B

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

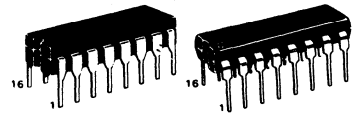
This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to l-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

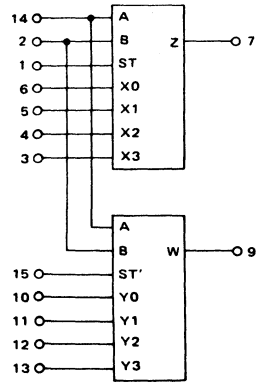
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS					OUTPUTS
B	A	X3 Y3	X2 Y2	X1 Y1	X0 Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5	–		pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.7 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

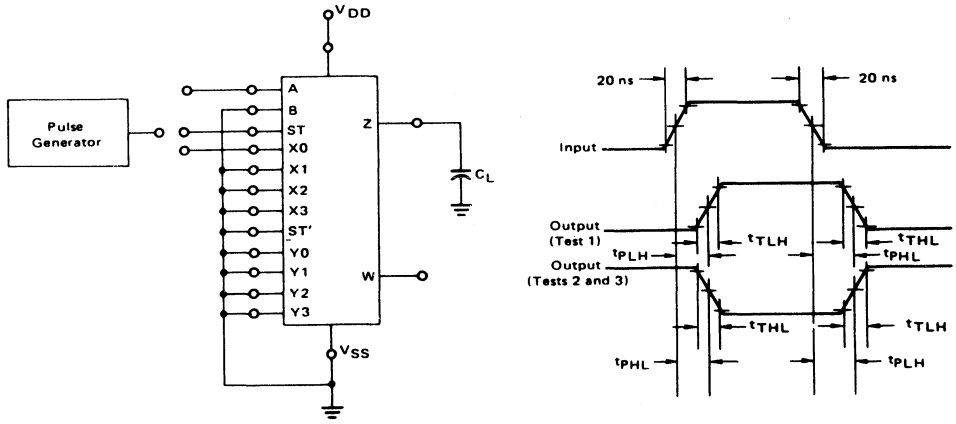
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
X, Y Input to Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 125 ns		5.0	–	210	420	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.55 ns/pF) C_L + 45 ns		15	–	70	140	
A Input to Output	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 140 ns		5.0	–	225	450	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
t_{PHL} = (1.7 ns/pF) C_L + 160 ns	t_{PHL}	5.0	–	245	490	ns
t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	230	
t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Strobe Input to Output	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 60 ns	t_{PHL}	5.0	–	145	290	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS

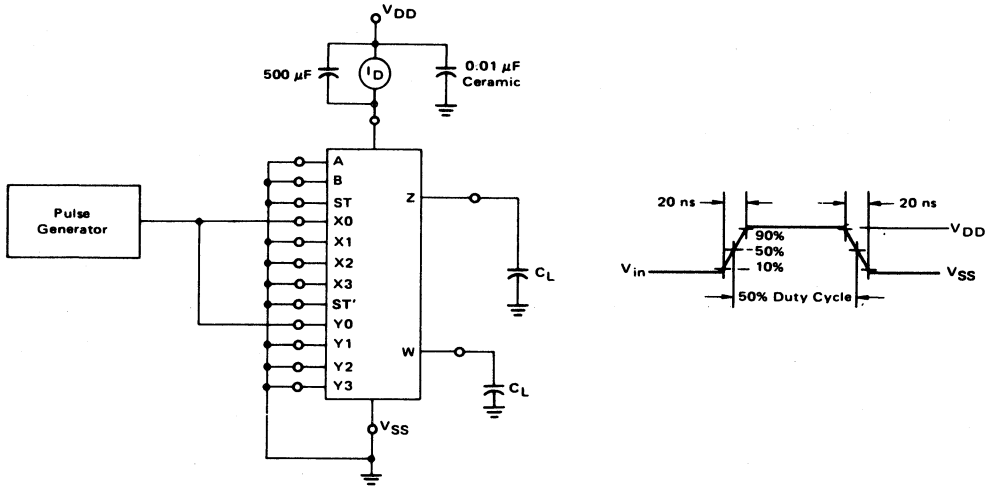


Input Connections for t_{TLH}, t_{THL}, t_{PHL}, t_{PLH}

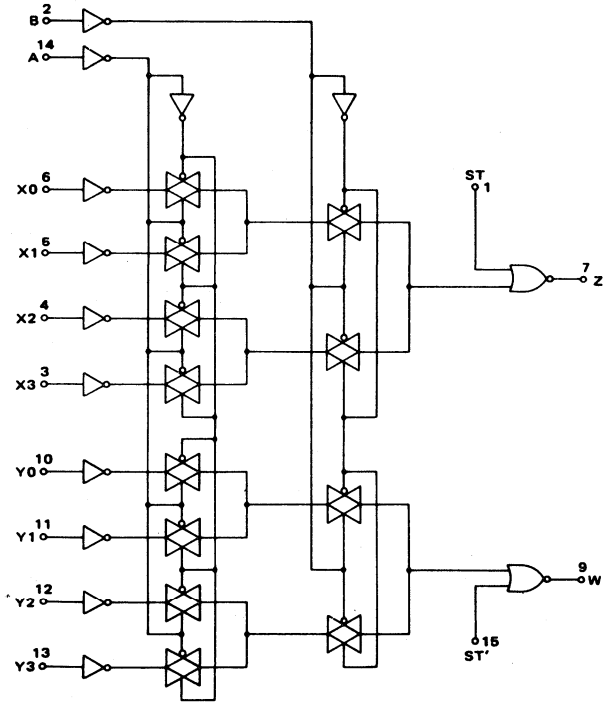
TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

6

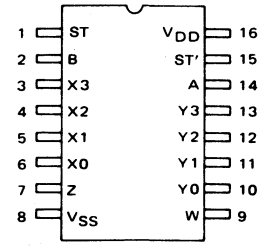
FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM



PIN ASSIGNMENT



6

MOTOROLA

MC14541B

PROGRAMMABLE TIMER

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/$\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow CLock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 = V_{DD})
  = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = V_{SS})

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

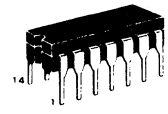
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	±45	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

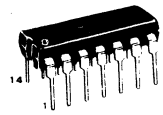
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

OSCILLATOR/TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 632



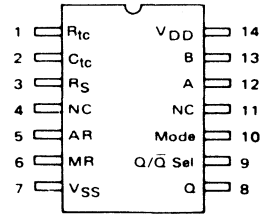
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



NC = No Connection

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−7.96	–	−6.42	−12.83	–	−4.49	–	
(V_{OH} = 9.5 Vdc)		10	−4.19	–	−3.38	−6.75	–	−2.37	–	
(V_{OH} = 13.5 Vdc)		15	−16.3	–	−13.2	−26.33	–	−9.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	–	4.0	8.0	–	2.8	–	
(V_{OL} = 1.5 Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−5.1	–	−4.27	−12.83	–	−3.5	–	
(V_{OH} = 9.5 Vdc)		10	−2.69	–	−2.25	−6.75	–	−1.85	–	
(V_{OH} = 13.5 Vdc)		15	−10.5	–	−8.8	−26.33	–	−7.22	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.24	–	1.04	3.12	–	0.85	–	
(V_{OL} = 0.5 Vdc)		10	3.18	–	2.66	8.0	–	2.18	–	
(V_{OL} = 1.5 Vdc)		15	12.4	–	10.4	31.2	–	8.50	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)										µAdc
		5.0	–	5.0	–	0.005	5.0	–	150	
(Pin 5 is High)	I_{DD}	10	–	10	–	0.010	10	–	300	
Auto Reset Disabled		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)										µAdc
		5.0	–	20	–	0.005	20	–	150	
(Pin 5 is High)	I_{DD}	10	–	40	–	0.010	40	–	300	
Auto Reset Disabled		15	–	80	–	0.015	80	–	600	
Auto Reset Quiescent Current										µAdc
	I_{DDR}	10	–	250	–	30	250	–	1500	
(Pin 5 is low)		15	–	500	–	82	500	–	2000	
Supply Current**† (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 µA/kHz) f + I_{DD}							µAdc
		10	I_D = (0.8 µA/kHz) f + I_{DD}							
		15	I_D = (1.2 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†When using the on chip oscillator the total supply current (in µAdc) becomes: $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in µA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see fig. 3) Dissipation during power-on with automatic reset enabled is typically 50µA @ V_{DD} = 10Vdc.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

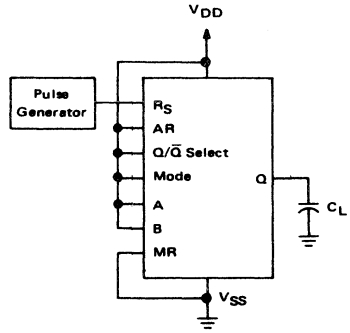
SWITCHING CHARACTERISITCS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay, Clock to Q (2^8 Output)	t_{PLH} t_{PHL}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns		5.0	–	3.5	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	–	1.25	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	–	0.9	2.9	
Propagation Delay, Clock to Q (2^{16} Output)	t_{PHL} t_{PLH}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	–	3.5	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns		15	–	2.5	7.5	
Clock Pulse Width	$t_{WH(cl)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.5	0.75	MHz
		10	–	4.0	2.0	
		15	–	6.0	3.0	
MR Pulse Width	$t_{WH(R)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Master Reset Removal Time	t_{rem}	5.0	420	210	—	ns
		10	200	100	—	
		15	200	100	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



(R_{tc} and C_{tc} outputs are left open)

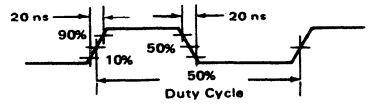
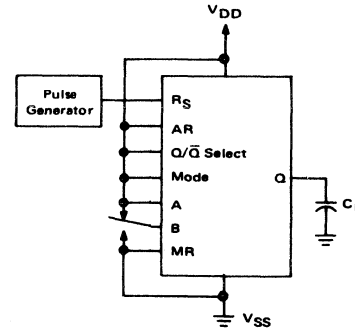
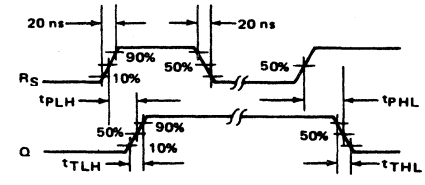


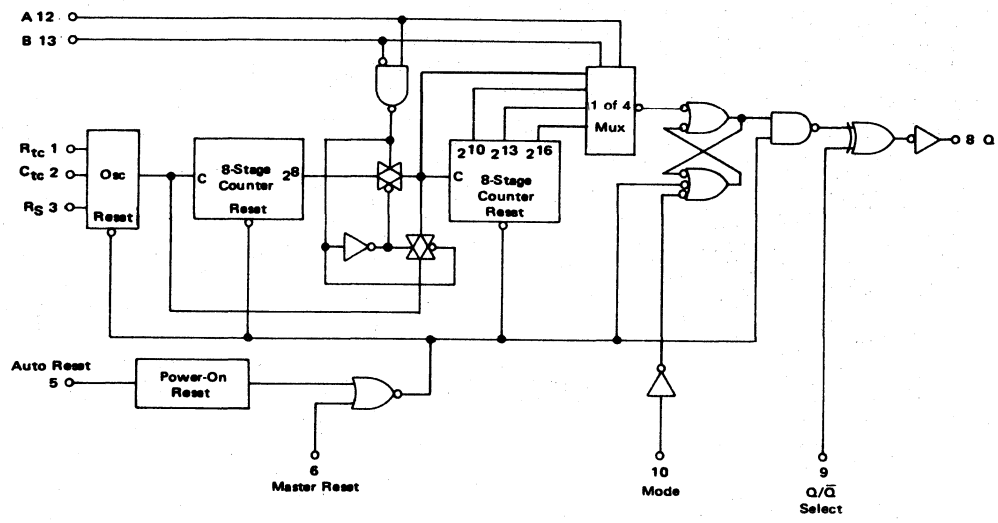
FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





6

EXPANDED BLOCK DIAGRAM



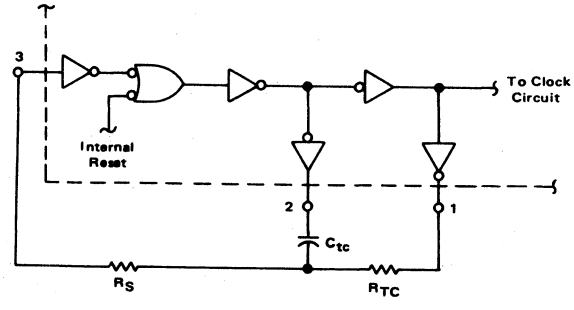
FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/$\overline{Q}$, 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

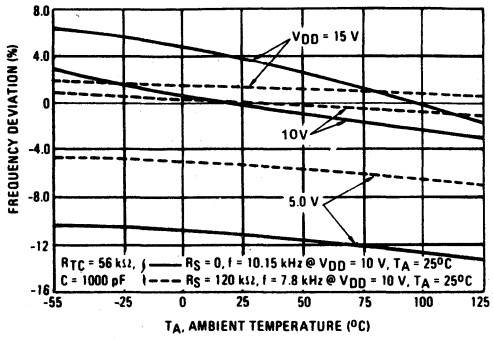
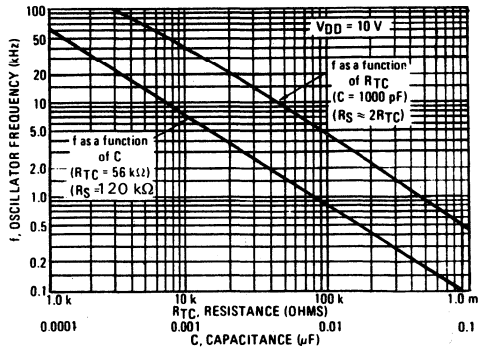


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C_{TC}



OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \qquad \text{if } (1\text{ kHz} \leq f \leq 100\text{ kHz})$$

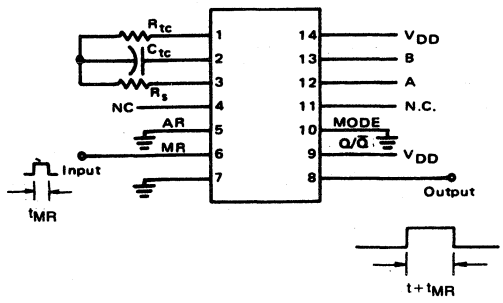
and $R_S \approx 2\,R_{tc}$ where $R_S \geq 10\text{ k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

DIGITAL TIMER APPLICATION



When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

6

MOTOROLA

MC14548B

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL (RETRIGGERABLE, RESETTABLE) MONOSTABLE MULTIVIBRATOR

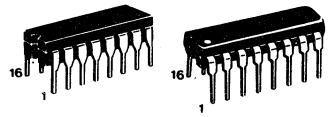
DUAL MONOSTABLE MULTIVIBRATOR
(RETRIGGERABLE, RESETTABLE)

The MC14548B is identical in pinout to the MC14538B and the MC14528B.

This dual monostable multivibrator may be triggered by either the positive (A input) or the negative edge (B input) of an input pulse, and produces an output pulse over a wide range of pulse widths. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the Q output low and $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

Due to minimal output pulse width variation over temperature, the MC14548 is recommended for new designs in lieu of the MC14528 or MC14538. However, the MC14548 requires more quiescent current than the MC14528 or MC14538.

- Unlimited Rise and Fall Times Allowed on the A Trigger Input
- Output Pulse Width is Independent of the Trigger Pulse Width
- Latched Trigger and Reset Inputs
- Supply Voltage Range = 3.0 to 18.0 Vdc
- For pulse widths < 1 μs, use the HC4538



L SUFFIX
CERAMIC PACKAGE
CASE 620

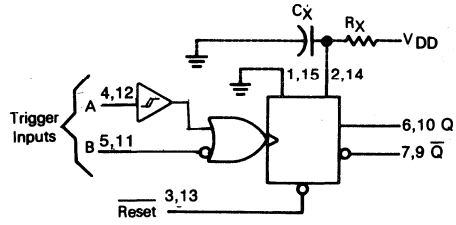
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

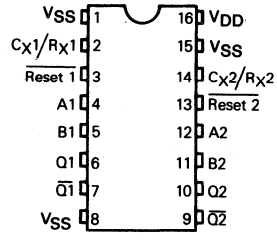
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)

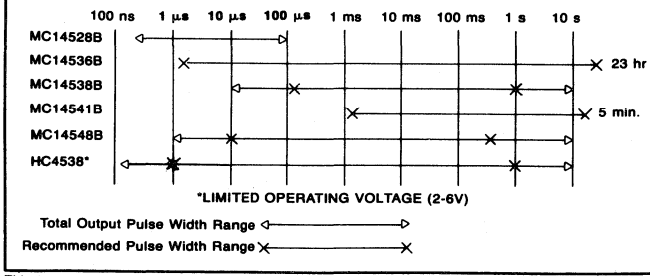


V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

PIN ASSIGNMENT



ONE-SHOT SELECTION GUIDE



FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{Q}$
H	⌐	H	⌐	⌐
H	L	⌐	⌐	⌐
H	⌐ ¬	L	Not Triggered	
H	H	⌐ ¬	Not Triggered	
H	L, H, ¬	H	Not Triggered	
H	L	L, H, ⌐	Not Triggered	
L	X	X	L	H
¬ ⌐	X	X	Not Triggered	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
		Vdc	Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	V
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	V
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current	I_{OH}									mA
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current, Pin 2 or 14	I_{in}	15	—	±0.05	—	± 0.00001	±0.05	—	±0.5	µA
Input Current, Other Inputs	I_{in}	15	—	±0.1	—	± 0.00001	±0.1	—	±1.0	µA
Input Capacitance, Pin 2 or 14	C_{in}	—	—	—	—	25	—	—	—	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current, Standby State (AL Devices) (Per Package)	I_{DD}	5.0	—	60	—	50	60	—	170	µA
Q = Low, $\overline{Q}$ = High		10	—	85	—	75	85	—	220	
		15	—	110	—	80	110	—	270	
Quiescent Current, Standby State (CL/CP Devices) (Per Package)	I_{DD}	5.0	—	80	—	50	80	—	220	µA
Q = Low, $\overline{Q}$ = High		10	—	105	—	75	105	—	270	
		15	—	130	—	80	130	—	370	
Quiescent Current, Active State (ALL) (Per Package)	I_{DD}	5.0	—	2.0	—	.04	.20	—	2.0	mA
$\overline{Q}$ = Low, Q = High		10	—	2.0	—	.08	.45	—	2.0	
		15	—	2.0	—	.13	.70	—	2.0	

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ #	Max	Unit
Output Transition Time Q or $\overline{Q}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	200 100 80	400 200 160	ns
$\overline{Reset}$ to Q or $\overline{Q}$		5.0 10 15	— — —	185 90 75	370 180 150	ns
Input Pulse Width A, B or $\overline{Reset}$	$t_{w(H)}$, $t_{w(L)}$	5.0 10 15	50 30 20	25 15 10	— — —	ns
Retrigger Time, To Extend Pulse Input A or B (C_X in μf) $K_1 = 2000\left(\frac{V}{\mu F}\right)$, $K_2 = 13\left(\frac{V}{\mu F}\right)$	t_{rx}	5.0 10 15	$0.75 + \frac{K_1 C_X}{V_{DD}+K_2 C_X}$	— — —	— — —	μs
Retrigger Time, To Issue New Pulse Input A or B	t_{rr}	5.0 10 15	0 0 0	— — —	— — —	ns
Recovery Time $\overline{Reset}$ Inactive to A or B	t_{rec}	5.0 10 15	20 10 6	11.6 4.8 3.0	— — —	ns
Input Rise and Fall Time $\overline{Reset}$	t_r, t_f	5.0 10 15	— — —	— — —	15 5 4	μs
B Input		5.0 10 15	— — —	286 40 22	200 25 15	
A Input		5.0 10 15	No Limit			
Output Pulse Width — Q or $\overline{Q}$ C_X=0.001 μF R_X= 10 kΩ	T	5.0 10 15	9 8 8	12.6 11.8 11.6	15 14 14	μs
C_X=0.01 μF R_X= 10 kΩ		5.0 10 15	82 69 61	90 77 73	100 85 80	μs
C_X=1.0 μF R_X= 100 kΩ		5.0 10 15	64 62 62	71 68 68	78 75 75	ms
Pulse Width Match between circuits in the same package C_X=0.1 μF R_X= 100 kΩ	$\frac{T1 - T2}{T1}$	5.0 10 15	— — —	±1 ±1 ±1	— — —	%

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	*	kΩ
External Timing Capitance	C_X	–	0	–	*	pF

* The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the MC14548B, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 10 mA. Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ.

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (Pins 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponsing multivibrator when there is a low voltage level on the A1 or A2 input.

$\overline{\text{Reset 1}}$, $\overline{\text{Reset 2}}$ (Pins 3, 13) — Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the $\overline{Q}$ output is set to a high voltage.

C_X1/R_X1 and C_X2/R_X2 (Pins 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram).

OUTPUTS

Q1, Q2 (Pins 6,10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q1}$, $\overline{Q2}$ (Pins 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

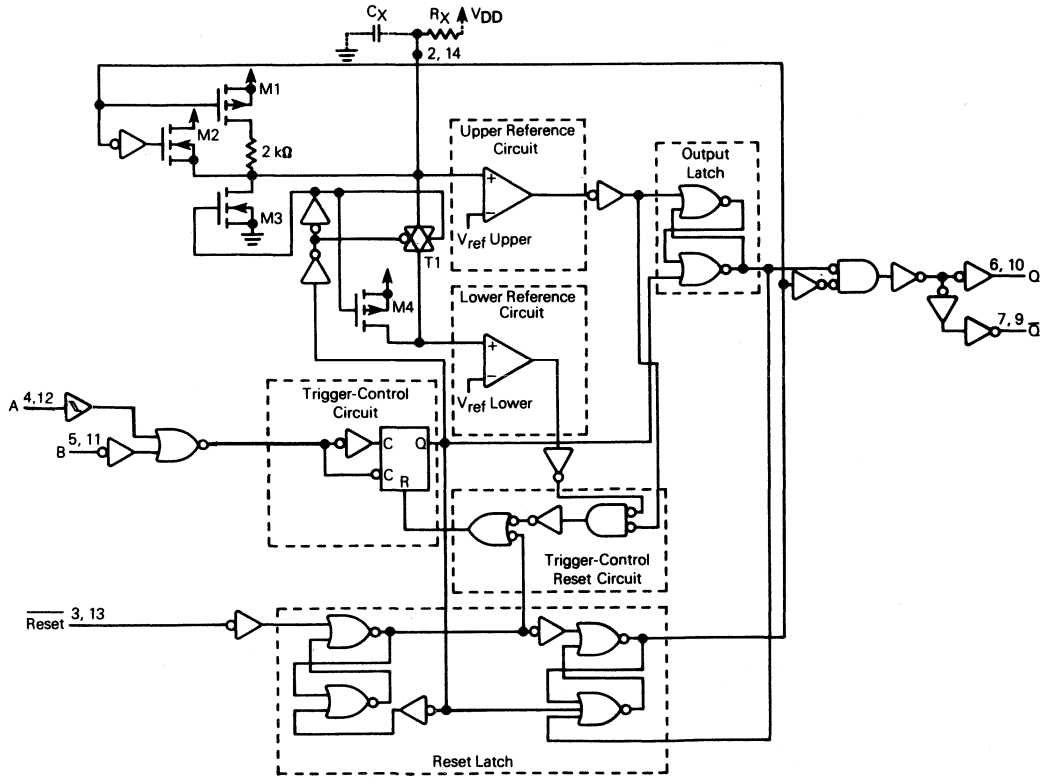
POWER

V_{DD} (Pin 16) — Most positive supply potential. This voltage may range from 3 to 18 volts with respect to V_{SS}.

V_{SS} (Pins 1, 8, 15) — Most negative supply potential (usually ground).

NOTE: All 3 pins must be connected externally to the power supply to insure proper performance.

FIGURE 1 — FUNCTION DIAGRAM
(½ the device)



CIRCUIT OPERATION

Figure 4 shows the 14548B configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1). In the quiescent state, the external timing capacitor, C_X, is charged to V_{DD}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower ≈ 1/3 V_{DD}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper ≈ 2/3 V_{DD}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the function diagram (Figure 1) and the timing diagram (Figure 2).

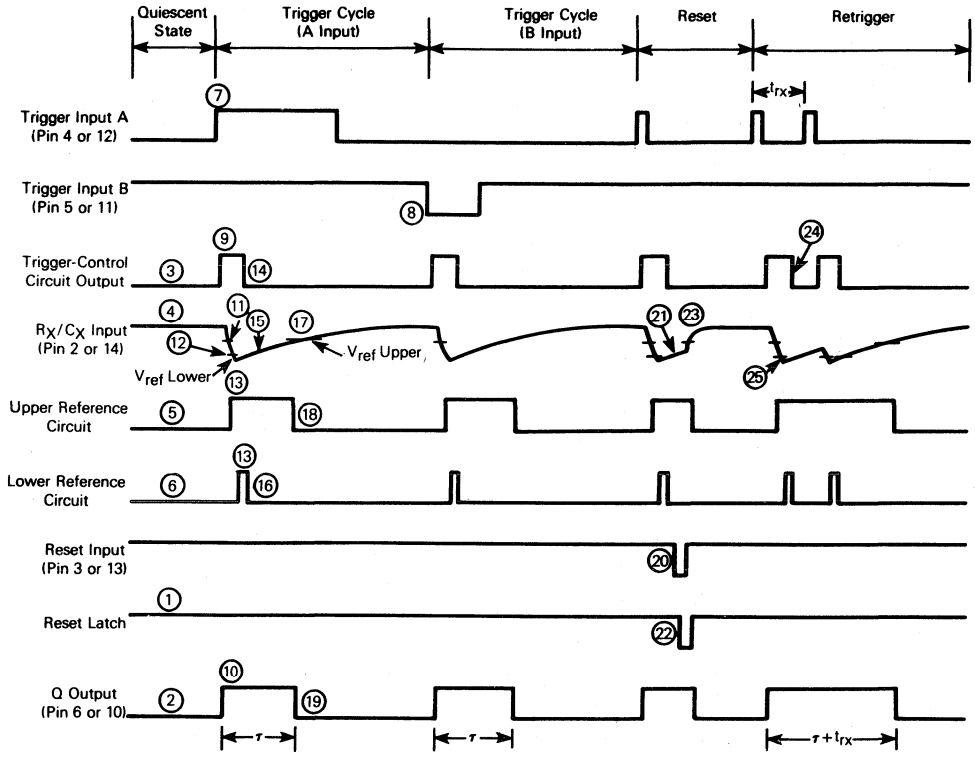
QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 2). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 2).

The output of the trigger-control is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{DD} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{DD} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

FIGURE 2 — TIMING DIAGRAM



TRIGGER OPERATION

The 14548B is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 14548B to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{DD}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 14548B to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the $\overline{\text{Reset}}$ pin always forces the Q output of the 14548B to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{DD} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 4), the MC14548B may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rx} (Figure 1) is a function of internal propagation delays and the discharge time of C_X.

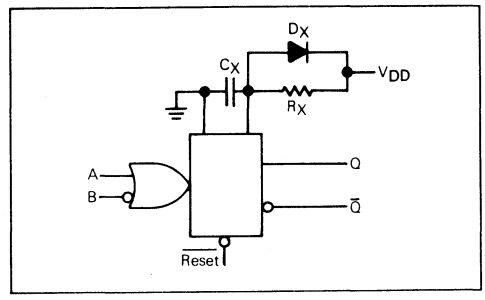
Figure 5 shows the device configured in the non-triggerable mode.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the 14548B because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{DD} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 10 mA, therefore, the turn-off time of the V_{DD} power supply must not be faster than $t = V_{DD} \bullet C_X/(10\ mA)$. For example, if V_{DD} = 5 V and C_X = 15 μF, the V_{DD} supply must turn off no faster than $t = (5\ V) \bullet (15\ \mu F)/10\ mA$ = 7.5 ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14548B may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected as shown in Figure 3.

FIGURE 3 — DISCHARGE PROTECTION DURING POWER DOWN



TYPICAL APPLICATIONS

FIGURE 4 — RETRIGGERABLE MONOSTABLE CIRCUITRY

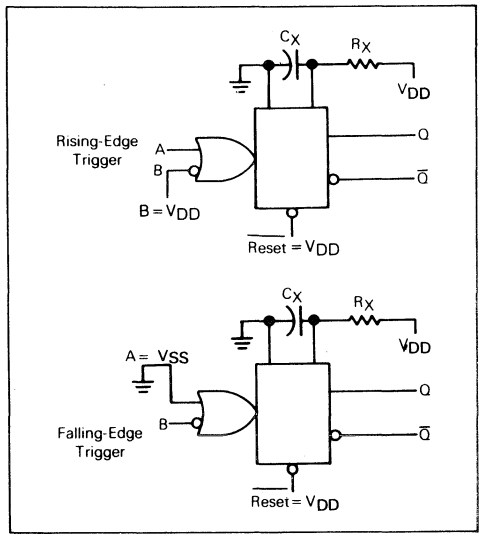
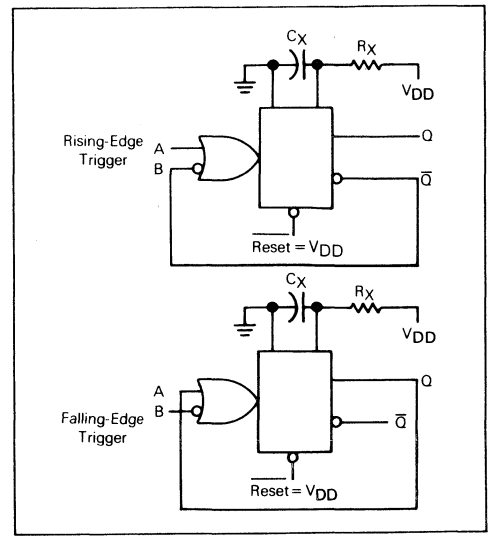


FIGURE 5 — NONRETRIGGERABLE MONOSTABLE CIRCUITRY



SWITCHING WAVEFORMS

FIGURE 6

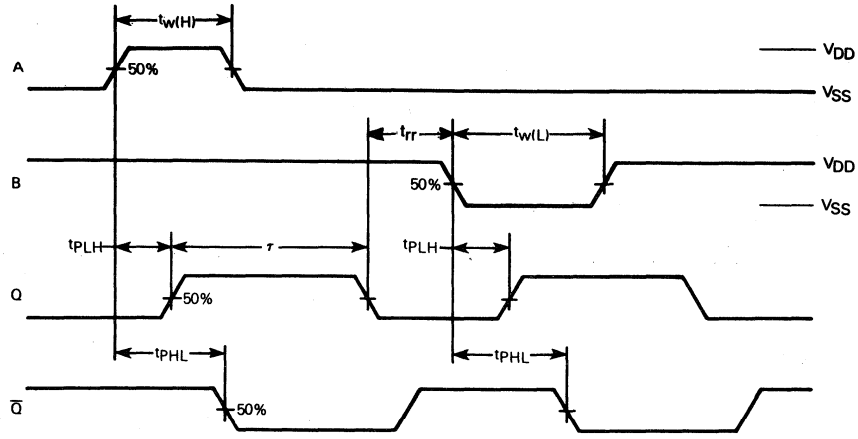


FIGURE 7

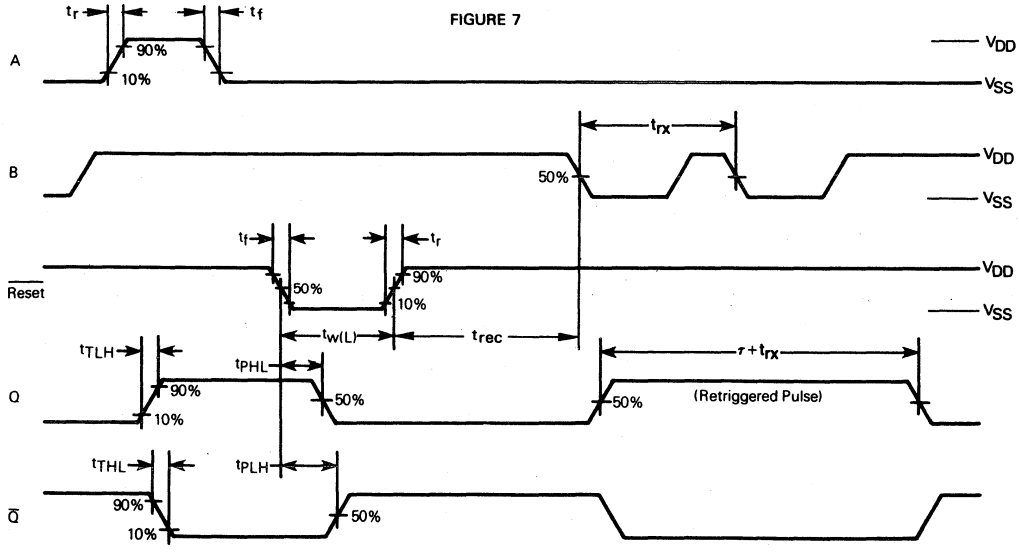
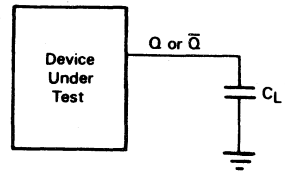


FIGURE 8 — TEST CIRCUIT



6

MOTOROLA

MC14551B

ANALOG MULTIPLEXER/DEMULTIPLEXER

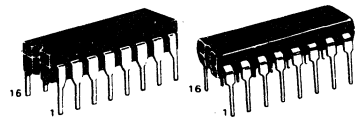
The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ √Cycle, f ≥ 1 kHz typical
- For Lower R_{ON}, Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXER/ DEMULTIPLEXER



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

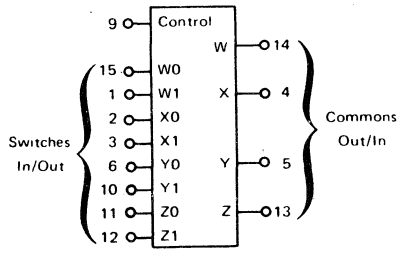
A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input & V_{EE} for Switch I/O)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

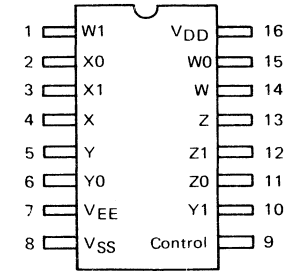
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

PIN ASSIGNMENT



Note: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

6

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3 \geq V_{SS} \geq V_{EE}$	3	18	3	—	18	3	18	V
Quiescent Current Per Package (AL Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	5	—	0.005	5	—	150	μA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	10	—	0.010	10	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	20	—	0.015	20	—	600	
Quiescent Current Per Package (CL/CP Device)	I_{DD}	5	Control Inputs: $V_{in} = V_{SS}$ or V_{DD},	—	20	—	0.005	20	—	150	μA
		10	Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$,	—	40	—	0.010	40	—	300	
		15	and $\Delta V_{switch} \leq 500$ mV**	—	80	—	0.015	80	—	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5	T_A = 25°C only	Typical			(0.07 μA/kHz)f + I_{DD}				μA
		10	(The channel component,				(0.20 μA/kHz)f + I_{DD}				
		15	$(V_{in} - V_{out})/R_{on}$, is not included.)				(0.36 μA/kHz)f + I_{DD}				
CONTROL INPUT (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5	R_{on} = per spec,	—	1.5	—	2.25	1.5	—	1.5	V
		10	I_{off} = per spec	—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5	R_{on} = per spec,	3.5	—	3.5	2.75	—	3.5	—	V
		10	I_{off} = per spec	7.0	—	7.0	5.50	—	7.0	—	
		15		11.0	—	11.0	8.25	—	11.0	—	
Input Leakage Current (AL Device)	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Leakage Current (CL/CP Device)	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN - W, X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No load	—	—	—	10	—	—	—	μV
ON Resistance (AL Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	800	—	250	1050	—	1300	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	400	—	120	500	—	550	
		15	and V_{in} = 0 to V_{DD} (Switch)	—	220	—	80	280	—	320	
ON Resistance (CL/CP Device)	R_{on}	5	$\Delta V_{switch} \leq 500$ mV**,	—	880	—	250	1050	—	1200	Ω
		10	$V_{in} = V_{IL}$ or V_{IH} (Control),	—	450	—	120	500	—	520	
		15	and V_{in} = 0 to V_{DD} (Switch)	—	250	—	80	280	—	300	
Δ ON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (AL Device) (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Off-Channel Leakage Current (CL/CP Device) (Figure 8)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±300	—	±0.05	±300	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	—	Pins Not Adjacent	—	—	—	0.15	—	—	—	pF
		—	Pins Adjacent	—	—	—	0.47	—	—	—	

* T_{low} = −55°C for AL Device, −40° for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$, $V_{EE} \leq V_{SS}$)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	—	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	—	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	—	12	30	
Control Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}					ns
$V_{EE} = V_{SS}$ (Figure 4)		5.0	—	350	875	
		10	—	140	350	
		15	—	100	250	
Second Harmonic Distortion R_L = 10 kΩ, f = 1 kHz, $V_{in} = 5\ V_{p-p}$	—	10	—	0.07	—	%
Bandwidth (Figure 5) R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})$ p-p, 20 Log $\frac{V_{out}}{V_{in}}$ = −3 dB, C_L = 50 pF	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})$ p-p, f_{in} = 55 MHz	—	10	—	−50	—	dB
Channel Separation (Figure 6) R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})$ p-p, f_{in} = 3 MHz	—	10	—	−50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 kΩ, R_L = 10 kΩ, Control $t_r = t_f$ = 20 ns	—	10	—	75	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

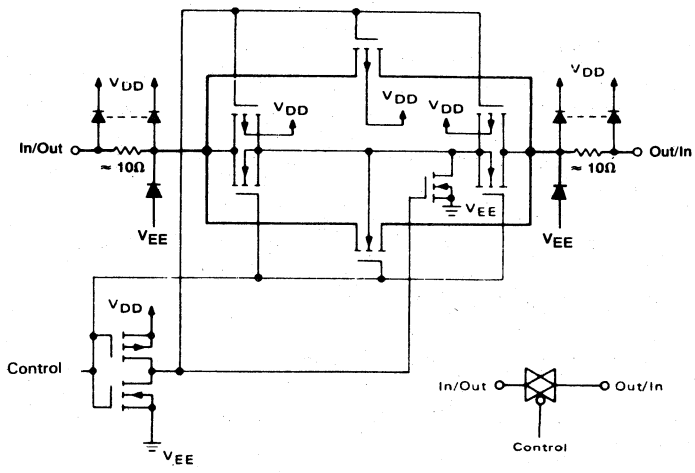
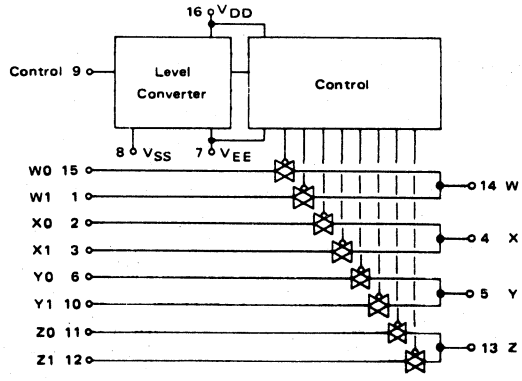


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 3 — ΔV ACROSS SWITCH

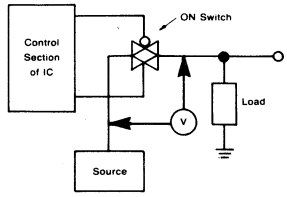


FIGURE 4 — PROPAGATION DELAY TIMES, CONTROL TO OUTPUT

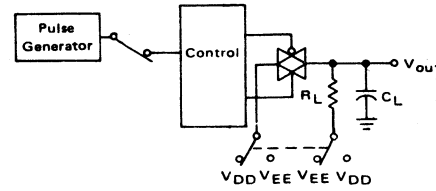


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

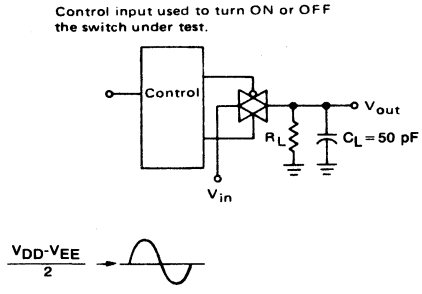


FIGURE 6 — CHANNEL SEPARATION (Adjacent Channels Used for Setup)

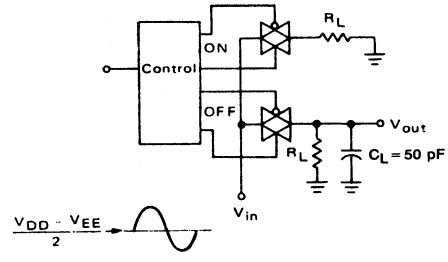


FIGURE 7 — CROSSTALK, CONTROL INPUT TO COMMON O/I

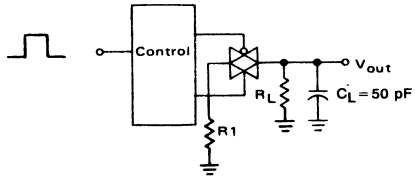
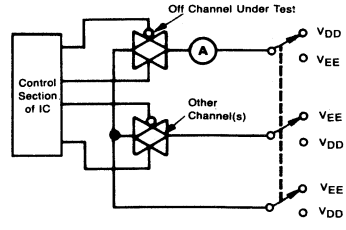
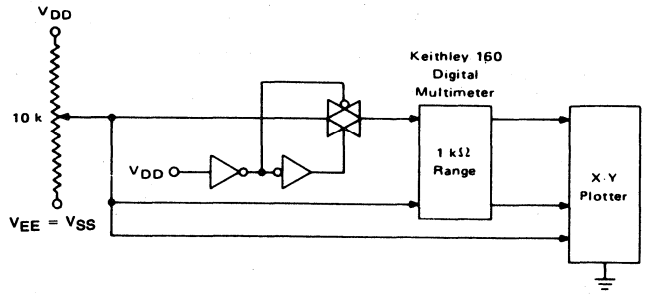


FIGURE 8 — OFF CHANNEL LEAKAGE



6

FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ –7.5V

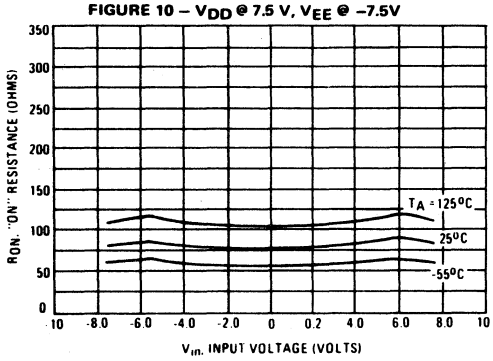


FIGURE 11 – V_{DD} @ 5.0V, V_{EE} @ –5.0 V

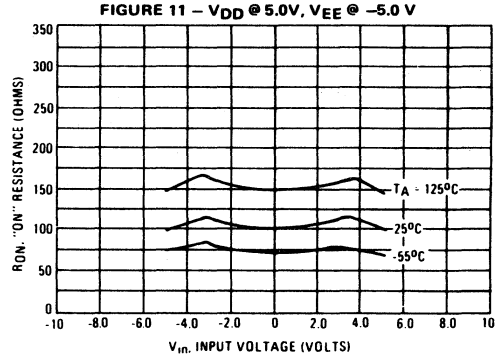


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ –2.5 V

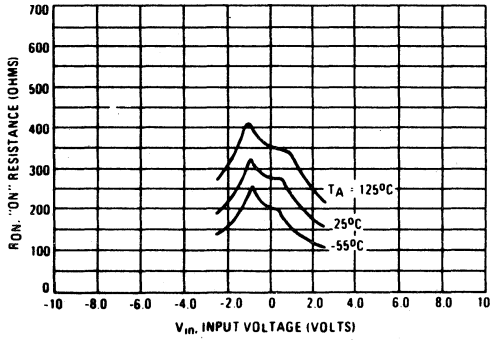
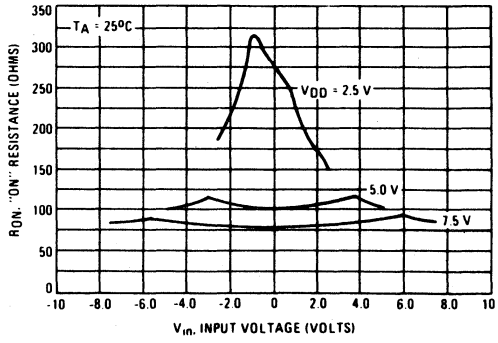


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$



6

APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5 volt maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5 volt maximum swing below V_{SS}. The example shows a ±4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 volts, V_{SS} = +5 volts, and V_{EE} = −3 volts is acceptable. See the table below.

FIGURE A — APPLICATION EXAMPLE

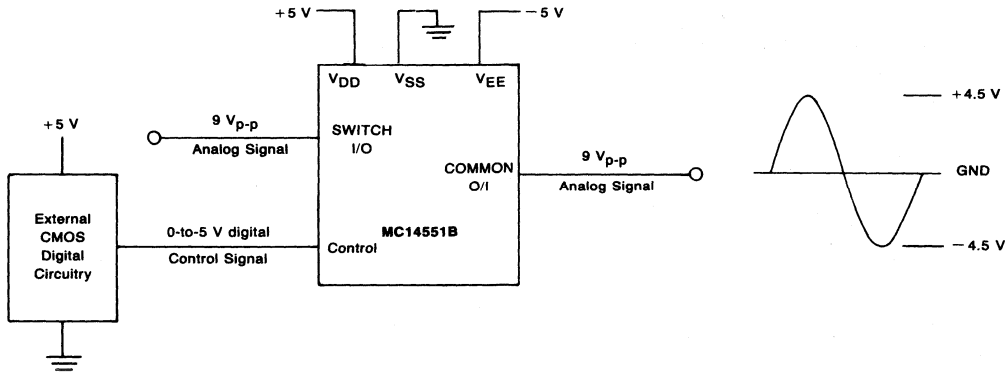
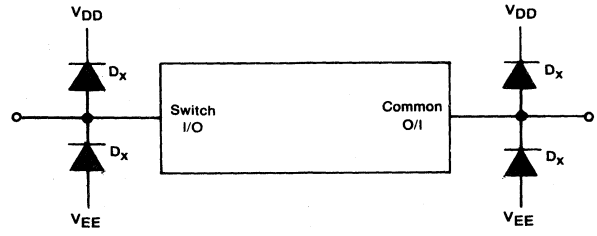


FIGURE B — EXTERNAL SCHOTTKY OR GERMANIUM CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low in Volts	Maximum Analog Signal Range in Volts
+8	0	−8	+8/0	+8 to −8 = 16 V_{p-p}
+5	0	−12	+5/0	+5 to −12 = 17 V_{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V_{p-p}
+5	0	−5	+5/0	+5 to −5 = 10 V_{p-p}
+10	+5	−5	+10/+5	+10 to −5 = 15 V_{p-p}

MOTOROLA

MC14553B

THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient), per Pin	±10	mA
I_{out}	Output Current (DC or Transient), per Pin	+20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

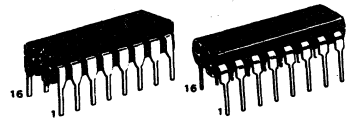
INPUTS				
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0	⌐¬	0	0	No Change
0	¬⌐	0	0	Advance
0	X	1	X	No Change
0	1	⌐¬	0	Advance
0	1	¬⌐	0	No Change
0	0	X	X	No Change
0	X	X	¬	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

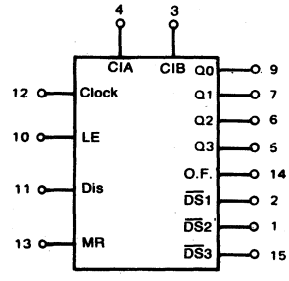
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
$V_{in}=V_{DD}$ or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	
$V_{in}=0$ or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
($V_O=4.5$ or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
($V_O=9.0$ or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
($V_O=13.5$ or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									
($V_O=0.5$ or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
($V_O=1.0$ or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
($V_O=1.5$ or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current (AL Device)	I_{OH}									mAdc
($V_{OH}=4.6$ Vdc) Source - Pin 3		5.0	−0.25	—	−0.20	−0.36	—	0.14	—	
($V_{OH}=9.5$ Vdc)		10	−0.62	—	−0.50	−0.9	—	0.35	—	
($V_{OH}=13.5$ Vdc)		15	−1.8	—	−1.5	−3.5	—	1.1	—	
($V_{OH}=4.6$ Vdc) Source - Other Outputs		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
($V_{OH}=9.5$ Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
($V_{OH}=13.5$ Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
($V_{OL}=0.4$ Vdc) Sink - Pin 3	I_{OL}	5.0	0.5	—	0.4	0.88	—	0.28	—	
($V_{OL}=0.5$ Vdc)		10	1.1	—	0.9	2.25	—	0.65	—	
($V_{OL}=1.5$ Vdc)		15	1.80	—	1.5	8.8	—	1.20	—	
($V_{OL}=0.4$ Vdc) Sink - Other Outputs		5.0	3.0	—	2.5	4.0	—	1.6	—	
($V_{OL}=0.5$ Vdc)		10	6.0	—	5.0	8.0	—	3.5	—	
($V_{OL}=1.5$ Vdc)		15	18	—	15	20	—	10	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
($V_{OH}=4.6$ Vdc) Source - Pin 3		5.0	−0.2	—	−0.16	−0.36	—	−0.12	—	
($V_{OH}=9.5$ Vdc)		10	−0.5	—	−0.4	−0.9	—	−0.3	—	
($V_{OH}=13.5$ Vdc)		15	−1.4	—	−1.2	−3.5	—	−1.0	—	
($V_{OH}=4.6$ Vdc) Source-Other Outputs		5.0	−0.52	—	−0.44	0.88	—	−0.36	—	
($V_{OH}=9.5$ Vdc)		10	−1.3	—	−1.1	−2.25	—	−0.9	—	
($V_{OH}=13.5$ Vdc)		15	−3.6	—	−3.0	−8.8	—	−2.4	—	
($V_{OL}=0.4$ Vdc) Sink - Pin 3	I_{OL}	5.0	0.23	—	0.2	0.88	—	0.16	—	
($V_{OL}=0.5$ Vdc)		10	0.60	—	0.5	2.25	—	0.40	—	
($V_{OL}=1.5$ Vdc)		15	1.80	—	1.5	8.8	—	1.20	—	
($V_{OL}=0.4$ Vdc) Sink - Other Outputs		5.0	2.4	—	2.0	4.0	—	1.6	—	
($V_{OL}=0.5$ Vdc)		10	3.8	—	3.0	8.0	—	2.5	—	
($V_{OL}=1.5$ Vdc)		15	10	—	84	20	—	7.0	—	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	µAdc
Input Capacitance ($V_{in}=0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	5.0	—	0.010	5.0	—	150	µAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	—	50	—	0.010	50	—	375	µAdc
		10	—	100	—	0.020	100	—	750	
		15	—	200	—	0.030	200	—	1500	
Total Supply Current**† (Dynamic Plus Quiescent, Per Package) ($C_L=50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T=(0.35\ \mu A/kHz)\ f+I_{DD}$							µAdc
		10	$I_T=(0.85\ \mu A/kHz)\ f+I_{DD}$							
		15	$I_T=(1.50\ \mu A/kHz)\ f+I_{DD}$							

*$T_{low}=-55$°C for AL Device, −40°C for CL/CP Device.
$T_{high}=+125$°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, $V = (V_{DD}-V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

6

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	2a	t_{TLH},					ns
T_{TLH}, T_{THL} = (1.5 ns/pF) C_L + 25 ns		t_{THL}	5.0	—	100	200	
T_{TLH}, T_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	—	50	100	
T_{TLH}, T_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	—	40	80	
Clock to BCD Out	2a	t_{PLH},	5.0	—	900	1800	ns
		t_{PHL}	10	—	500	1000	
			15	—	200	400	
Clock to Overflow	2a	t_{PHL}	5.0	—	600	1200	ns
			10	—	400	800	
			15	—	200	400	
Reset to BCD Out	2b	t_{PHL}	5.0	—	900	1800	ns
			10	—	500	1000	
			15	—	300	600	
Clock to Latch Enable Setup Time	2b	t_{su}	5.0	600	300	—	ns
Master Reset to Latch Enable Setup Time			10	400	200	—	
			15	200	100	—	
Removal Time	2b	t_{rem}	5.0	−80	−200	—	ns
Latch Enable to Clock			10	−10	−70	—	
			15	0	−50	—	
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0	550	275	—	ns
			10	200	100	—	
			15	150	75	—	
Reset Pulse Width	2b	$t_{WH(R)}$	5.0	1200	600	—	ns
			10	600	300	—	
			15	450	225	—	
Reset Removal Time	—	t_{rem}	5.0	−80	−180	—	ns
			10	0	−50	—	
			15	20	−30	—	
Input Clock Frequency	2a	f_{cl}	5.0	—	1.5	0.9	MHz
			10	—	5.0	2.5	
			15	—	7.0	3.5	
Input Clock Rise Time	2b	t_{TLH}	5.0	No Limit			ns
			10				
			15				
Scan Oscillator Frequency	1	f_{osc}	5.0	—	1.5/C1	—	Hz
(C1 measured in μF)			10	—	4.2/C1	—	
			15	—	7.0/C1	—	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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FIGURE 1 — 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 3)

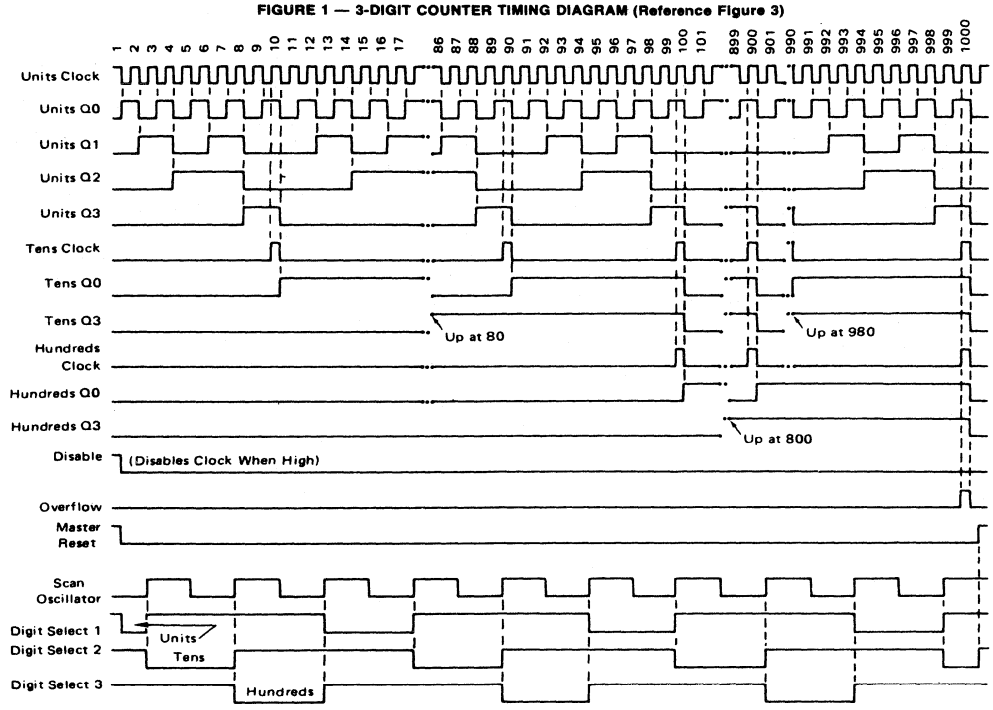
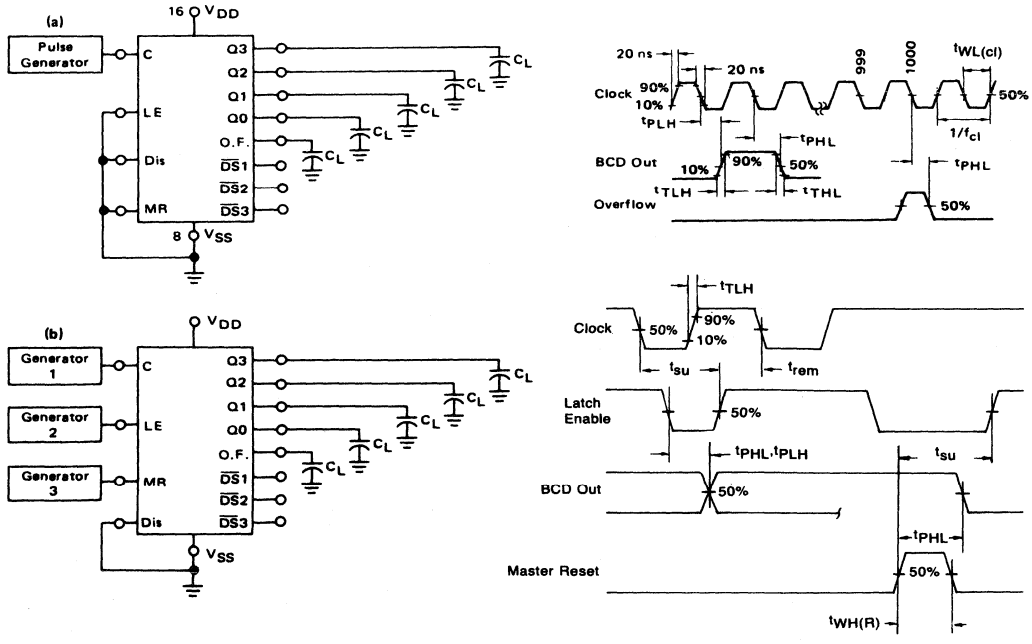


FIGURE 2 — SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



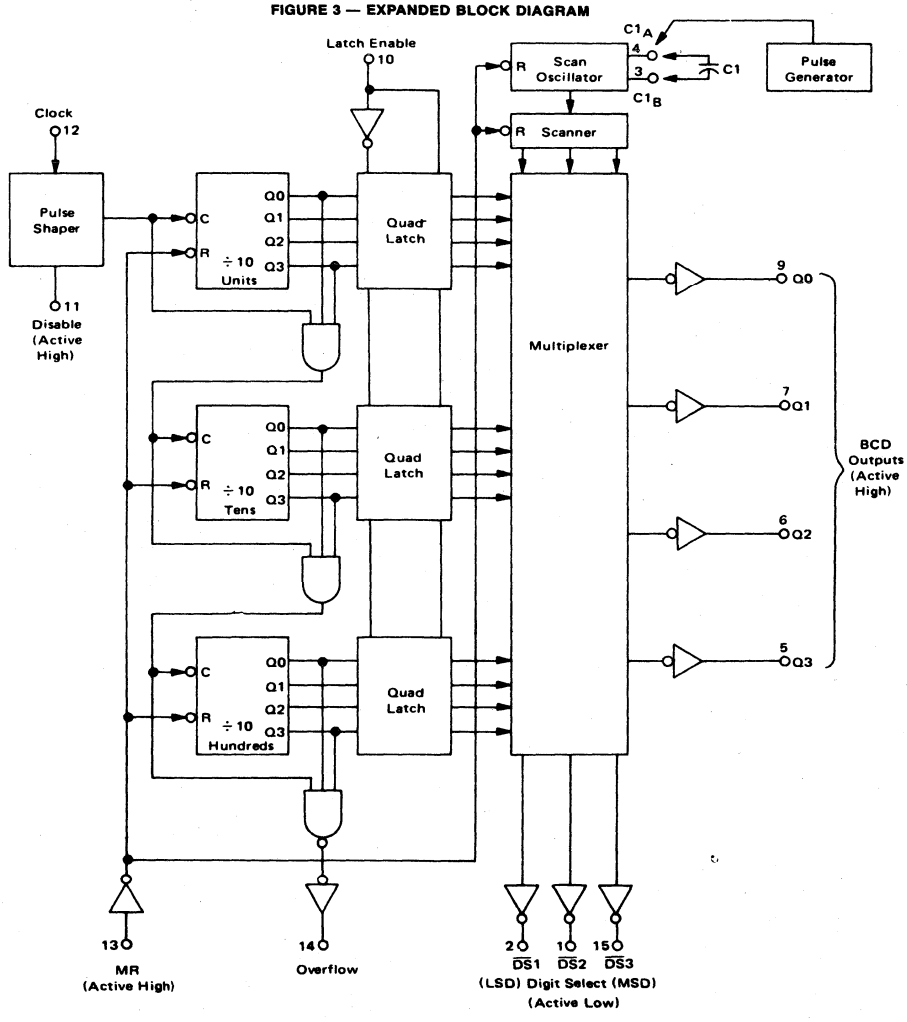
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 3, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

FIGURE 3 — EXPANDED BLOCK DIAGRAM



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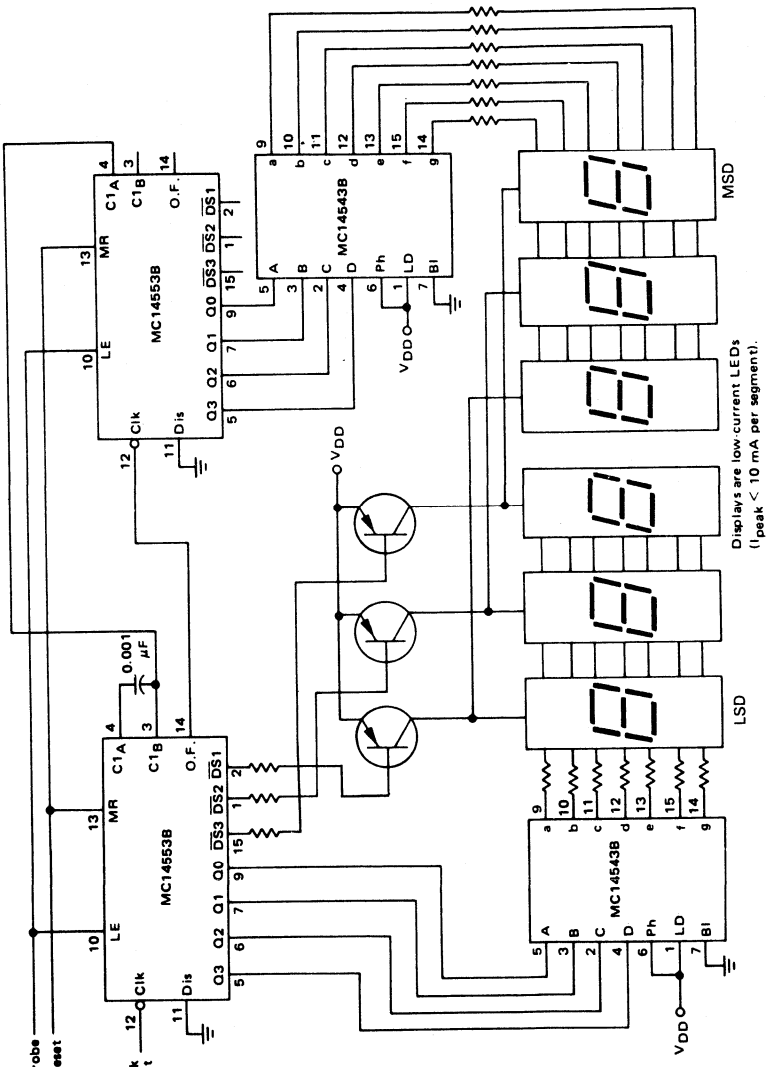


FIGURE 4 — SIX-DIGIT DISPLAY

MOTOROLA

MC14554B

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements.

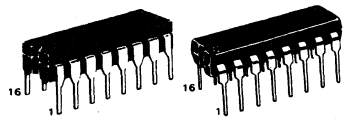
Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

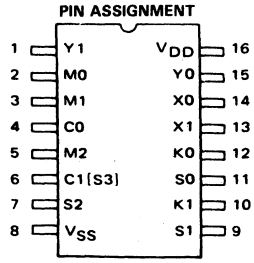
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

PIN ASSIGNMENT



EQUATIONS

$S = (X \times Y) + K + M$

Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).

Example:
Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0 µA/kHz) f + I_{DD}							
		15	I_T = (3.0 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.0035.

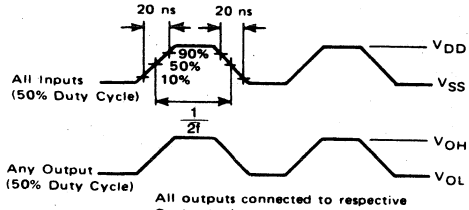
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
K0 to C0						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 185 ns		5.0	–	270	675	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	215	
M0 to S2						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 595 ns		5.0	–	680	1700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 247 ns		10	–	280	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	210	570	

*The formulas given are for the typical characteristics only at 25°C.

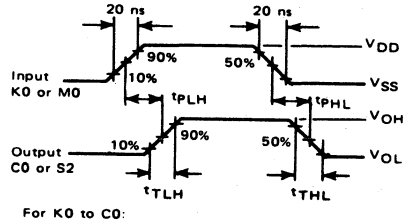
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION WAVEFORMS



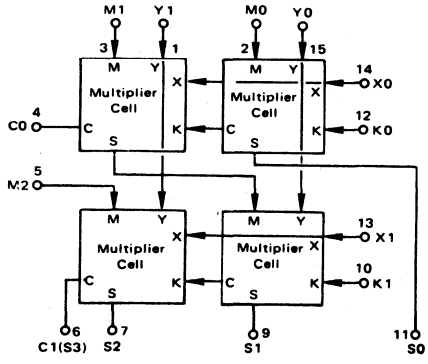
All outputs connected to respective C_L loads. f = system clock frequency

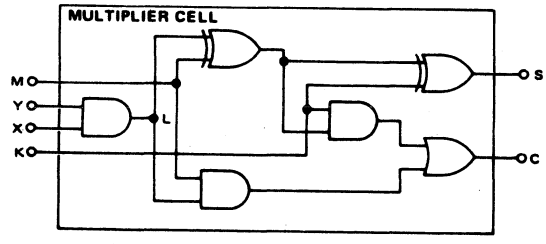
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



For K0 to C0:
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.
For M0 to S2:
Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

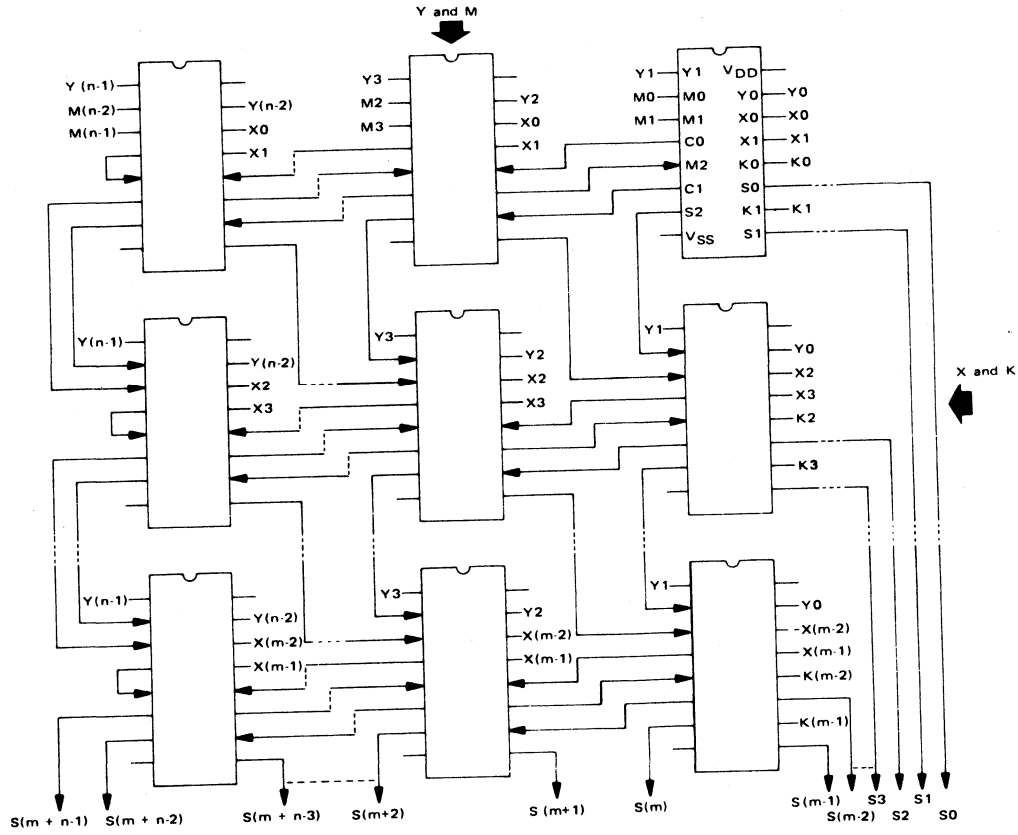
LOGIC DIAGRAM





EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



S = (X x Y) + K + M Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) · · · S2 S1 S0
X = X(m-1) X (m-2) · · · X2 X1 X0, Y = Y(n-1) Y(n-2) · · · Y2 Y1 Y0
K = K(m-1) K(m-2) · · · K2 K1 K0 and M = M(n-1) M(n-2) · · · M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

6

MOTOROLA

MC14555B
MC14556B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

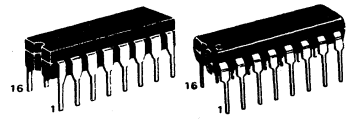
Active High Outputs – MC14555B
Active Low Outputs – MC14556B

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

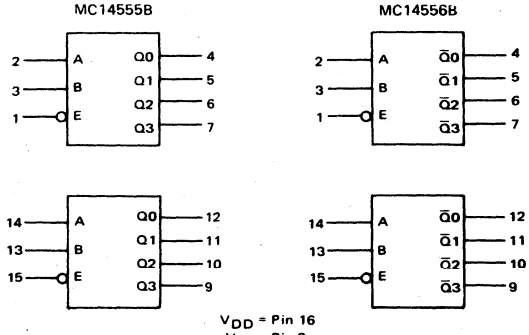
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q}3$	$\overline{Q}2$	$\overline{Q}1$	$\overline{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.7 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

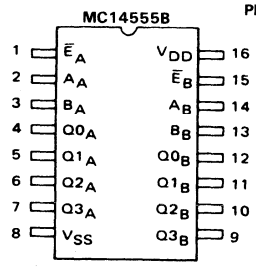
**The formulas given are for the typical characteristics only at 25°C.

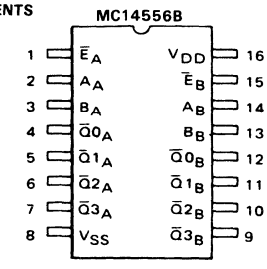
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

PIN ASSIGNMENTS





6

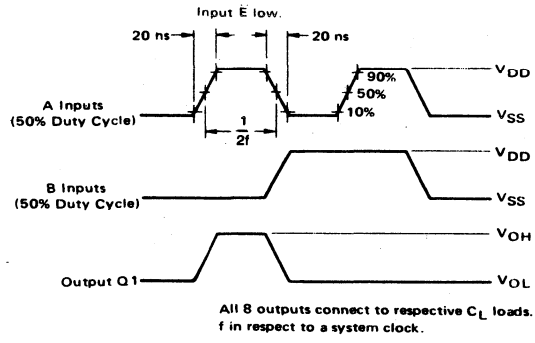
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time – A, B to Output	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns	t_{PHL}	5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Propagation Delay Time – E to Output	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	–	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	130	

*The formulas given are for the typical characteristics only at 25°C.

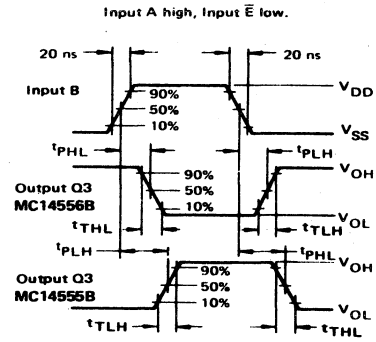
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

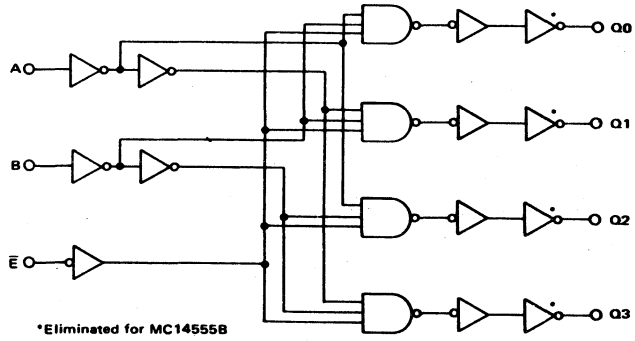


All 8 outputs connect to respective C_L loads.
f in respect to a system clock.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM
(1/2 of Dual)



*Eliminated for MC14555B

6

MOTOROLA

MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

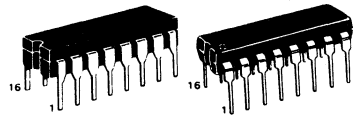
The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

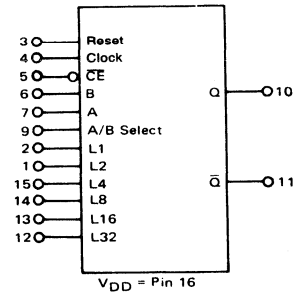
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LENGTH SELECT TRUTH TABLE

L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33 Bits
1	0	0	0	0	1	34-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
Rst	A/B	Clock	$\overline{CE}$	Q
0	0	↑	0	B
0	1	↑	0	A
0	0	1	↓	B
0	1	1	↓	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.75 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.5 µA/kHz) f + I_{DD}							
		15	I_T = (5.25 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

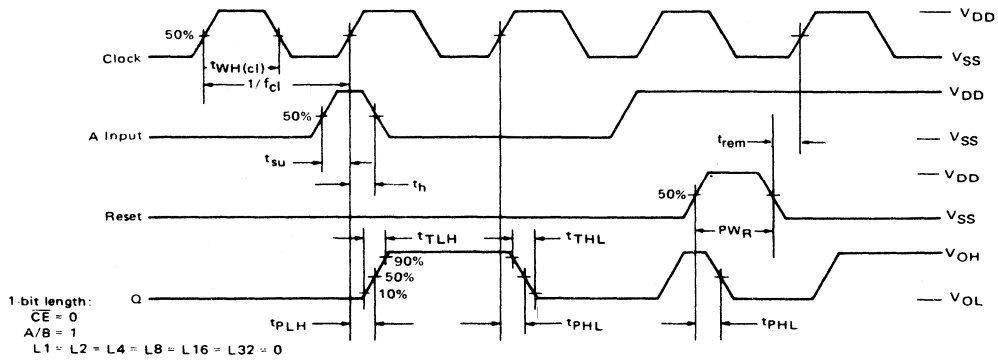
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Rise and Fall Time, Q or $\overline{Q}$ Output	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay, Clock or $\overline{CE}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	90	180	
Propagation Delay, Reset to Q or $\overline{Q}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 70 ns		15	—	95	190	
Pulse Width, Clock	$t_{WH(cl)}$	5	200	95	—	ns
		10	100	45	—	
		15	75	35	—	
Pulse Width, Reset	$t_{WH(rst)}$	5	300	150	—	ns
		10	140	70	—	
		15	100	50	—	
Clock Frequency (50% Duty Cycle)	f_{cl}	5	—	3.0	1.7	MHz
		10	—	7.5	5.0	
		15	—	13.0	6.7	
Setup Time, A or B to Clock or $\overline{CE}$	t_{su}					ns
Worst case condition: L1 = L2 = L4 = L8 = L16 = L32 = V_{SS} (Register Length)		5	700	350	—	
		10	290	130	—	
		15	145	85	—	
Best case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)		5	400	45	—	
		10	165	5	—	
		15	60	0	—	
Hold Time, Clock or $\overline{CE}$ to A or B	t_h					ns
Best case condition: L1 = L2 = L4 = L8 = L16 = L32 = V_{SS}		5	200	−150	—	
		10	100	−60	—	
		15	10	−50	—	
Worst case condition: L32 = V_{DD}, L1 through L16 = Don't Care (Any register length from 33 to 64)		5	400	50	—	
		10	185	25	—	
		15	85	22	—	
Rise and Fall Time, Clock	t_r, t_f	5	No Limit			—
		10				
		15				
Rise and Fall Time, Reset or $\overline{CE}$	t_r, t_f	5	—	—	15	μs
		10	—	—	5	
		15	—	—	4	
Removal Time, Reset to Clock or $\overline{CE}$	t_{rem}	5	160	80	—	ns
		10	80	40	—	
		15	70	35	—	

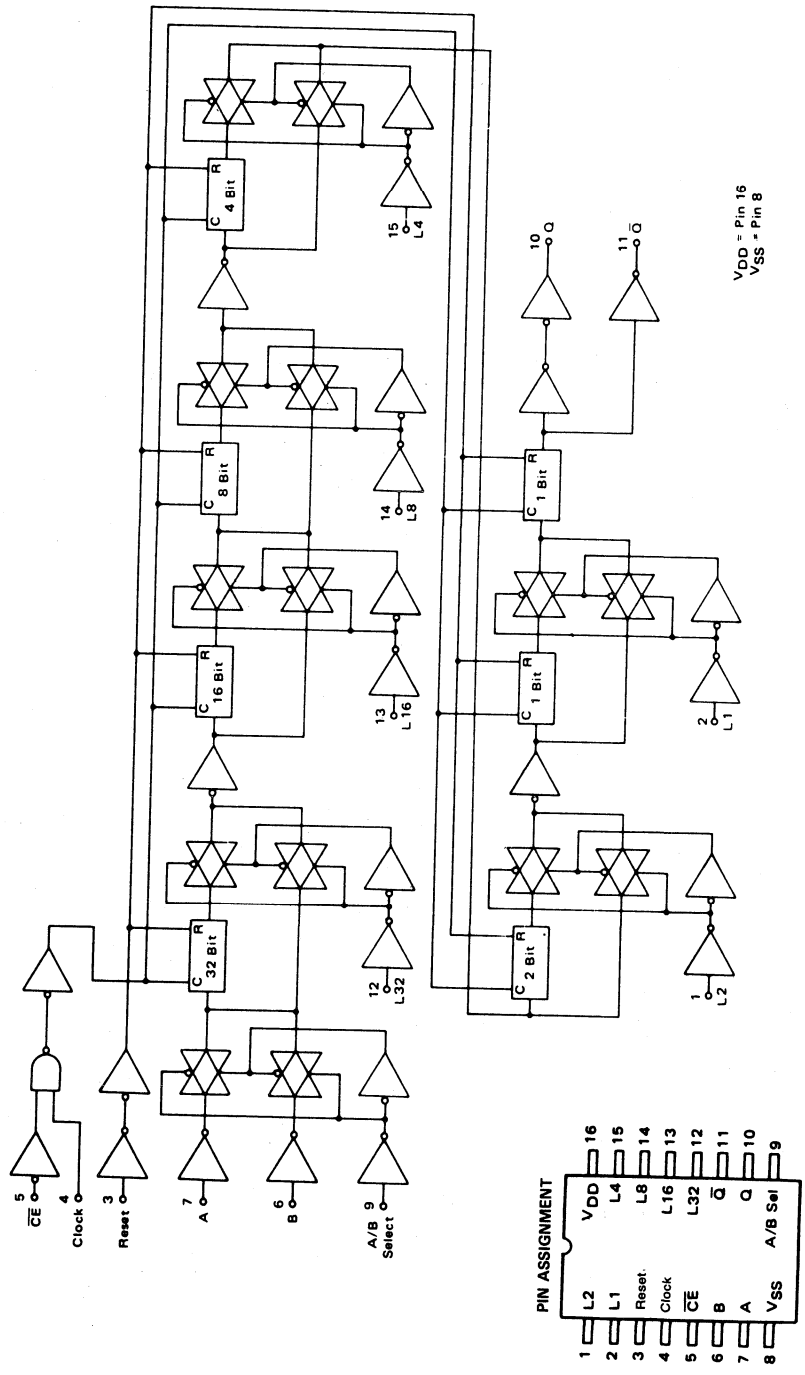
*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TIMING DIAGRAM



6

LOGIC DIAGRAM



PIN ASSIGNMENT

6

MOTOROLA

MC14560B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER

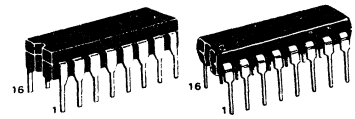
NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE*

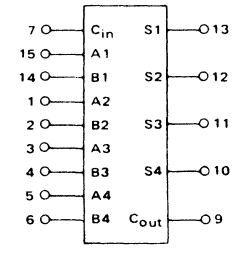
INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.68 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.35 μA/kHz) f + I_{DD}							
		15	I_T = (5.03 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

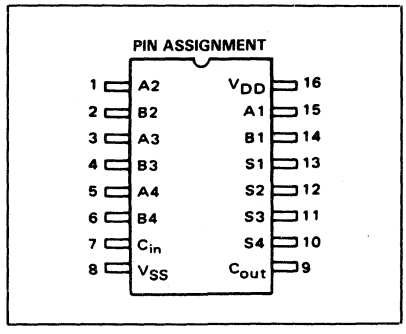
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.



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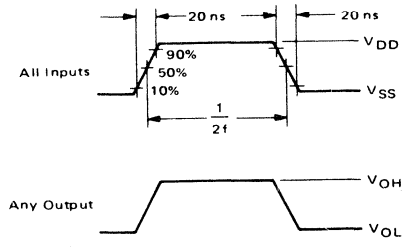
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A or B to S	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	675	
A or B to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
C_{in} to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	450	
Turn-Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	–	800	2250	
t_{PLH} = (0.66 ns/pF) C_L + 197 ns		10	–	350	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	–	240	750	
Turn-On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	

*The formulas given are for the typical characteristics only at 25°C.

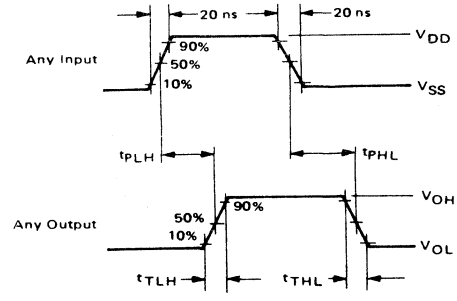
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION WAVEFORMS



Duty Cycle = 50%
All outputs connected to respective C_L loads
f = System clock frequency

FIGURE 2 – SWITCHING TIME WAVEFORMS



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FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

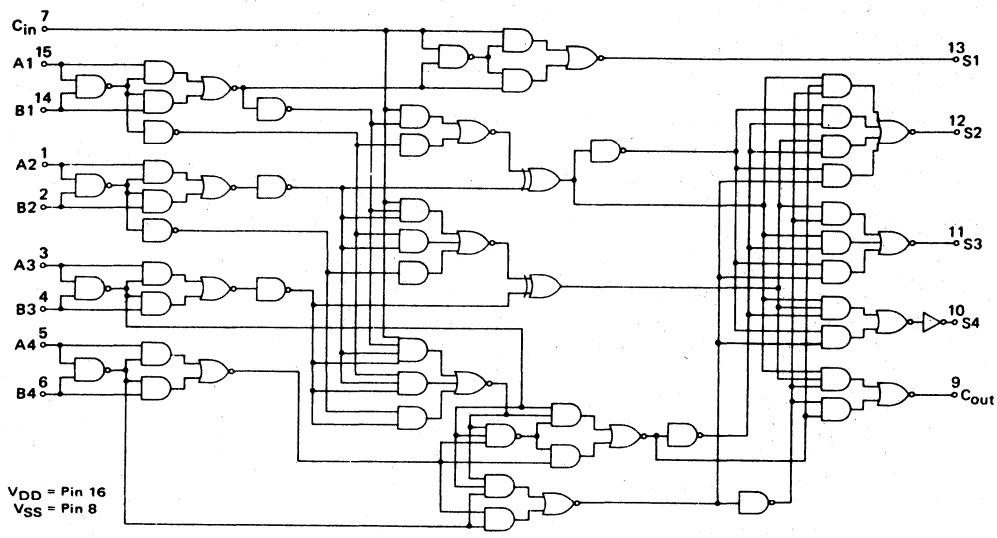
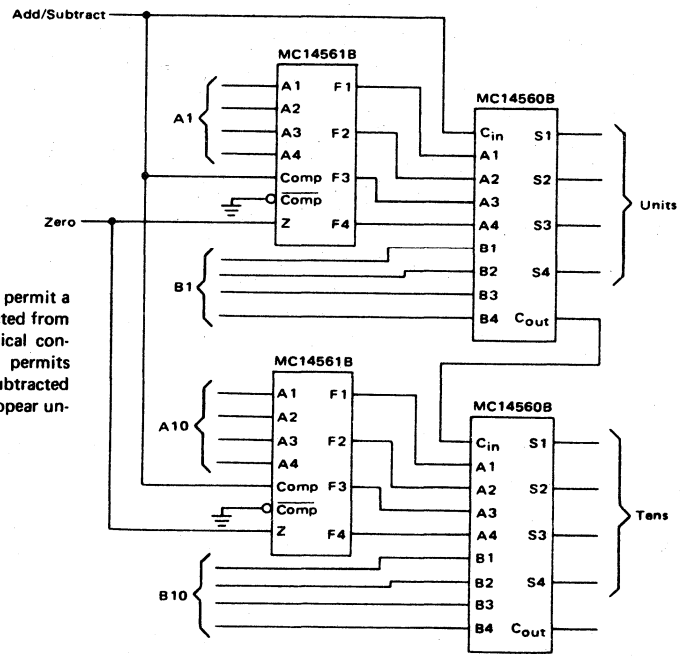


FIGURE 3 – PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

APPLICATIONS INFORMATION

INTRODUCTION

Frequently in small digital systems, simple decimal arithmetic is performed. Decimal data enters and leaves the system arithmetic unit in a binary coded decimal (BCD) format. The adder/subtracter in the airthmetic unit may be required to accept sign as well as magnitude, and generate sign, magnitude, and overflow. In the past, it has been cumbersome to build sign and magnitude adder/subtracters. Now, using Motorola's MSI CMOS functions, the MC14560 NBCD Adders and MC14561 9's Complementers, NBCD adder/subtracters may be built economically, with surprisingly low package count and moderate speed.

Some background information on BCD arithmetic is presented here, followed by simple circuits for unsigned adder/subtracters. The final circuit discussed is an adder/subtracter for signed numbers with complete overflow and sign correction logic.

DECIMAL NUMBER REPRESENTATION

Because logic elements are binary or two-state devices, decimal digits are generally represented as a group of bits in a weighted format. There are many possible binary codes which can be used to represent a decimal number. One of the most popular codes using 4 binary digits to represent 0 thu 9 is Natural Binary Coded Decimal (NBCD or 8-4-2-1 code).

NBCD is a weighted code. If a value of "0" or "1" is assigned to each of the bit positions, where the rightmost position is 2^0 and the leftmost is 2^3, and the values are summed for a given code, the result is equal to the decimal digit represented by the code. Thus, 0110 equals $0{\cdot}2^3 + 1{\cdot}2^2 + 1{\cdot}2^1 + 0{\cdot}2^0 = 4 + 2 = 6$. The 1010, 1011, 1100, 1101, 1110, and 1111 binary codes are not used. Because of these illegal states, the addition and subtraction of NBCD numbers is more complex than similar calculations on straight binary numbers.

ADDITION OF UNSIGNED NBCD NUMBERS

When 2 NBCD digits, A and B, and a possible carry, C, are added, a total of 20 digit sums (A + B + C) are possible as shown in Table 1.

The binary representations for the digit sums 10 thru 19 are offset by 6, the number of unused binary states, and are not correct. An algorithm for obtaining the correct sum is shown in Figure 1. A conventional method of implementing the BCD addition algorithm is shown in Figure 2(a). The NBCD digits, A and B, are summed by a 4 bit binary full adder. The resultant (sum and carry) is input to a binary/BCD code converter which generates the correct BCD code and carry.

An NBCD adder block which performs the above function is available in a single CMOS package (MC14560). Figure 2(b) shows n decades cascaded for addition of n digit unsigned NBCD numbers. Add time is typically 0.1 + 0.2n μs for n decades. When the carry out of the most significant decade is a logical "1", an overflow is indicated.

COMPLEMENT ARITHMETIC

Complement arithmetic is used in NBCD subtraction. That is, the "complement" of the subtrahend is added to the minuend. The complementing process amounts to biasing the subtrahend such that all possible sums are positive. Consider the subtraction of the NBCD numbers, A and B:

$$R = A - B$$

where R is the result. Now bias both sides of the equation by $10^N - 1$ where N is the number of digits in A and B.

$$R + 10^N - 1 = A - B + 10^N - 1$$

Rearranging,

$$R + 10^N - 1 = A + (10^N - 1 - B)$$

The term $(10^N - 1 - B)$, $-B$ biased by $10^N - 1$, is known as the 9's complement of B. When A>B, $R + 10^N - 1 > 10^N - 1$; thus R is a positive number. To obtain R, 1 is added to $R + 10^N - 1$, and the carry term, 10^N, is dropped. The addition of 1 is called End Around Carry (EAC).

When $A < B$, $R + 10^N - 1 < 10^N - 1$, no EAC results and R is a negative number biased by $10^N - 1$; thus $R + 10^N - 1$ is the 9's complement of R.

SUBTRACTION OF UNSIGNED NBCD NUMBERS

Nine's complement arithmetic requires an element to perform the complementing function. An NBCD 9's complementer may be implemented using a 4 bit binary adder and 4 inverters, or with combinatorial logic. The Motorola MC14561 9's complementer is available in a single package. It has true and inverted complement disable, which allow straight-through or complement modes of operation. A "zero" line forces the output to "0". Figure 3 shows an NBCD subtracter block using the MC14560 and MC14561. Also shown are n cascaded blocks for subtraction of n digit unsigned numbers. Subtract time is 0.6 + 0.4n μs for n stages. Underflow (borrow) is indicated by a logical "0" on the carry output of the most significant digit. A "0" carry also indicates that the difference is a negative number in 9's complement form. If the result is input to a 9's complementer, as shown, and its mode controlled by the carry out of the most significant digit, the output of the complementer will be the correct negative magnitude. Note that the carry out of the most significant digit (MSD) is the input to carry in of the least significant digit (LSD). This End Around Carry is required because subtraction is done in 9's complement arithmetic.

By controlling the complement and overflow logic with an add/subtract line, both addition and subtraction are performed using the basic subtracter blocks (Figure 4).

TABLE 1 — Sum = A + B + C

Binary Sums		Decimal Number	Corrected Binary Sums
0000		0	0000
0001		1	0001
0010		2	0010
0011		3	0011
0100		4	0100
0101		5	0101
0110		6	0110
0111		7	0111
1000		8	1000
1001		9	1001
1010	Non valid BCD representation	10	0000 + Carry
1011		11	0001 + Carry
1100		12	0010 + Carry
1101		13	0011 + Carry
1110		14	0100 + Carry
1111		15	0101 + Carry
0000 + Carry		16	0110 + Carry
0001 + Carry		17	0111 + Carry
0010 + Carry		18	1000 + Carry
0011 + Carry		19	1001 + Carry

ADDITION AND SUBTRACTION OF SIGNED NBCD NUMBERS

Using MC14560 NBCD Adders and MC14561 9's Complementers, a sign and magnitude adder/subtracter can be configured (Figure 5). Inputs A and B are signed positive (A_S, B_S = "0") or negative (A_S, B_S = "1"). B is added to or subtracted from A under control of an Add/Sub line (subtraction = "1"). The result, R, of the operation is positive signed, positive signed with overflow, negative signed, or negative signed with overflow. Add/subtract time is typically 0.6 + 0.4n μs for n decades.

An exclusive-OR of Add/Sub line and B_S produces B', which controls the B complementers. If B_S, the sign of B, is a logical "1" (B is negative) and the Add/Sub line is a "0" (add B to A), then the output of the exclusive-OR (B_S') is a logical "1" and B is complemented. If B_S = "1" and Add/Sub = "1", B is not complemented since subtracting a negative number is the same as adding a positive number. When Add/Sub is a "1" and B_S = "0", B_S' is a "1" and B is complemented. The A complementer is controlled by the A sign bit, A_S. When A_S = "1", A is complemented.

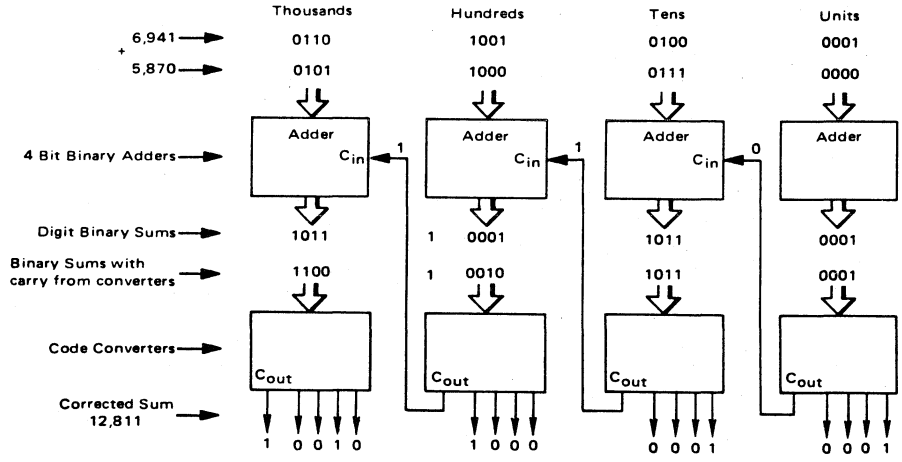
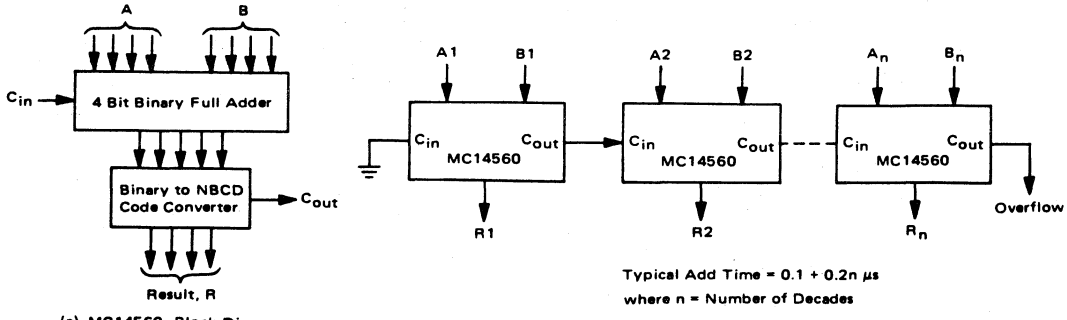


FIGURE 4 — Unsigned NBCD Addition Algorithm



(a) MC14560 Block Diagram

(b) n-Decade Adder

FIGURE 5 — Addition of Unsigned NBCD Numbers

The truth table and Karnaugh maps for sign, overflow, and End Around Carry are shown in Figures 6 and 7. Note the use of B_S' from the exclusive-OR of Add/Sub and B_S. B_S' eliminates Add/Sub as a variable in the truth table. As an example of truth table generation, consider an n decade adder/subtracter where A_S = "0", B_S = "1", and Add/Sub = "0". B is in 9's complement form, $10^N - 1 - B$. Thus $A + (10^N - 1 - B) = 10^N - 1 + (A - B)$. There is no carry when $A \leq B$, and the sign is negative (sign = "1"). When A_S and B_S are opposite states and Add/Sub is a "0" (add mode), no overflow can occur (overflow = "0"). The other output states are determined in a similar manner (see Figure 6).

From the Karnaugh maps it is apparent that End Around Carry is composed of the two symmetrical functions S2 and S3 of three variables with A_S B_S' C_{out} as the center of symmetry. This is the definition of the majority logic function $M_3(ABC)$. Similarly the Sign is composed of the symmetrical functions S2(3) and S3(3) but with the center of symmetry translated to A_SB_S' C_{out}. This is equivalent to the majority function $M_3(A_SB_S'\ \overline{C}_{out})$. Further evaluation of the maps and truth table reveal that Overflow can be generated by the exclusive-OR function of End Around Carry and Carry Out. This analysis results in a minimum device count consisting of one exclusive-OR package and one dual Majority Logic package to implement B_S', EAC, Sign and Overflow. The logic connections of these devices are shown in Figure 5.

The output sign, R_S, complements the result of the add/subtract operation when R_S = "1". This is required because the adder performs 9's complement arithmetic. Complementing, when R_S indicates the result is negative, restores sign and magnitude convention.

Several variations of the adder/subtracter are possible. For example, 9's complement is available at the output of the NBCD adders, and output complementers are eliminated if sign and magnitude output is not required.

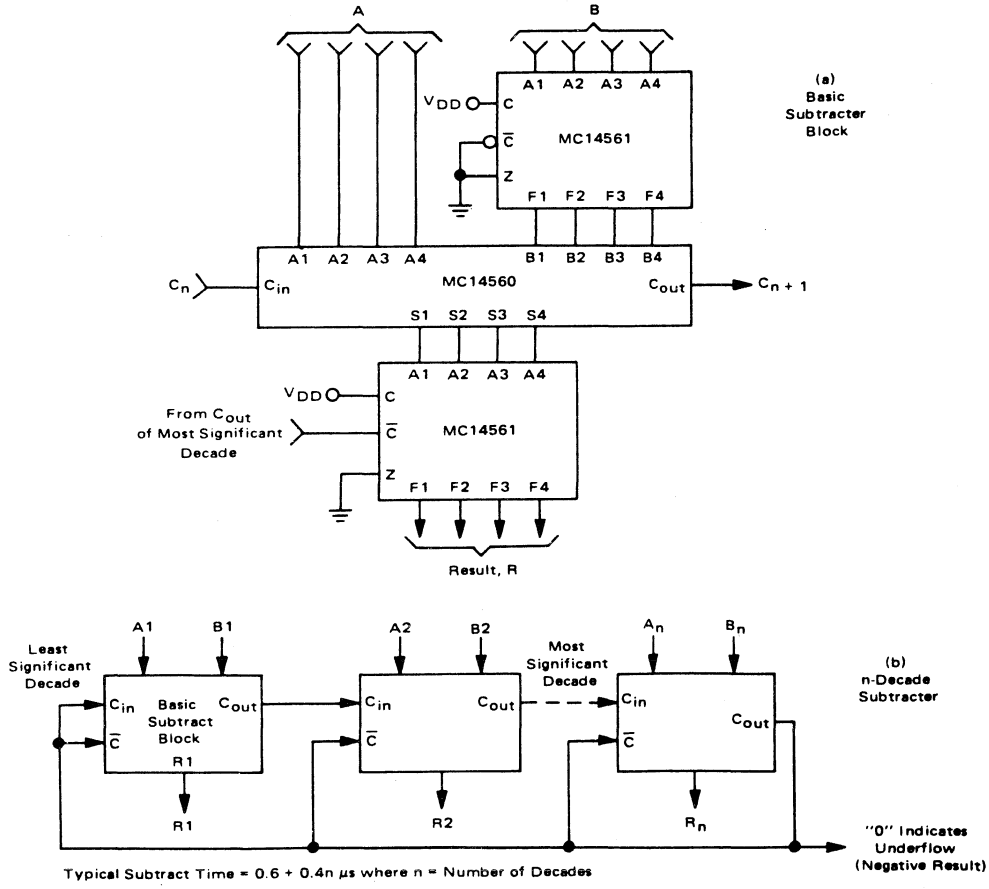


FIGURE 6 — Subtraction of Unsigned NBCD Numbers

SUMMARY

The concepts of binary code representations for decimal numbers, addition, and complement subtraction were discussed in detail. Using the basic Adder and Complementer MSI blocks, adder/subtracters for both signed and unsigned numbers were illustrated with examples.

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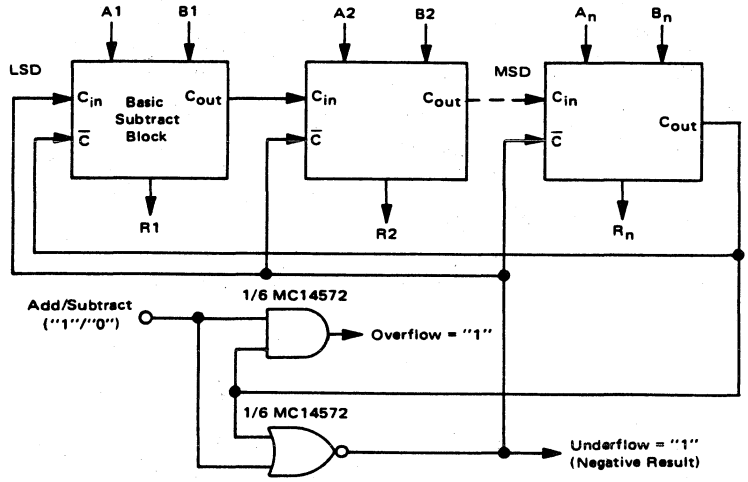


FIGURE 7 — Adder/Subtracter for Unsigned NBCD Numbers

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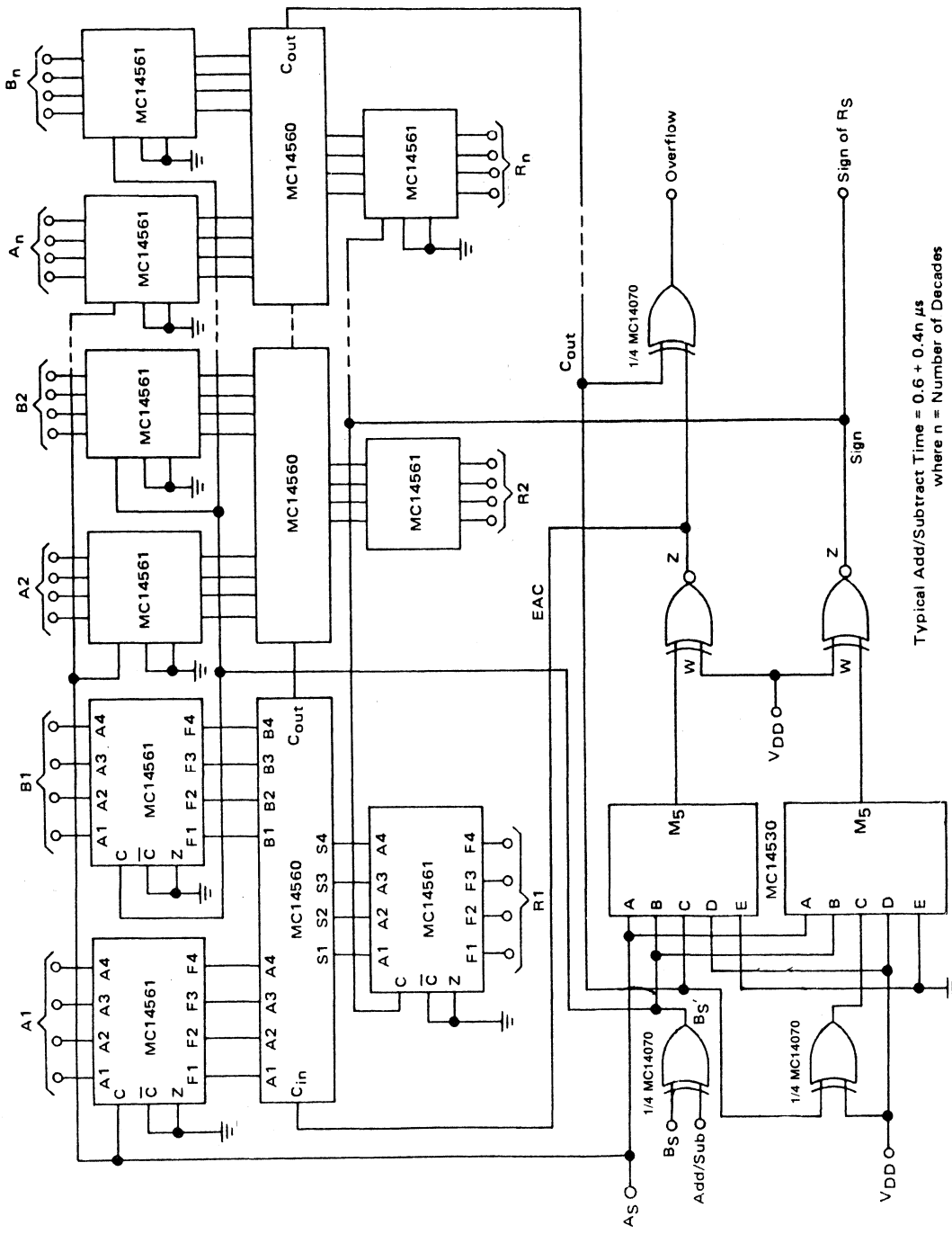


FIGURE 8 — SIGN AND MAGNITUDE ADDER/SUBTRACTER WITH OVERFLOW

INPUTS			Arithmetic Expression for R* (Result) (N = Number of Digits, 10^N = Modulus A, B, R are Positive Magnitudes)	OUTPUTS		
A_S "1" = Neg	B_S' "1" = Neg	C_{out} "1" = Carry		End Around Carry (EAC) "1" = EAC	Sign of R "1" = Negative	Overflow "1" = Overflow
0	0	0	R = A + B	No EAC ("0") because R is correct result.	Since A and B are positive signed, R is positive signed ("0").	When C_{out} = "0", there is no carry ($R < 10^N$) and thus no overflow ("0").
0	0	1				When C_{out} = "1", there is a carry ($R \geq 10^N$) and thus overflow ("1")
0	1	0	R = A - B = A + (10^N - 1 - B) = A - B + 10^N - 1	No EAC ("0") because 9's complement expression for R is correct result.	A ≤ B when C_{out} = "0"; thus sign of R must be negative ("1").	There is never an overflow when numbers of opposite sign are added.
0	1	1		EAC = "1" because expression for R is in error by 1.	A > B when C_{out} = "1"; thus sign of R must be positive ("0").	
1	0	0	R = B - A = B + (10^N - 1 - A) = B - A + 10^N - 1	No EAC ("0") because 9's complement expression for R is correct result.	B ≤ A when C_{out} = "0"; thus sign of R must be negative ("1").	
1	0	1		EAC = "1" because expression for R is in error by 1.	B > A when C_{out} = "1"; thus sign of R must be positive ("0").	
1	1	0	R = - A - B = (10^N - 1 - A) + (10^N - 1 - B) = - (A + B) + 2 × 10^N - 2	EAC = "1" because 9's complement expression for R is in error by 1.	Since A and B are negative signed, R is negative signed ("1").	When C_{out} = "0", there is no carry ($R < 10^N$) and (A + B) ≥ 10^N - 1 indicating overflow ("1").
1	1	1				When C_{out} = "1", there is a carry ($R \geq 10^N$) and (A + B) ≤ 10^N - 1 indicating no overflow ("0").

*Output of Adders

FIGURE 9 — Truth Table Generation for EAC, Sign, and Overflow Logic

TRUTH TABLE

INPUTS			OUTPUTS		
A_S	B_S'	C_{out}	EAC	SGN	OVF
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	0	1	0
1	1	0	1	1	1
0	0	1	0	0	1
0	1	1	1	0	0
1	0	1	1	0	0
1	1	1	1	1	0

B_S' = (Add/Sub)⊕B_S
A_S = Sign of A ("1" = Negative)
B_S = Sign of B ("1" = Negative)
C_{out} = Adder Carry Out

KARNAUGH MAPS

End Around Carry

C_{out} \ A_S	0	1
1	0	1
0	1	1
1	0	1
0*	0	1

B_S'

Sign (SGN)

C_{out} \ A_S	1	0
1	1	1
0	1	1
0*	0	0
0	1	1

B_S'

Overflow (OVF)

C_{out} \ A_S	0	1
1	0	1
0	0	0
1	0	0
0	0	0

B_S'

* = Center of Symmetry

$$EAC = S2\,(A_S B_S'\, C_{out}) + S3\,(A_S B_S'\, C_{out})$$
$$= M_3\,(A_S B_S'\, C_{out})$$

$$SGN = S2\,(A_S B_S'\, \overline{C}_{out}) + S3\,(A_S B_S'\, \overline{C}_{out})$$
$$= M_3\,(A_S B_S'\, C_{out})$$

EAC		C_{out}		OVF
0	1	0	0	0 1
1	1	1	1	0 0
0	1	1	1	1 0
0	0	0	0	0 0

⊕ ⊕ =

FIGURE 10 — Mapping of EAC, Sign and Overflow Logic

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MOTOROLA

MC14561B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

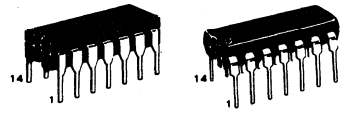
9's COMPLEMENTER

9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable ($\overline{Comp}$) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

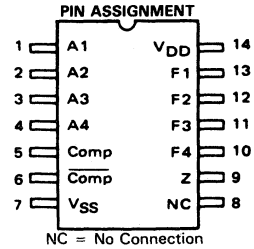
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

PIN ASSIGNMENT



NC = No Connection

TRUTH TABLE

Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\overline{A1}$	A2	$A2\overline{A3} + \overline{A2}A3$	$\overline{A2}\overline{A3}\overline{A4}$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.0 µA/kHz) f + I_{DD}							
		15	I_T = (4.5 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

6

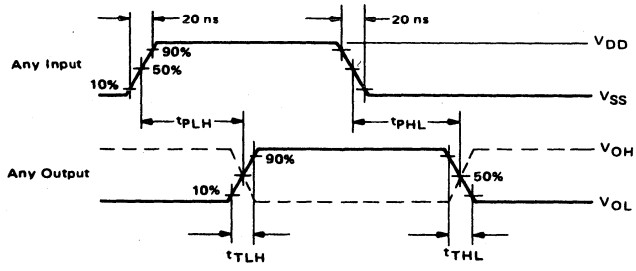
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	300	

*The formulas given are for the typical characteristics only at 25°C.

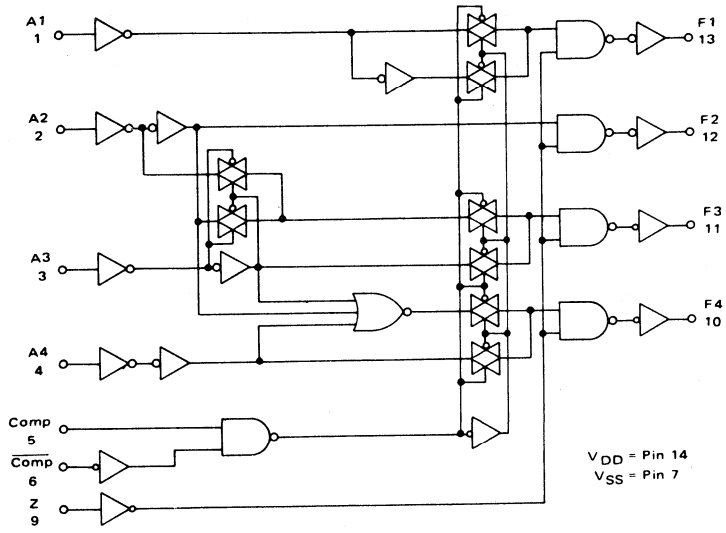
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME WAVEFORMS



6

LOGIC DIAGRAM



TRUTH TABLE – COMPLEMENT MODE

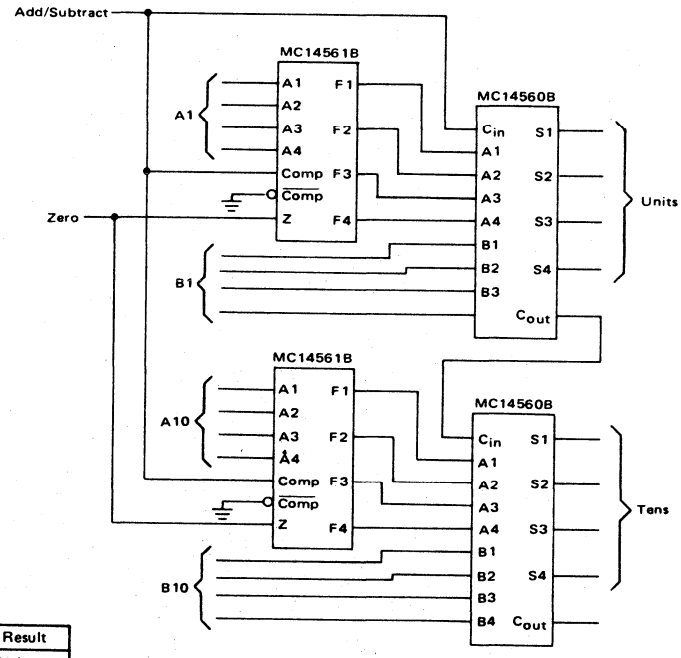
(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

	Decimal Equivalent Input	Inputs A4	A3	A2	A1	Decimal Equivalent Output	Outputs F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1	1
	7	0	1	1	1	2	0	0	1	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
Illegal BCD Input Codes	10	1	0	1	0	7	0	1	1	1
	11	1	0	1	1	6	0	1	1	0
	12	1	1	0	0	5	0	1	0	1
	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 – PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)

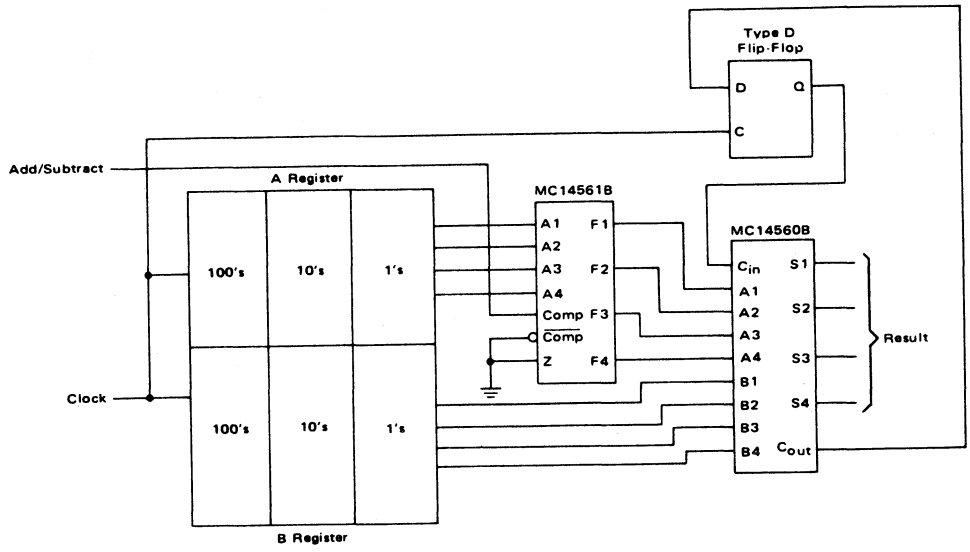


TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



MOTOROLA

MC14562B

128-BIT STATIC SHIFT REGISTER

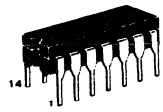
The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Fully Static Operation
- Cascadable to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

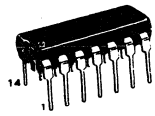
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

128-BIT STATIC SHIFT REGISTER.



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

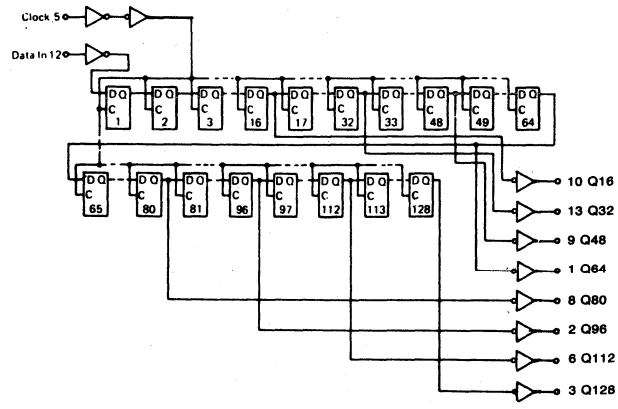
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

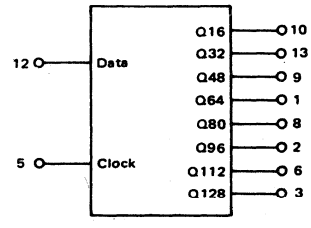
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.94 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.81 µA/kHz) f + I_{DD}							
		15	I_T = (5.52 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

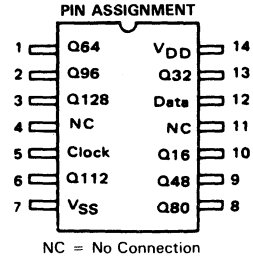
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

PIN ASSIGNMENT



NC = No Connection

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

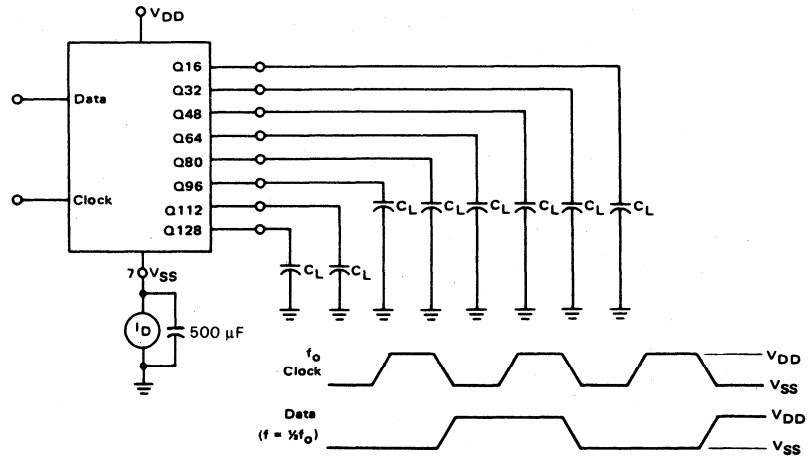
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 515 ns		5.0	–	600	1200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
(50% Duty Cycle)		10	220	110	–	
		15	150	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	1.9	1.1	MHz
		10	–	5.6	3.0	
		15	–	8.0	4.0	
Data to Clock Setup Time	$t_{su(1)}$	5.0	-20	-170	–	ns
		10	-10	-64	–	
		15	0	-60	–	
	$t_{su(0)}$	5.0	-20	-91	–	ns
		10	-10	-58	–	
		15	0	-48	–	
Data to Clock Hold Time	$t_{h(1)}$	5.0	350	263	–	ns
		10	165	109	–	
		15	155	100	–	
	$t_{h(0)}$	5.0	350	267	–	ns
		10	200	140	–	
		15	140	93	–	
Clock Input Rise and Fall Times	t_r, t_f	5.0	—	—	15	μs
		10	—	—	5	
		15	—	—	4	

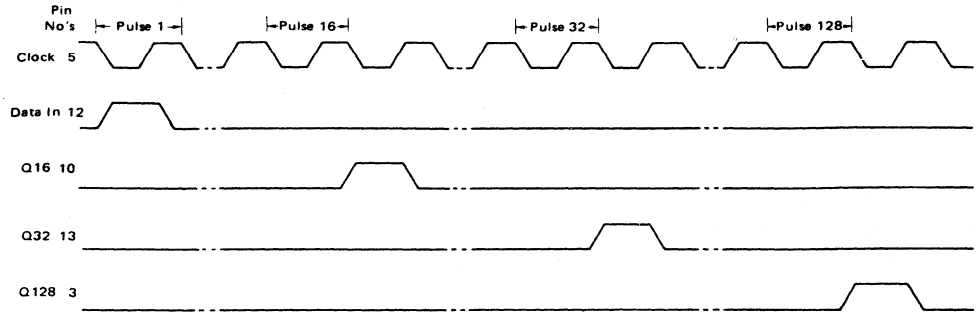
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

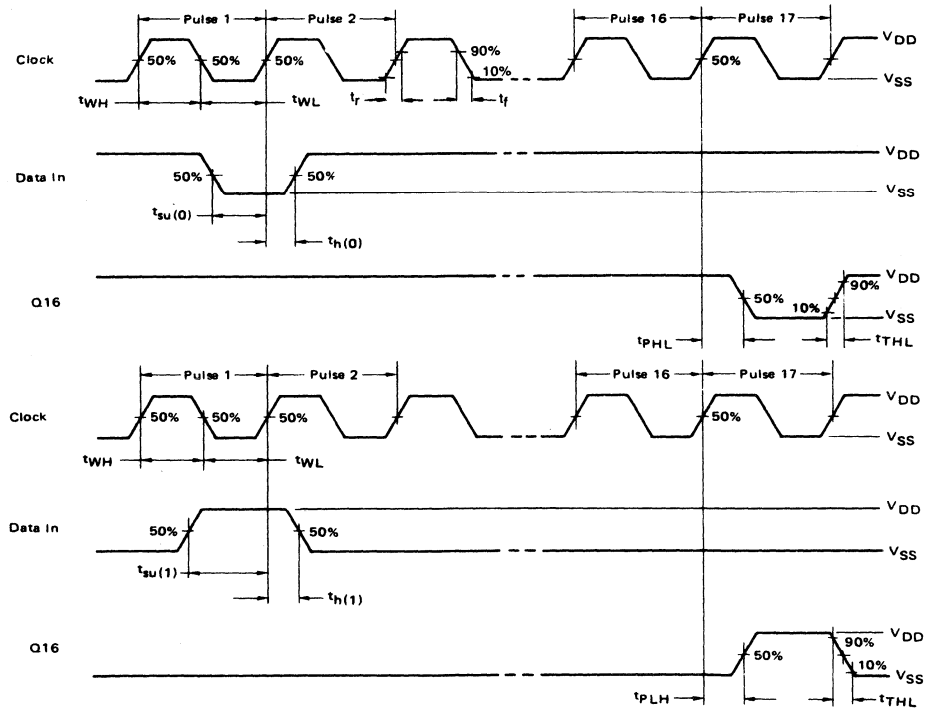
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

6

MOTOROLA

MC14566B

INDUSTRIAL TIME BASE GENERATOR

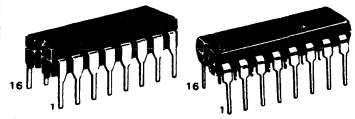
The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line. Pin 11 = V_{DD} will cause ÷5.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL
TIME BASE GENERATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

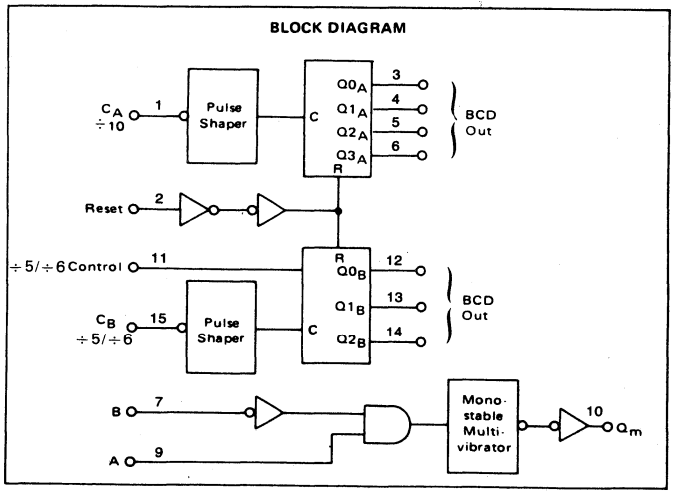
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

ORDERING INFORMATION

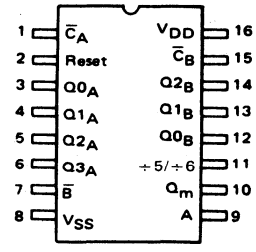
A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.0 μA/kHz) f + I_{DD}							
		15	I_T = (3.0 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time, Clock to $Q3_A$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1365 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 497 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 295 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	1450 530 320	4500 1500 1000	ns
Propagation Delay Time, Reset to $Q3_A$ t_{PHL} = (1.7 ns/pF) C_L + 845 ns t_{PHL} = (0.66 ns/pF) C_L + 282 ns t_{PHL} = (0.5 ns/pF) C_L + 185 ns	t_{PHL}	5.0 10 15	– – –	930 315 210	3000 1000 750	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0 10 15	1200 400 270	400 125 90	– – –	ns
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	1200 400 270	400 125 90	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	1.0 2.5 4.2	0.3 1.0 1.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			–
Monostable Multivibrator Pulse Width	$t_{WH(Q_m)}$	5.0 10 15	1200 400 300	2800 900 600	– – –	ns

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

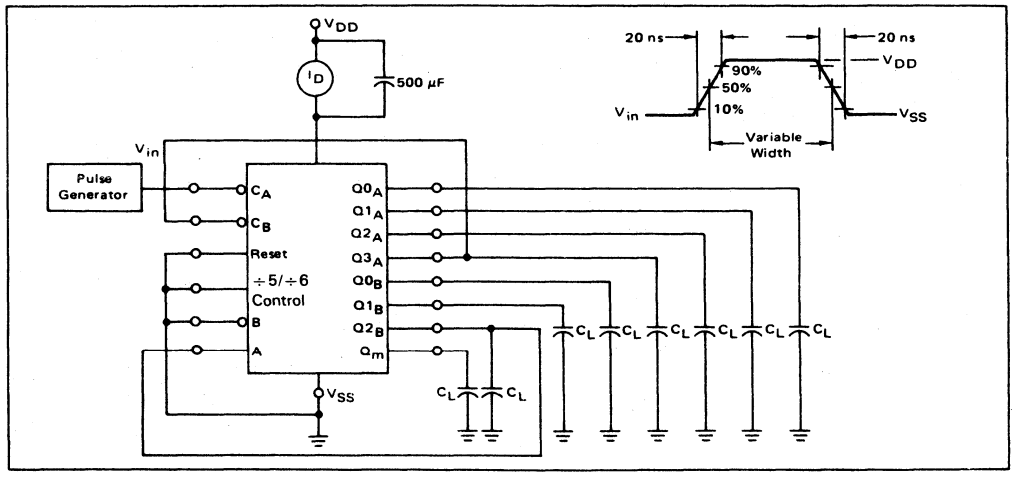
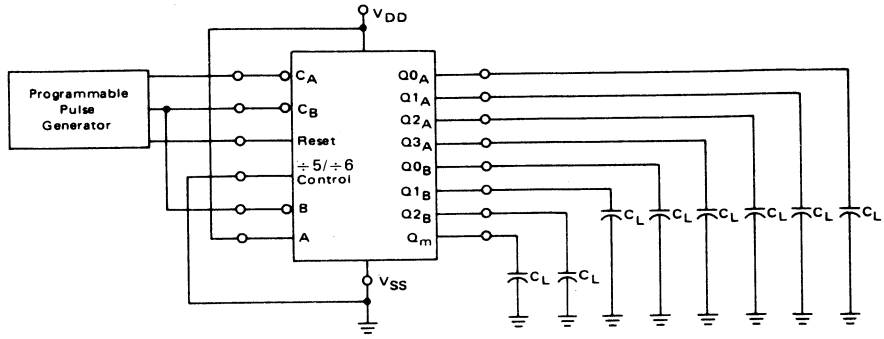
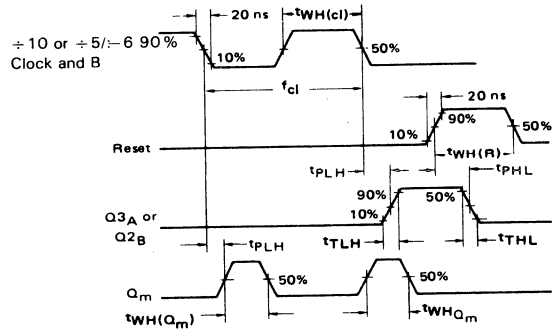


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



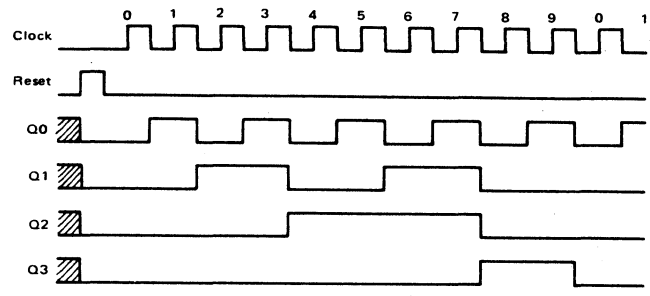
Note: Assume ÷ 10 Counter at "6" and ÷5/÷6 Counter at "2" at beginning of sequence.



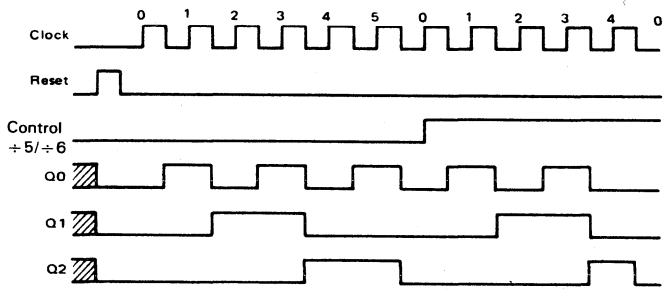
6

TIMING DIAGRAM

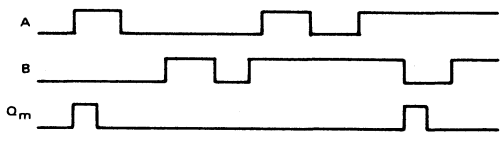
Divide-By-10 Counter



Divide-By-5/Divide-By-6



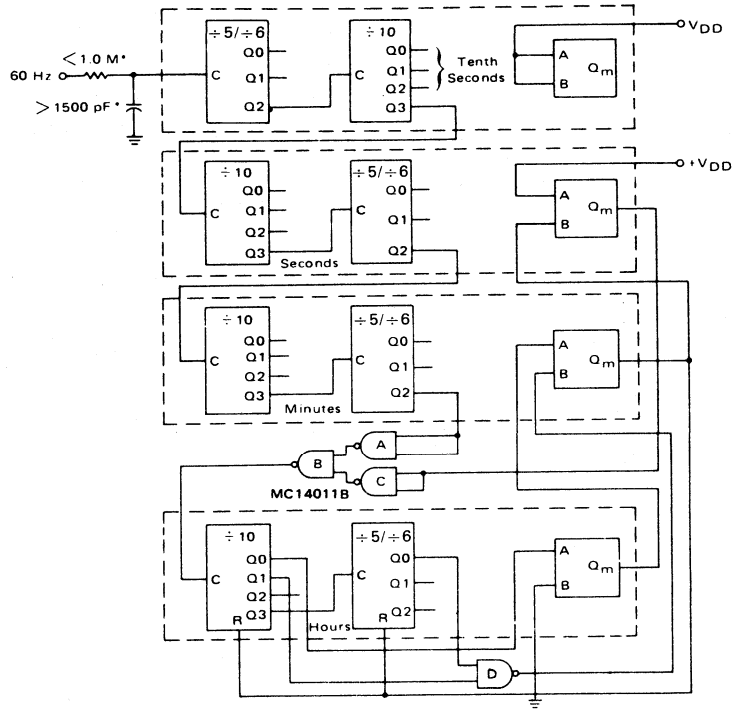
Monostable Multivibrator



▨ = Don't Care

6

APPLICATION – 12 HOUR CLOCK



÷5/÷6 Control not shown = V_{SS}

Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

6

MOTOROLA

MC14569B

PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BINARY/BCD DOWN COUNTER

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

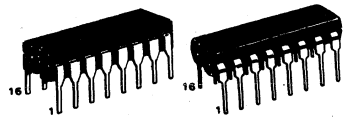
This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BINARY/BCD DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

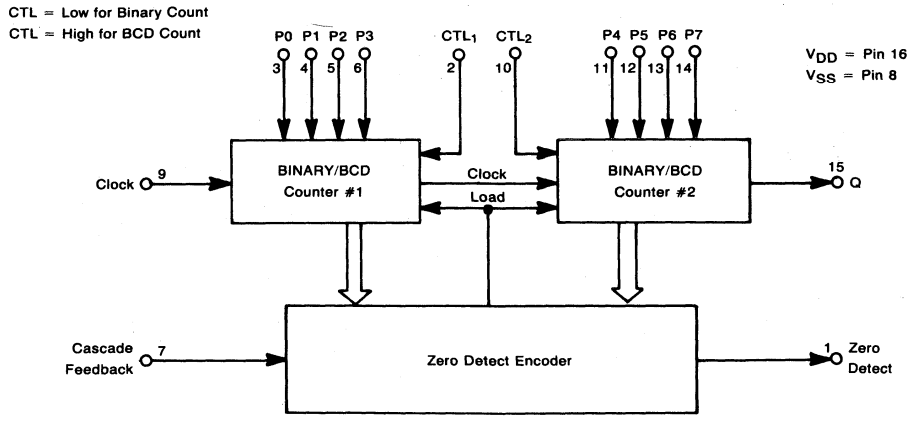
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

BLOCK DIAGRAM



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.005	50	–	150	μAdc
		10	–	100	–	0.010	100	–	300	
		15	–	200	–	0.015	200	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	(0.58 μA/kHz) f + I_{DD}							μAdc
		10	(1.20 μA/kHz) f + I_{DD}							
		15	(1.95 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn-On Delay Time	t_{PLH}					ns
Zero Detect Output		5.0	–	420	700	
		10	–	175	300	
		15	–	125	250	
Q Output		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn-Off Delay Time	t_{PHL}					ns
Zero Detect Output		5.0	–	380	600	
		10	–	150	300	
		15	–	100	200	
Q Output		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	–	ns
		10	150	45	–	
		15	115	30	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.7	
		15	–	13.0	7.8	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	NO LIMIT			µs
		10				
		15				

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

FIGURE 1

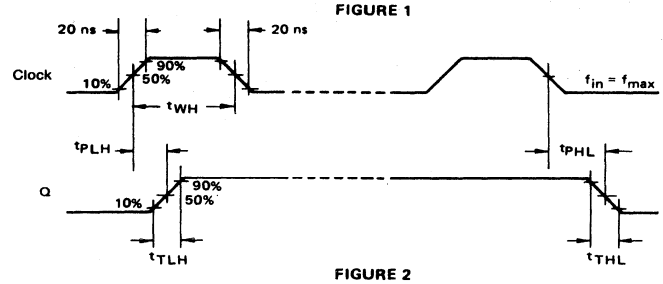
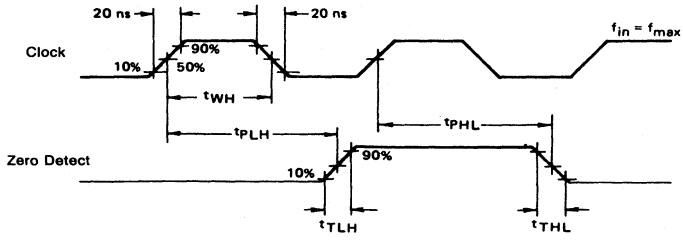


FIGURE 2



6

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL_1 (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL_2 (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

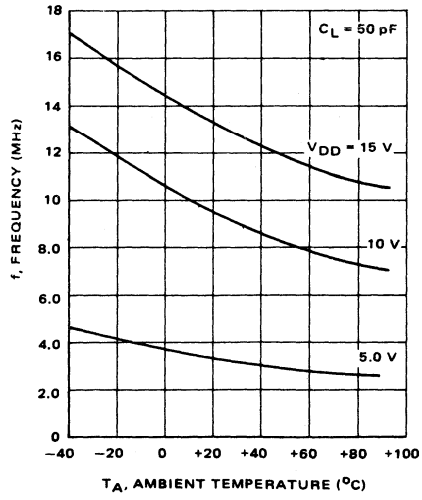
V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

OPERATING CHARACTERISTICS

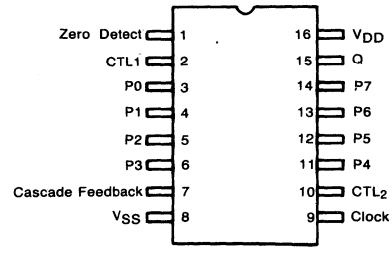
The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL_1 and CTL_2.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.



PIN ASSIGNMENT



6

TABLE 1 — MODE CONTROLS (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL_1	CTL_2	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

Note: Data Preset Inputs (P0-P7) are "Don't Cares" while Cascade Feedback is Low.

TABLE 2 — MODE CONTROLS (CTL_1 = Low, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	1	0	0	0	136	136	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	1	1	1	255	255	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)

6

TABLE 3 — MODE CONTROLS (CTL_1 = High, CTL_2 = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	0	0	1	19	X	
0	0	1	0	0	0	0	0	20	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	0	0	0	0	0	60	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	0	0	0	0	150	150	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	0	0	1	159	159	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 Binary				Counter #1 BCD						Counting Sequence

X = No Output (Always Low)

6

TABLE 4 — MODE CONTROLS (CTL_1 = Low, CTL_2 = High, Cascade Feedback = High)

Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	48	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	0	0	0	0	0	64	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	0	1	0	0	0	0	80	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
0	1	1	1	0	0	0	0	112	X	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	144	144	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	1	1	1	159	159	
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0			
128	64	32	16	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

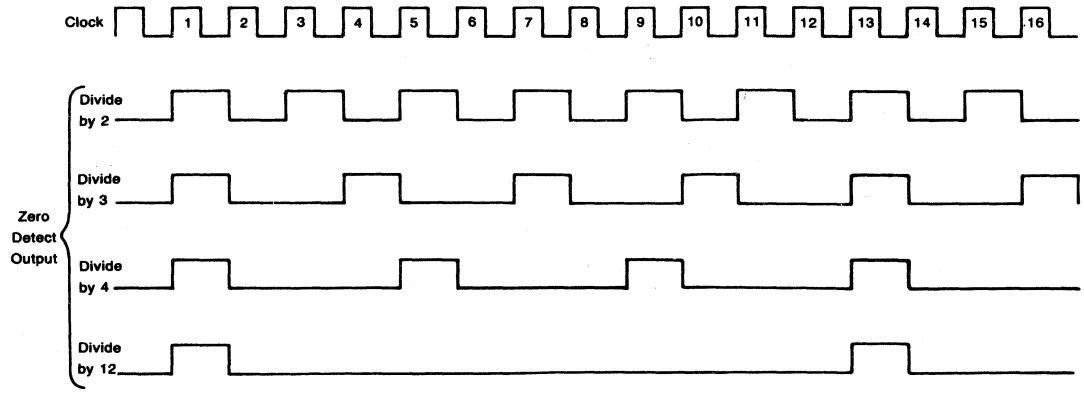
X = No Output (Always Low)

TABLE 5 — MODE CONTROLS (CTL_1 = High, CTL_2 = High, Cascade Feedback = High)

Preset Values								Divide Ratio		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	X	X	Illegal State
0	0	0	0	0	0	1	0	2	X	Min Count
0	0	0	0	0	0	1	1	3	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	1	0	0	0	0	50	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	↓
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	1	0	0	1	99	99	
80	40	20	10	8	4	2	1			Bit Value
Counter #2 BCD				Counter #1 BCD						Counting Sequence

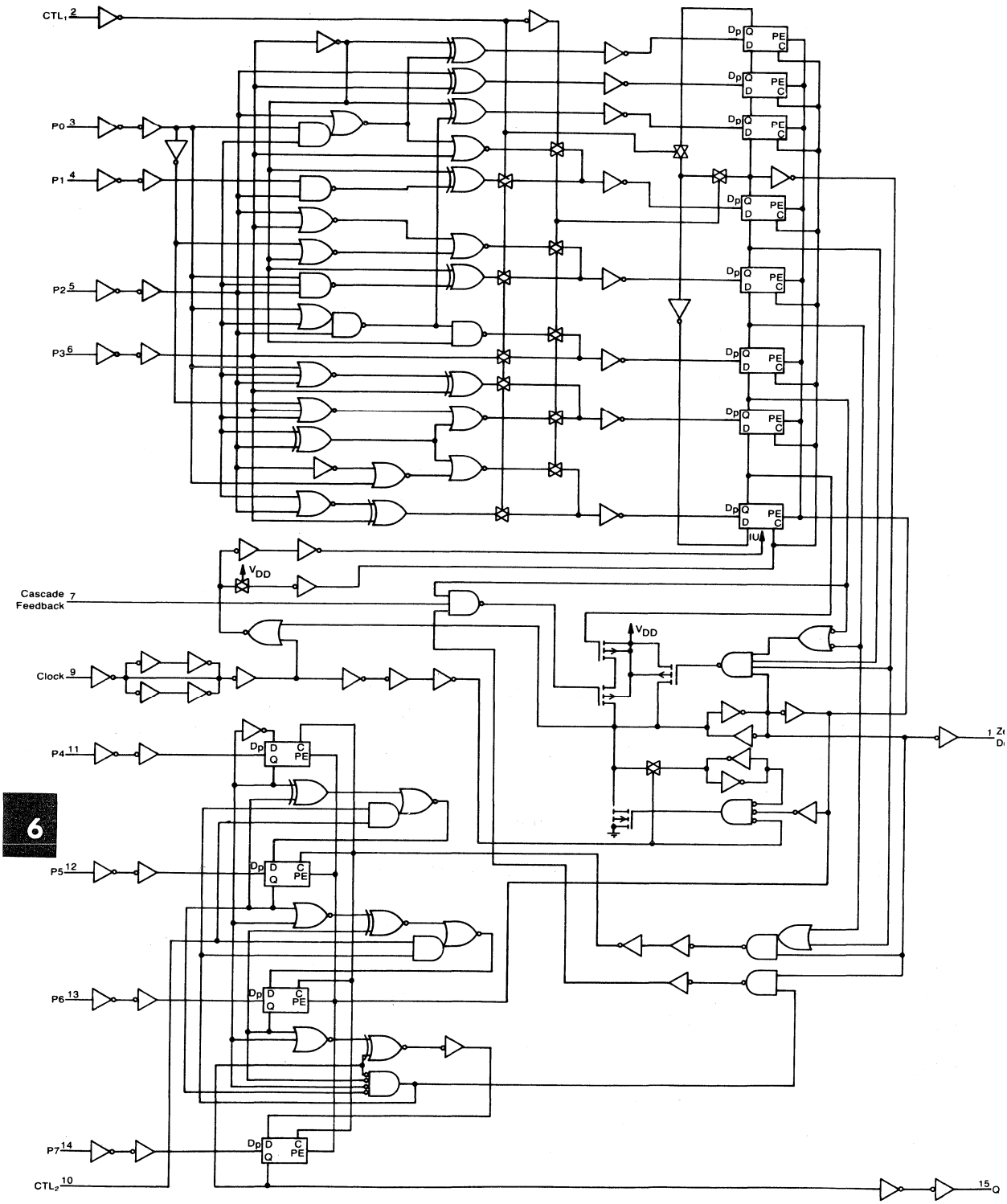
X = No Output (Always Low)

TIMING DIAGRAM MC14569B



MC14569B

LOGIC DIAGRAM



6

TYPICAL APPLICATIONS

FIGURE 6 — CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

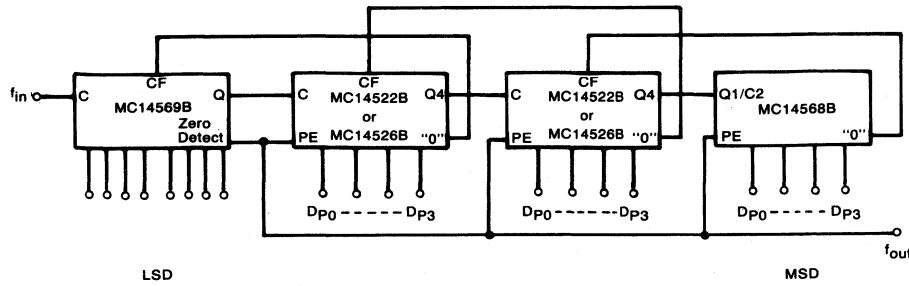
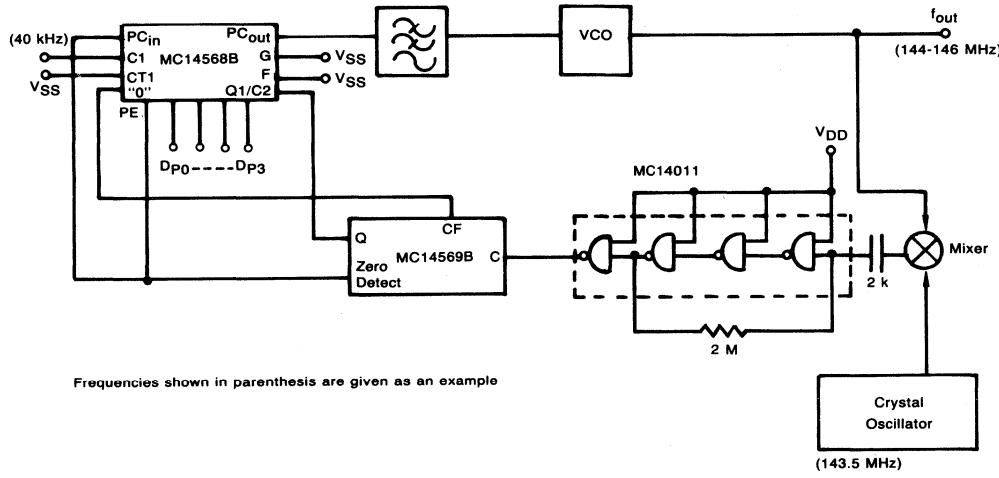


FIGURE 7 — FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example

6

MOTOROLA

MC14572UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

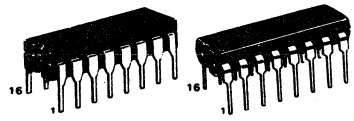
HEX GATE

4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE

HEX GATE

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

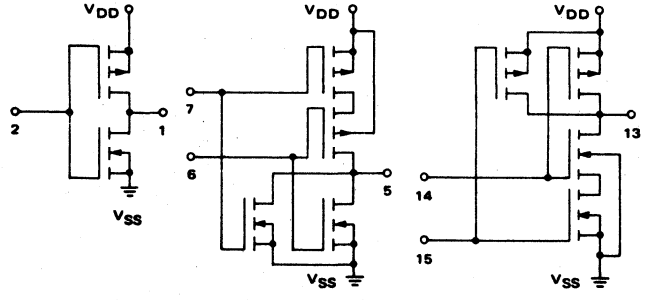
C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

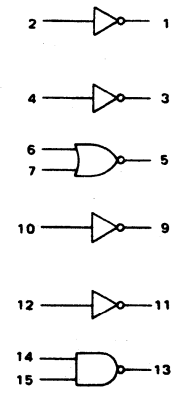
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.89 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.80 µA/kHz) f + I_{DD}							
		15	I_T = (5.68 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

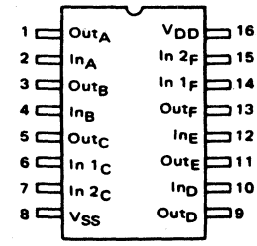
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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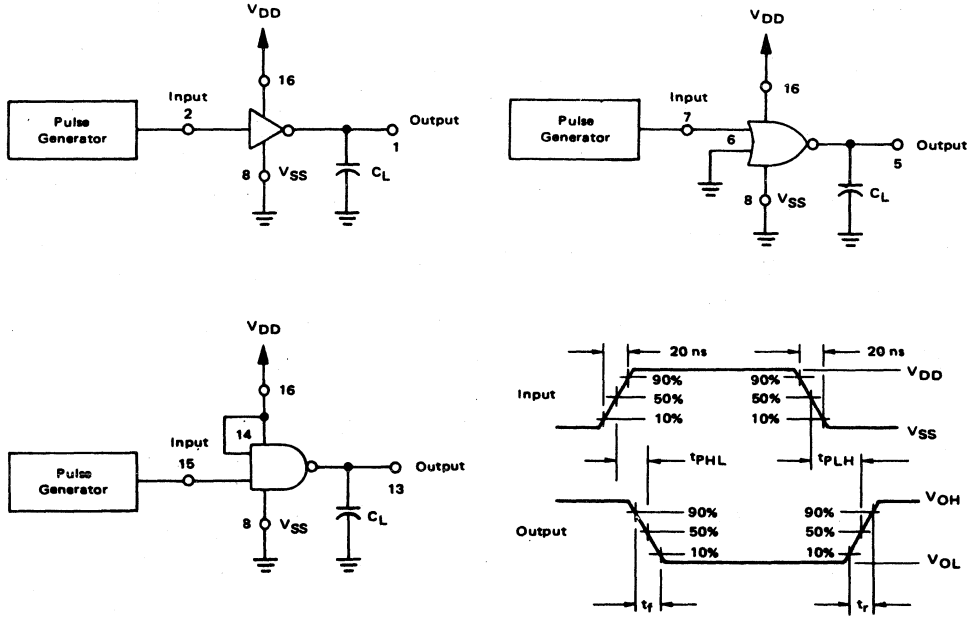
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 5 ns		5.0	–	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 17 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



MOTOROLA

MC14580B

4 x 4 MULTIPORT REGISTER

The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

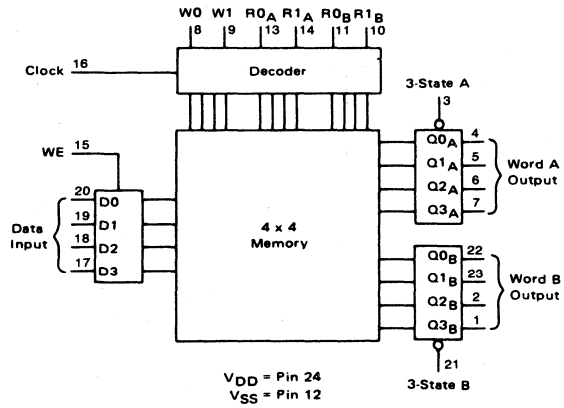
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin Compatible with CD40108

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

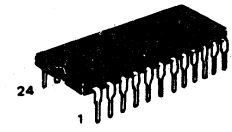
BLOCK DIAGRAM



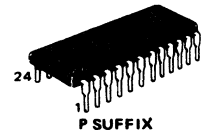
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

4 x 4 MULTIPORT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 623



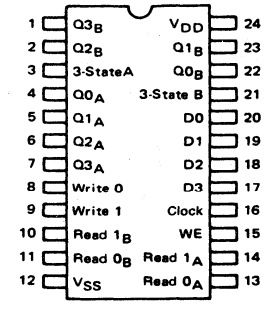
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.18 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.91 µA/kHz) f + I_{DD}							
		15	I_T = (2.67 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

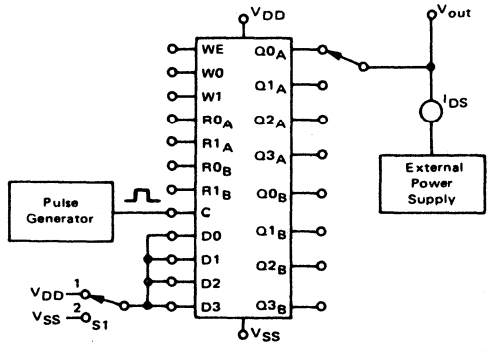
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SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns	(Figures 3 and 6)	10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	—	650	1300	ns
Clock to Output	(Figures 3 and 6)	10	—	250	500	
		15	—	170	340	
Write Enable Setup Time	t_{su}	5.0	800	400	—	ns
(Enabling a Write and Read)	(Figure 5)	10	300	150	—	
		15	200	100	—	
Write Enable Removal Time	t_{rem}	5.0	0	−100	—	ns
(Enabling a Write and Read)	(Figure 5)	10	0	−50	—	
		15	0	−35	—	
Setup Time**	t_{su}	5.0	50	20	—	ns
Address, Data to Clock	(Figure 3)	10	30	0	—	
		15	25	0	—	
Hold Time**	t_h	5.0	480	160	—	ns
Clock to Address, Data	(Figure 3)	10	195	65	—	
		15	150	50	—	
3-State Enable/Disable Delay Time	t_{PHZ}, t_{PLZ}	5.0	—	130	260	ns
	t_{PZH}, t_{PZL}	10	—	60	120	
	(Figures 4 and 7)	15	—	45	90	
Clock Pulse Width	t_w	5.0	820	410	—	ns
	(Figure 3)	10	330	165	—	
		15	220	110	—	

**When loading repetitive highs, the output may glitch low momentarily after the rising edge of Clock. However, data integrity remains unaffected and data is valid after the propagation delays listed in the Switching Characteristics Table.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

6

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

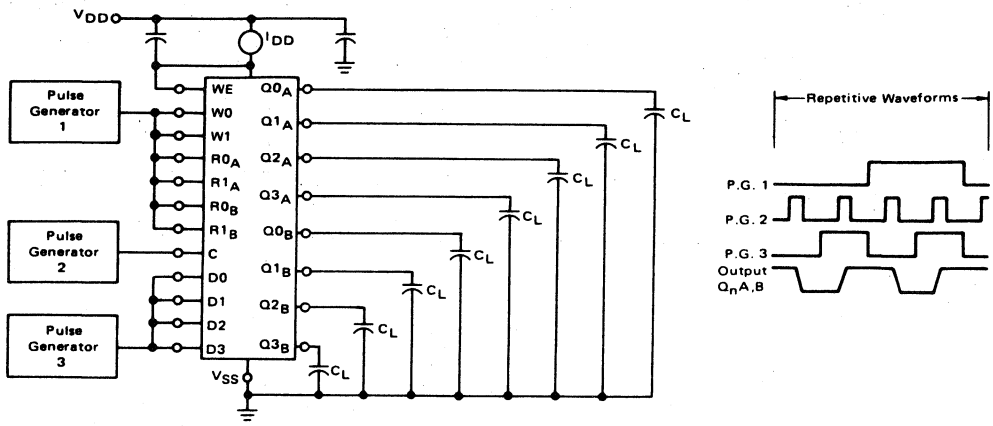


FIGURE 3

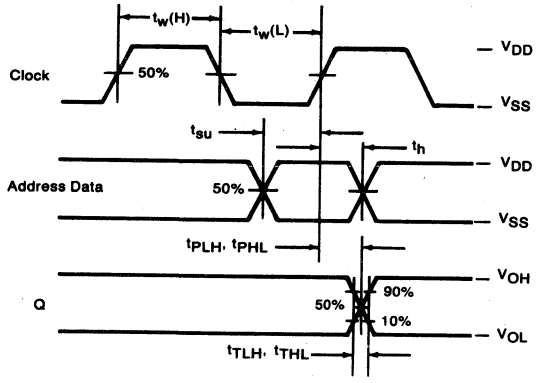


FIGURE 4

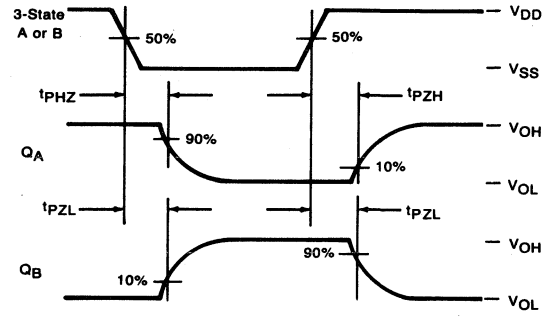


FIGURE 5

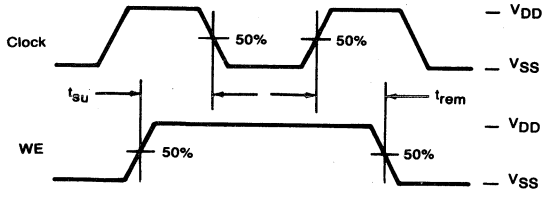


FIGURE 6 — TEST CIRCUIT

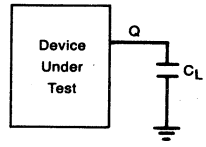
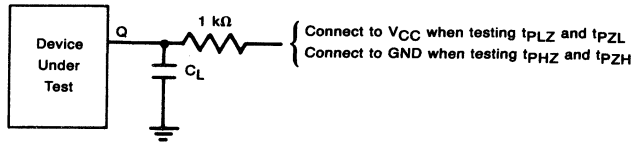
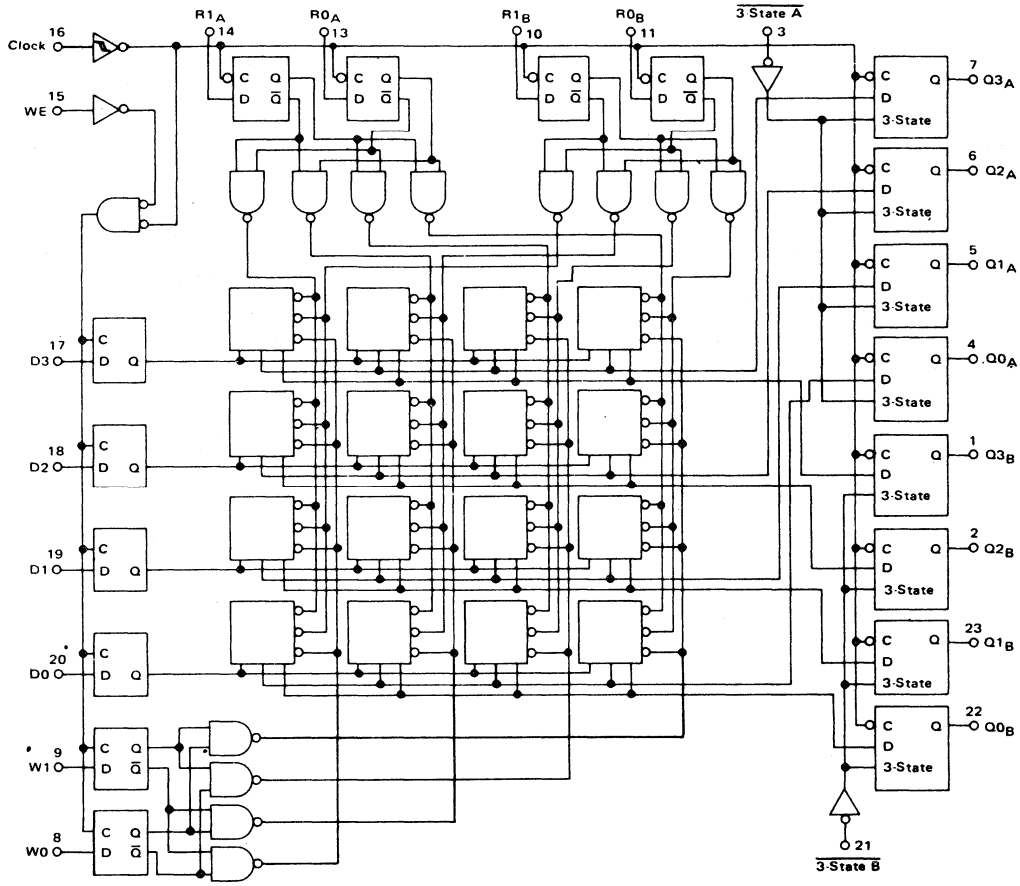


FIGURE 7 — TEST CIRCUIT



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
⌐¬	1	0	1	0	1	0	1	1	1	1	1	1
⌐¬	1	0	1	0	1	0	1	1	1	0	0	0
⌐¬	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	X	0	X	Z	Z
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⌐¬	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⌐¬	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

Z = High Impedance
X = Don't care

MOTOROLA

MC14581B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT

4-BIT ARITHMETIC LOGIC UNIT

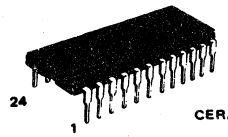
The MC14581B is a CMOS 4-bit ALU capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 14-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active Low	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

- Functional and Pinout Equivalent to 74181.
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 623



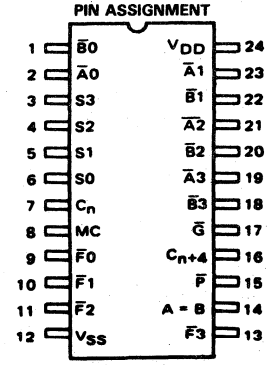
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

PIN ASSIGNMENT



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	-0.8	−1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.7 μA/kHz) f + I_{DD}							
		15	I_T = (5.5 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.008.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Sum in to Sum Out	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns		5.0	–	705	1410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to Sum Out (Logic Mode)	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 520 ns	t_{PHL}	5.0	–	605	1210	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	–	215	430	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to A = B	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 870 ns	t_{PHL}	5.0	–	955	1910	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	660	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 220 ns		15	–	245	490	
Sum In to P or G	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 400 ns	t_{PHL}	5.0	–	485	970	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Sum In to C_{n+4}	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 530 ns		5.0	–	615	1230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	440	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	360	
Carry In to Sum Out	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns	t_{PHL}	5.0	–	380	760	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 80 ns		15	–	105	210	
Carry in to C_{n+4}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS		DC DATA INPUTS		MODE	FIG. 3 WAVEFORM
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}		
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	$\overline{B}_0$	Any $\overline{F}$	All A's	M	Exclusive OR	#2

6

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

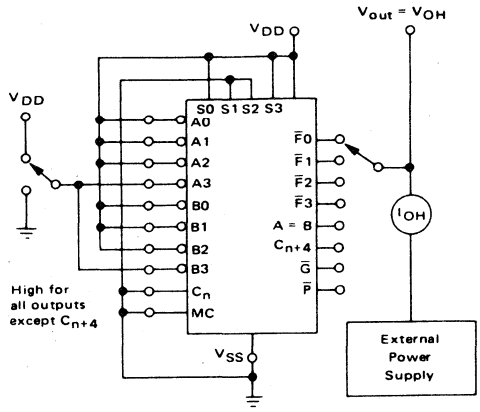


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

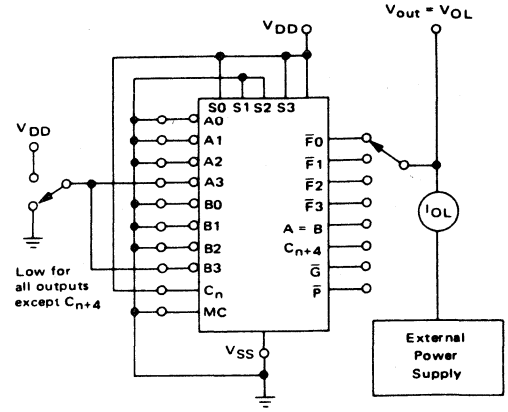


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

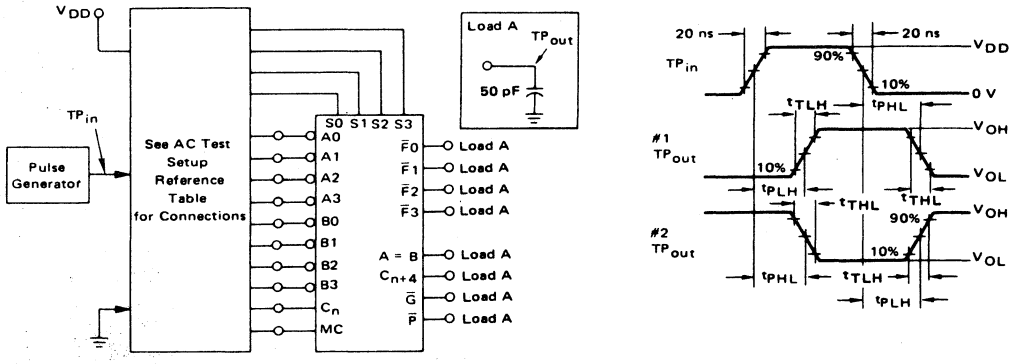
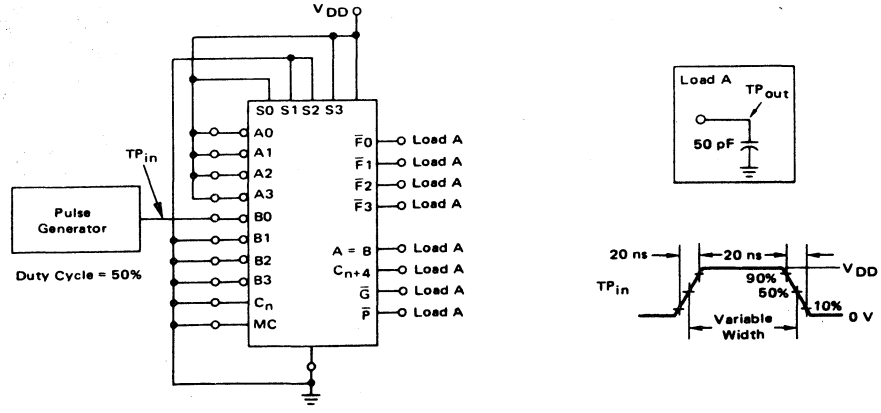
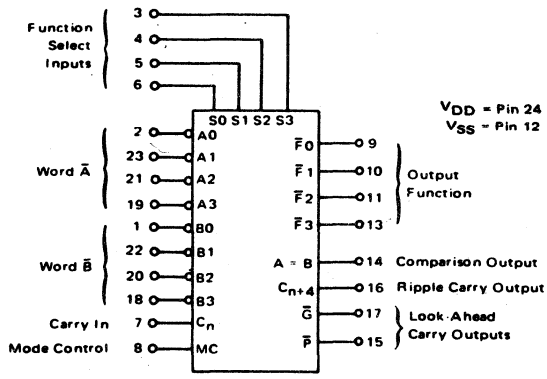


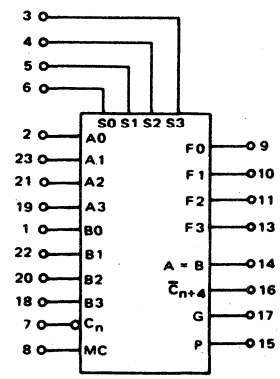
FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



BLOCK DIAGRAM (ACTIVE LOW)



BLOCK DIAGRAM (ACTIVE HIGH)



TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH *	
				LOGIC FUNCTION	ARITHMETIC* FUNCTION	LOGIC FUNCTION	ARITHMETIC* FUNCTION
S3	S2	S1	S0	(MC = H)	(MC = L, C_n = L)	(MC = H)	(MC = L, $\overline{C}_n$ = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{A\overline{B}}$	AB minus 1	$\overline{A+\overline{B}}$	A+B
L	L	H	L	$\overline{A}$+B	A$\overline{B}$ minus 1	$\overline{A}$B	A+$\overline{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+\overline{B}}$	A plus (A+$\overline{B}$)	$\overline{A\overline{B}}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A+$\overline{B}$)	$\overline{B}$	(A+B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A+$\overline{B}$	A+$\overline{B}$	A$\overline{B}$	A$\overline{B}$ minus 1
H	L	L	L	$\overline{A}$B	A plus (A+B)	$\overline{A+B}$	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A+B)	B	(A+$\overline{B}$) plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	A$\overline{B}$	AB plus A	A+$\overline{B}$	(A+B) plus A
H	H	H	L	AB	A$\overline{B}$ plus A	A+B	(A+$\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

6

MOTOROLA

MC14582B

CMOS MSI

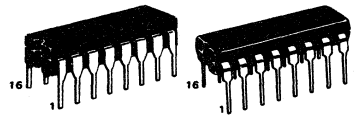
(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK

LOOK-AHEAD CARRY BLOCK

The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Expandable to any Number of Bits
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

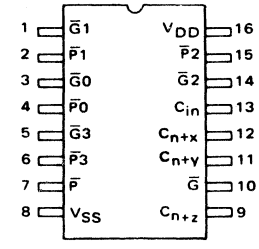
LOGIC EQUATIONS

$C_{n+x} = \overline{G0} + (\overline{P0} \bullet C_n)$
$C_{n+y} = \overline{G1} + (\overline{P1} \bullet \overline{G0}) + (\overline{P1} \bullet \overline{P0} \bullet C_n)$
$C_{n+z} = \overline{G2} + (\overline{P2} \bullet \overline{G1}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{G0}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{P0} \bullet C_n)$
$\overline{G} = \overline{G3} + (\overline{P3} \bullet \overline{G2}) + (\overline{P3} \bullet \overline{P2} \bullet \overline{G1}) + (\overline{P1} \bullet \overline{P2} \bullet \overline{P3} \bullet \overline{G0})$
$\overline{P} = \overline{P3} \bullet \overline{P2} \bullet \overline{P1} \bullet \overline{P0}$

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

PIN ASSIGNMENT



6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.4 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.8 μA/kHz) f + I_{DD}							
		15	I_T = (4.3 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

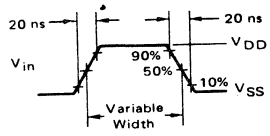
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 260 ns	t_{PHL}	5.0	–	345	690	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



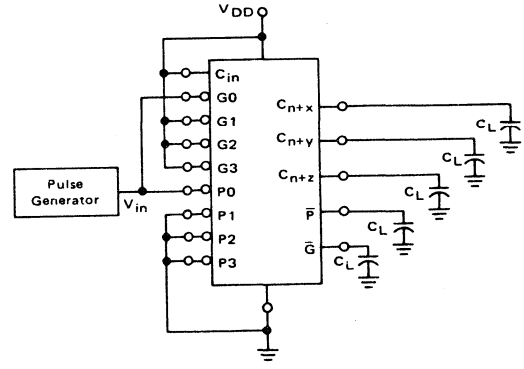


FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

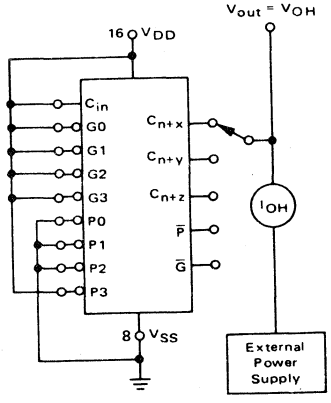
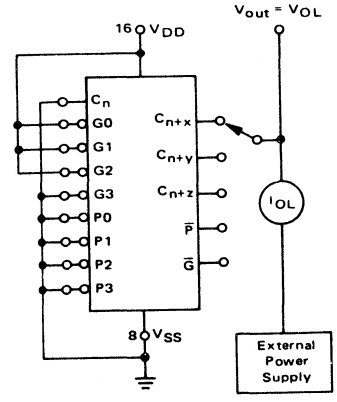
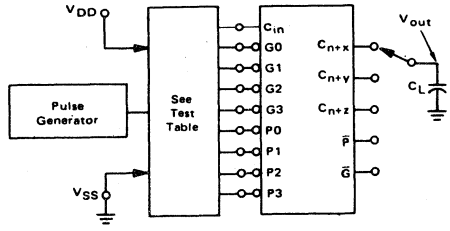


FIGURE 3 – SINK CURRENT TEST CIRCUIT



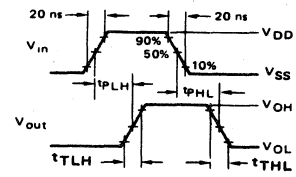
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FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

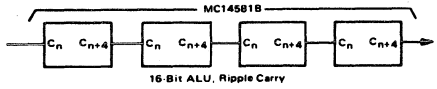


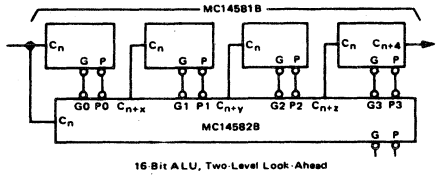
TEST TABLE

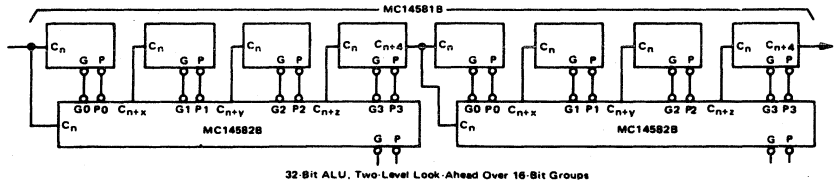
AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\bar{P}0$	$\bar{P}$	Remaining $\bar{P}$'s, C_n	$\bar{G}$'s
$\bar{G}0$	$\bar{G}$	$\bar{P}$'s, C_n	Remaining $\bar{G}$'s
C_n	C_{n+x}, C_{n+y}, C_{n+z}	$\bar{P}$'s	$\bar{G}$'s

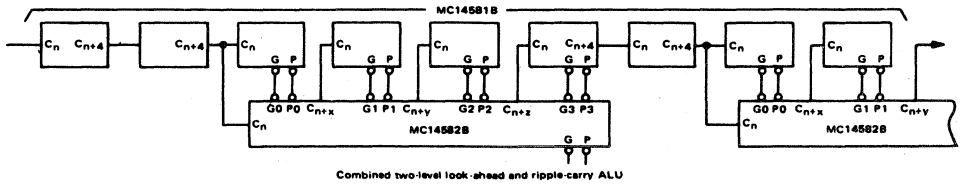


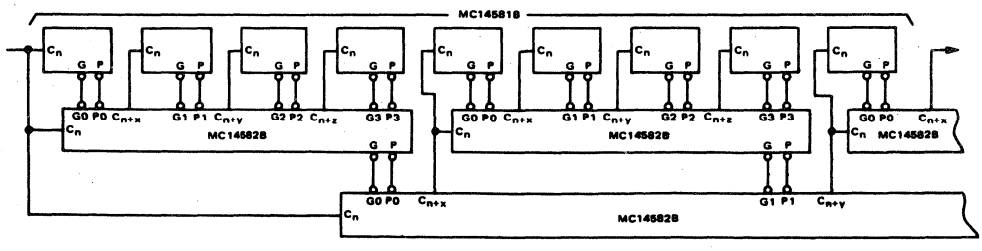
TYPICAL APPLICATIONS











A and B inputs and F outputs are not shown (MC14581B).

MOTOROLA

MC14583B

DUAL SCHMITT TRIGGER

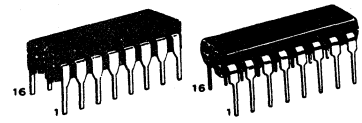
The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

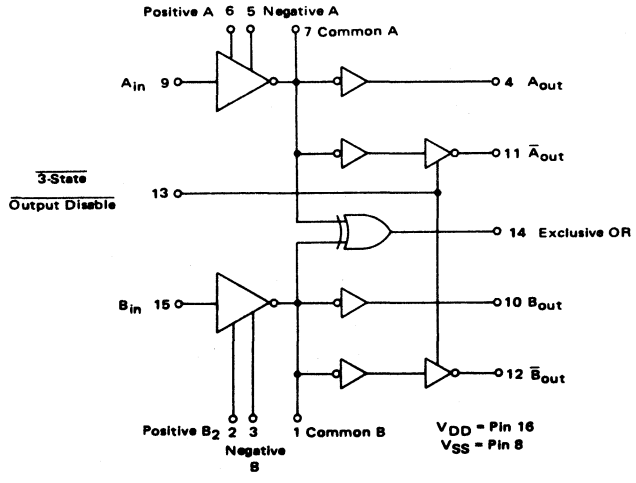
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

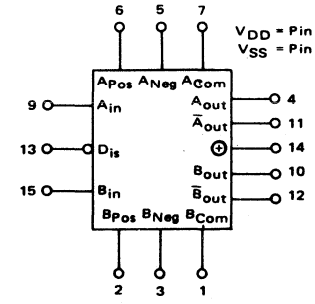
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

LOGIC DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\bar{A}_{out}$	B_{out}	$\bar{B}_{out}$	⊕
0	0	0	0	Z	0	Z	0
0	0	1	0	1	0	1	0
0	1	0	0	Z	1	Z	1
0	1	1	0	1	1	0	1
1	0	0	1	Z	0	Z	1
1	0	1	1	0	0	1	1
1	1	0	1	Z	1	Z	0
1	1	1	1	0	1	0	0

Z = High impedance at output

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in}=V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in}=0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage A and B "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.33 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.65 μA/kHz) f + I_{DD}							
		15	I_T = (3.98 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

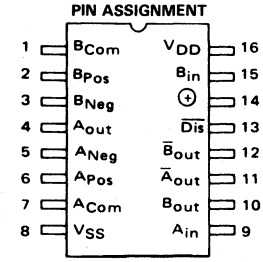
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.005.

PIN ASSIGNMENT



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

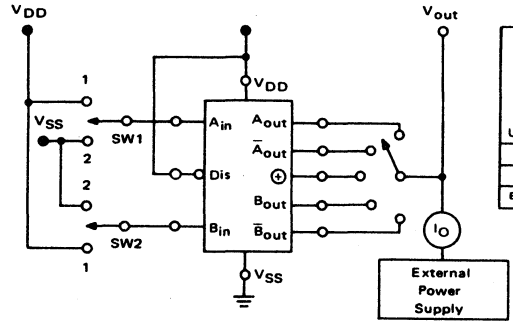
Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A_{in}, B_{in} to A_{out}, B_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
A_{in}, B_{in} to A_{out}, B_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1015 ns	t_{PHL}	5.0	–	1100	2200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 347 ns		10	–	380	760	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 235 ns		15	–	260	520	
A_{in}, B_{in} to Exclusive OR	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns	t_{PHL}	5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns		10	–	280	560	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
3-State Enable, Disable Delay Time (see figure 5)	t_{on},					ns
t_{on}, t_{off} = (1.7 ns/pF) C_L + 140 ns	t_{off}	5.0	–	225	450	
t_{on}, t_{off} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{on}, t_{off} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	
Positive Threshold Voltage	V_{T+}	5.0	–	3.30	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	5.70	–	
		15	–	8.20	–	
Negative Threshold Voltage	V_{T-}	5.0	–	1.70	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	4.30	–	
		15	–	6.80	–	
Hysteresis Voltage	V_H	5.0	0.85	1.70	3.40	Vdc
(R1, R2 = 5.0 kΩ)		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	
Threshold Voltage Variation, A to B	ΔV_T	5.0	–	0.1	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	0.15	–	
		15	–	0.20	–	

*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6

FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS: TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		OUTPUT SINK CHARACTERISTICS: TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

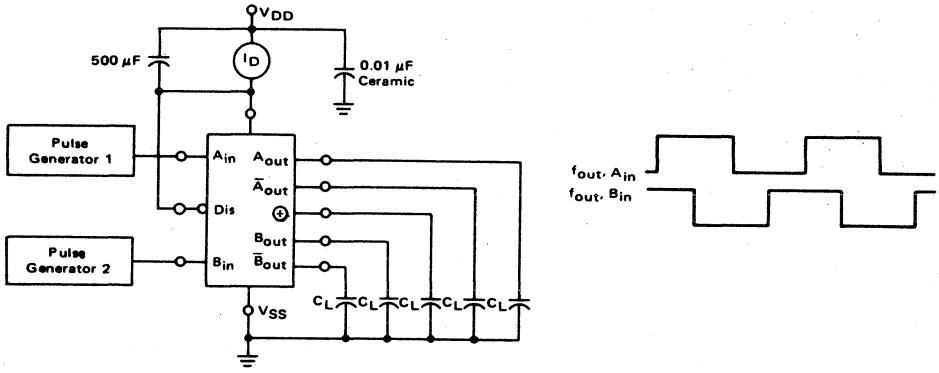
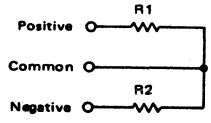
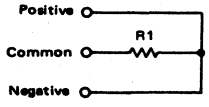


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



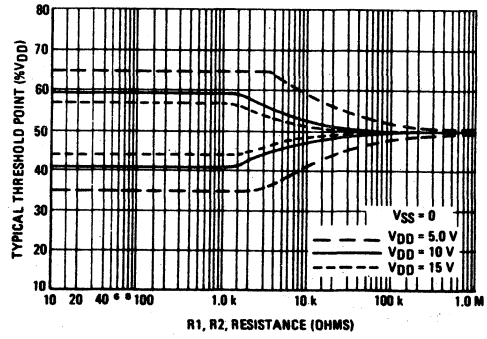
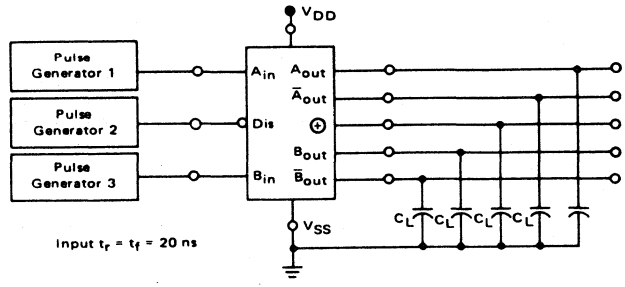
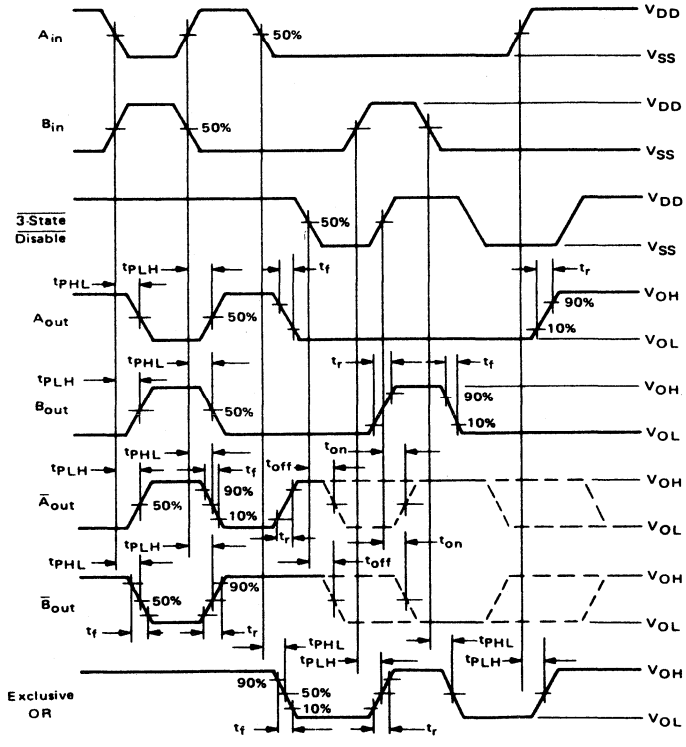


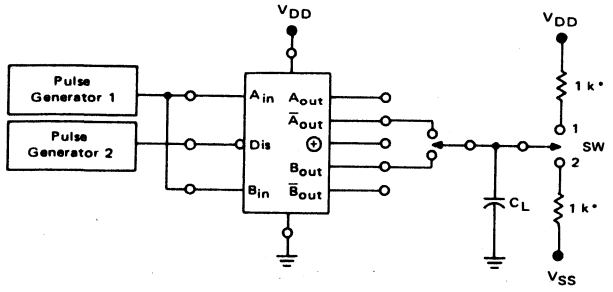
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





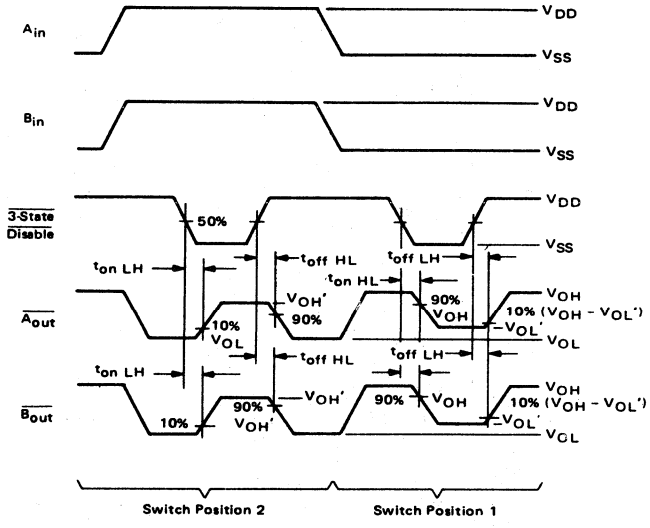
Note: Dashed lines indicate high output resistance.

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
t_{on} HL	1
t_{on} LH	2
t_{off} HL	2
t_{off} LH	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

6

MOTOROLA

MC14584B

CMOS SSI

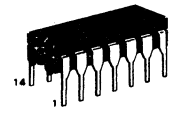
(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER

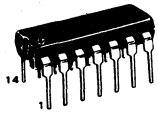
HEX SCHMITT TRIGGER

The MC14584B Hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity to "square up" slowly changing waveforms.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysterisis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

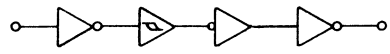
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

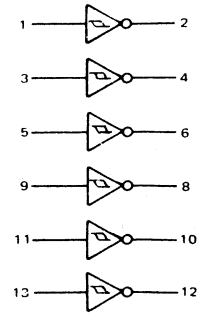
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	34	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.8\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.4\ \mu A/kHz)\ f + I_{DD}$							
Hysteresis Voltage	V_H‡	5.0	0.27	1.0	0.25	0.6	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.30	0.70	1.2	0.25	1.2	
		15	0.77	1.7	0.60	1.1	1.5	0.50	1.4	
Threshold Voltage Positive-Going	V_{T+}	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	V_{T-}	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ V f k$$

where: I_T is in µA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

‡$V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than $V_{T+\ max} - V_{T-\ min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

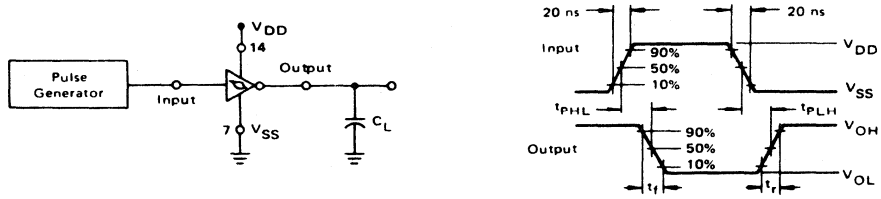


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS

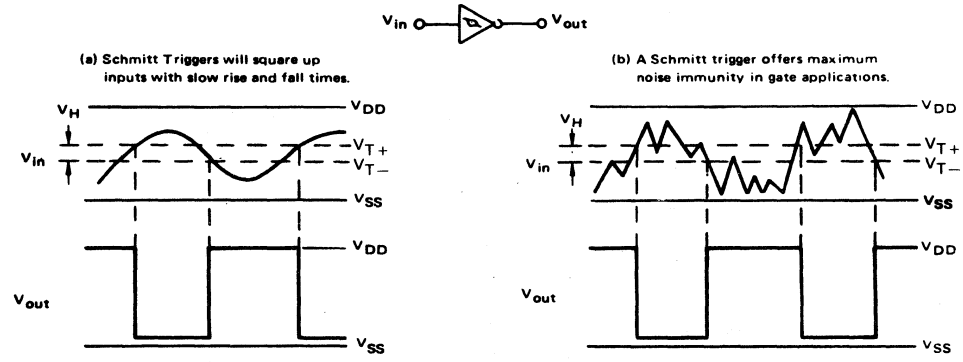
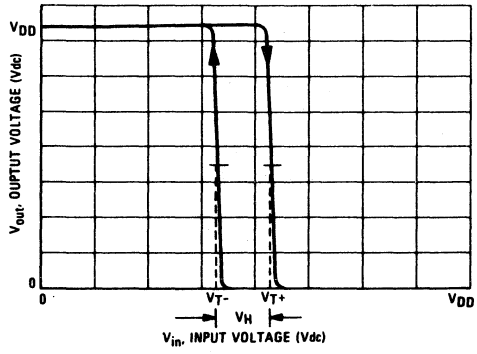
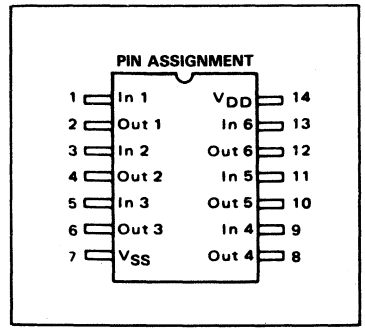


FIGURE 3 – TYPICAL TRANSFER CHARACTERISTICS





6

MOTOROLA

MC14585B

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

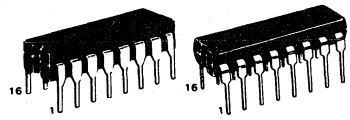
4-BIT MAGNITUDE COMPARATOR

4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A>B), (A<B), and (A=B) to the corresponding inputs of the next significant comparator. Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range
- Can be Cascaded - See Fig. 3



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

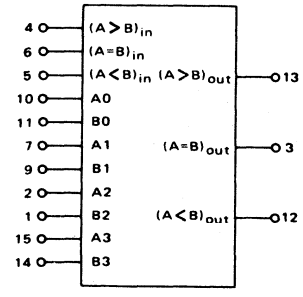
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	×	×	×	×	×	×	0	0	1
A3=B3	A2>B2	×	×	×	×	×	0	0	1
A3=B3	A2=B2	A1>B1	×	×	×	×	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	×	×	×	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	×	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	×	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	×	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	1	1	×	1	1	0
A3=B3	A2=B2	A1=B1	A0<B0	×	×	×	1	0	0
A3=B3	A2=B2	A1<B1	×	×	×	×	1	0	0
A3=B3	A2<B2	×	×	×	×	×	1	0	0
A3<B3	×	×	×	×	×	×	1	0	0

× = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

6

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.8 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

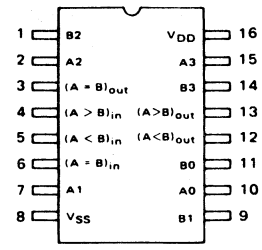
**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

PIN ASSIGNMENT



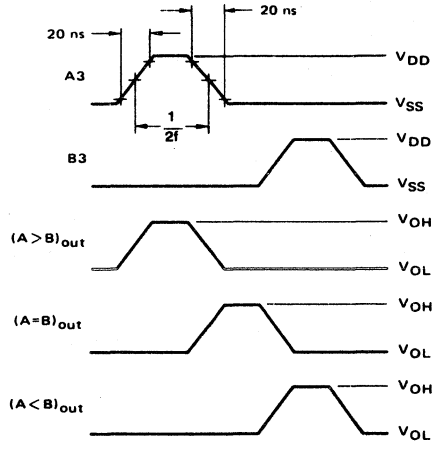
6

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Turn-On, Turn-Off Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	860	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	

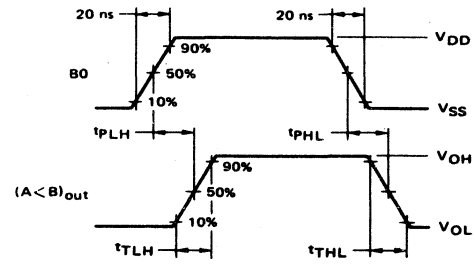
*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low
f in respect to a system clock.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

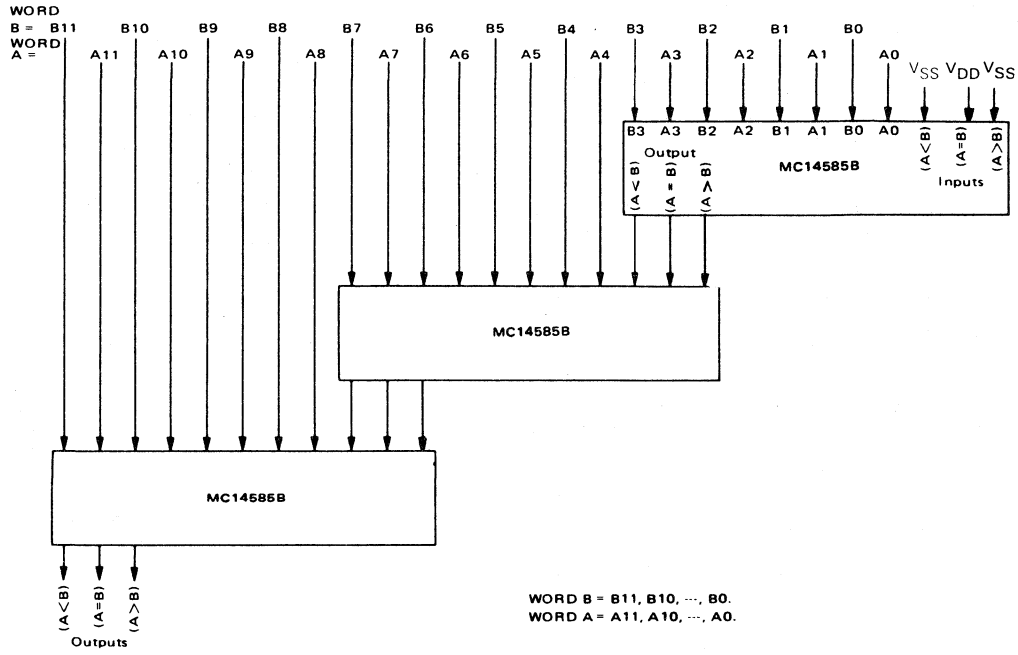


Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A< B) low.

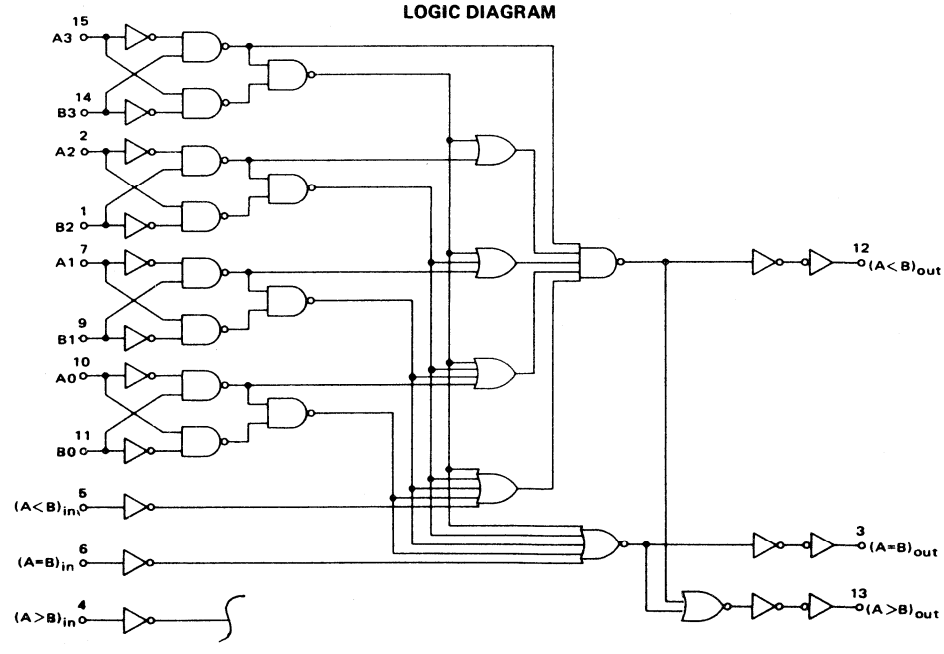
6

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

FIGURE 3 – CASCADING COMPARATORS



LOGIC DIAGRAM



MOTOROLA

MC14597B
MC14598B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT, BUS-COMPATIBLE THREE-STATE LATCHES

Internal Counter — MC14597B
Binary Address — MC14598B

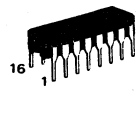
8-BIT BUS-COMPATIBLE LATCHES

The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the MC14597B to indicate the position of the Address counter.

All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
  With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads



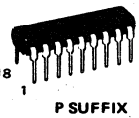
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

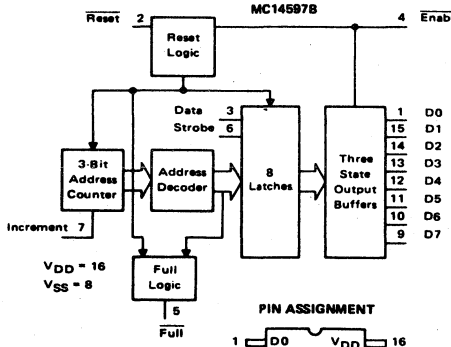
ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

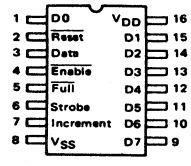
C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

BLOCK DIAGRAMS

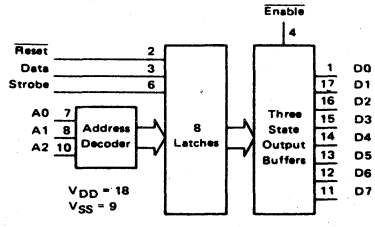
MC14597B



PIN ASSIGNMENT



MC14598B

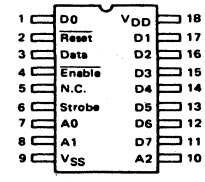


OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedance
0	D_n

D_n = State of nth latch

PIN ASSIGNMENT



NC = No Connection

6

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}	Input Voltage, $\overline{\text{Enable}}$ (DC or Transient)	−0.5 to V_{DD} +0.5	V
V_{in}	Input Voltage, All other Inputs (DC or Transient)	−0.5 to V_{DD} +12	V
V_{out}	Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage** — $\overline{\text{Enable}}$ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 Vdc)		10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.4	–	3.4	2.4	–	2.4	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 Vdc)		10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	10	–	10	4.3	–	10	–	
Input Voltage "0" Level	V_{IL}									Vdc
Other Inputs										
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current Source	I_{OH}									mAdc
($\overline{\text{Full}}$—Sink Only)										
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-1.0	-2.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)		10	–	–	–	-6.0	–	–	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	–	–	–	6.0	–	–	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	12	–	–	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Three-State Leakage Current	I_{TL}									μAdc
(AL Device)		15	–	±0.1	–	±0.00001	±0.1	–	±3.0	
(CL/CP Device)		15	–	±1.0	–	±0.00001	±1.0	–	±7.5	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an External Load Capacitance of 130 pF	I_T	5.0	I_T = (2.0 μA/kHz)f + I_{DD}							μAdc
		10	I_T = (4.0 μA/kHz)f + I_{DD}							
		15	I_T = (6.0 μA/kHz)f + I_{DD}							

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

** The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

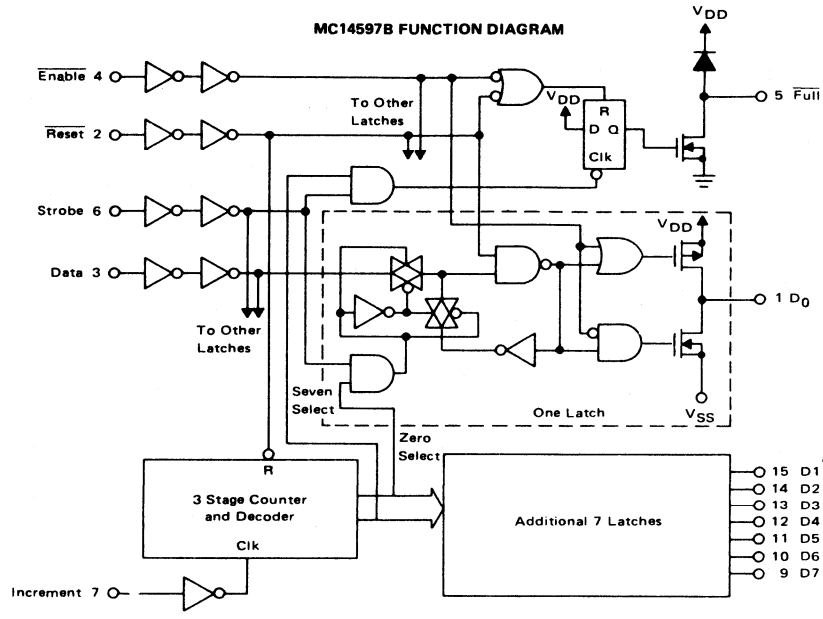
6

SWITCHING CHARACTERISTICS* (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

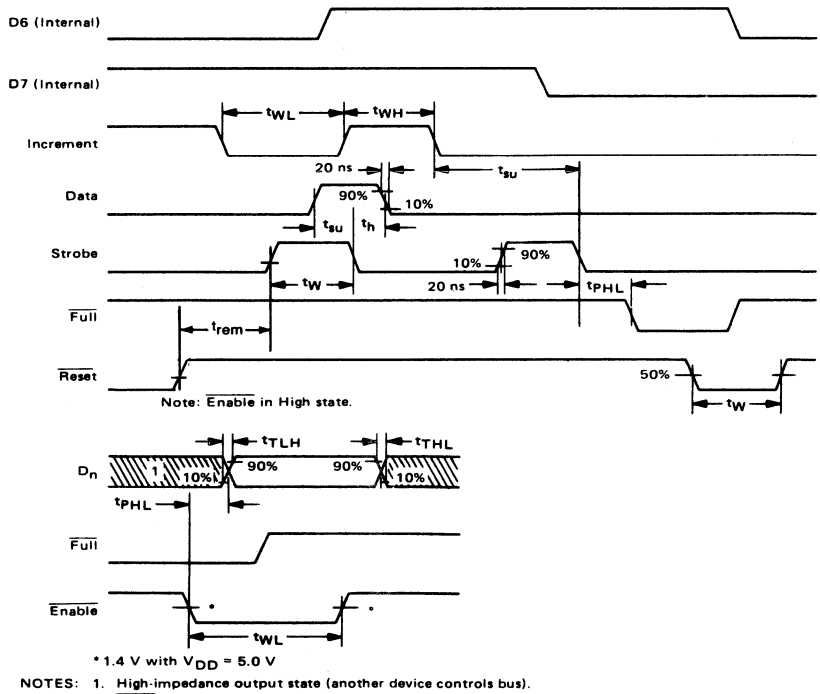
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L +35 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L +25 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L +20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
$\overline{\text{Enable}}$ to Output		5.0	–	160	320	
		10	–	125	250	
		15	–	100	200	
Strobe to Output		5.0	–	200	400	
		10	–	100	200	
		15	–	80	160	
Strobe to $\overline{\text{Full}}$ (MC14597B only)		5.0	–	200	400	
		10	–	100	200	
		15	–	80	160	
$\overline{\text{Reset}}$ to Output		5.0	–	175	350	
		10	–	90	180	
		15	–	70	140	
Pulse Width	t_{WH}, t_{WL}					ns
$\overline{\text{Enable}}$		5.0	320	160	–	
		10	240	120	–	
		15	160	80	–	
Strobe		5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
Increment (MC14597B only)		5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
$\overline{\text{Reset}}$		5.0	300	150	–	
		10	160	80	–	
		15	100	50	–	
Setup Time	t_{su}					ns
Data		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only),		5.0	200	100	–	
		10	100	50	–	
		15	70	35	–	
Increment (MC14597B only)		5.0	400	200	–	
		10	200	100	–	
		15	170	85	–	
Hold Time	t_h					ns
Data		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only)		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
$\overline{\text{Reset}}$ Removal Time	t_{rem}	5.0	20	−25	—	ns
		10	20	−15	—	
		15	20	−10	—	

*The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14597B FUNCTION DIAGRAM



MC14597B TIMING DIAGRAMS

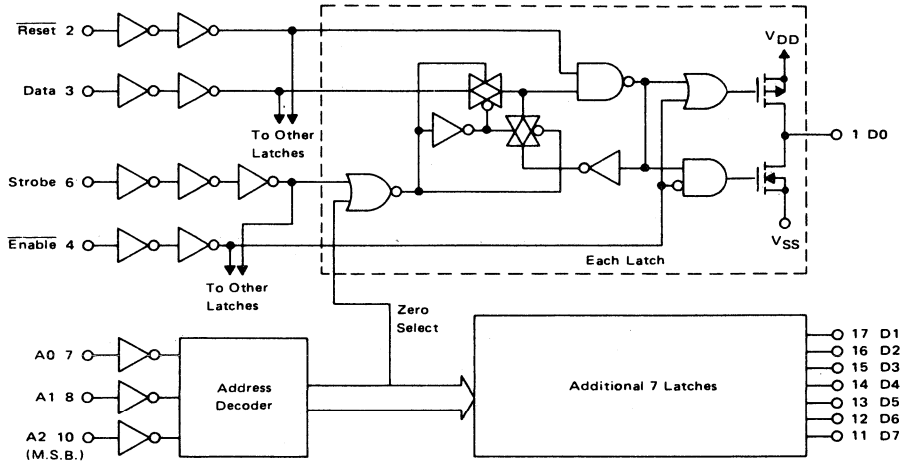


* 1.4 V with V_{DD} = 5.0 V

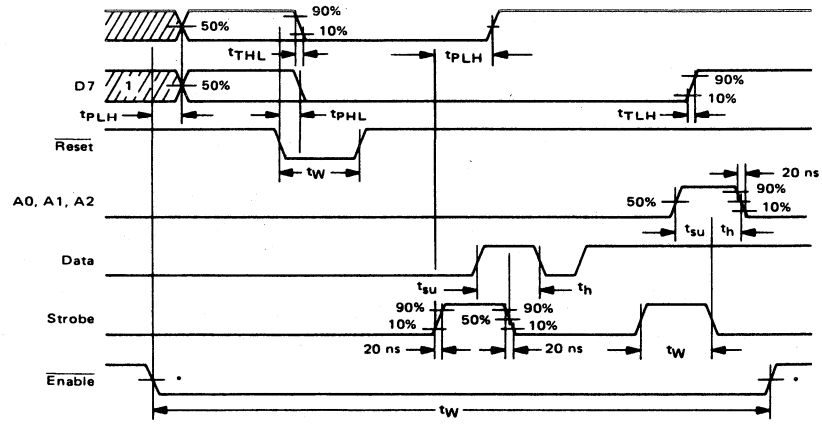
NOTES: 1. High-impedance output state (another device controls bus).
2. Reset in High state.

6

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



* 1.4 V with V_{DD} = 5.0 V.

NOTES 1. High-impedance output state (another device controls bus).
2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Addressed Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

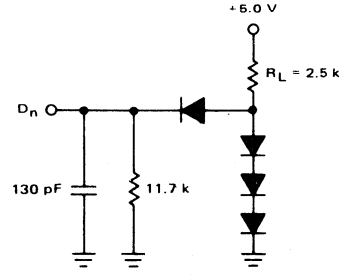
* = No change in state of latch
X = Don't care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
↓	X	1	Count Up	–
↑	X	1	No Change	–
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

Test Load
All Outputs



Circuit diagrams external to or containing Motorola products are included as a means of illustration only. Complete information sufficient for construction purposes may not be fully illustrated. Although the information herein has been carefully checked and is believed to be reliable, Motorola assumes no responsibility for inaccuracies. Information herein does not convey to the purchaser any license under the patent rights of Motorola or others.

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MOTOROLA

MC14599B

FOR COMPLETE DATA
SEE MC14099B

8-BIT ADDRESSABLE LATCH

The MC14599B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. The data pin is a bidirectional data port, which is controlled by the Write/Read line.

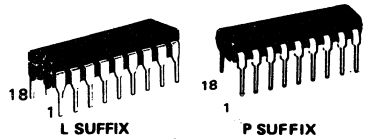
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH
WITH BIDIRECTIONAL PORT



L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

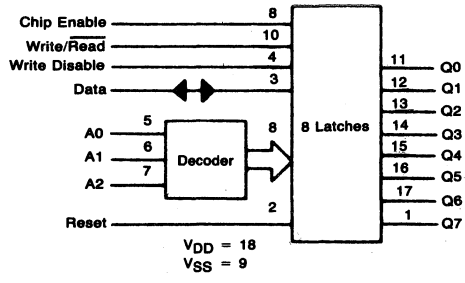
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

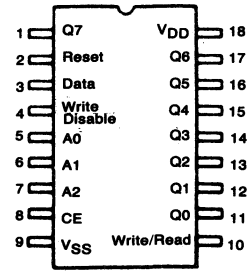
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14599B



PIN ASSIGNMENT



6

CMOS Reliability

7

MOTOROLA

Introduction

This chapter is intended to demonstrate the quality and reliability aspects of the semiconductor products supplied by Motorola.

Quality in Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is its philosophy to "design in" reliability. At all development points of any new design, reliability orientated guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola's Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola incoming inspection specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

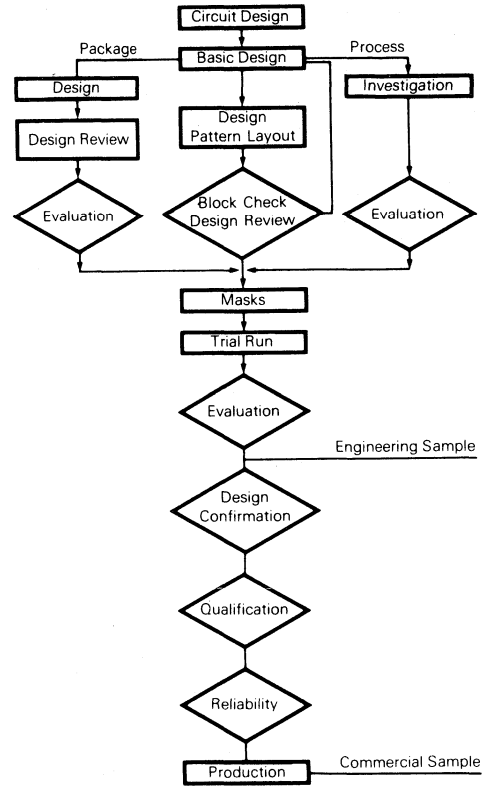
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



This basic design flow-chart omits some feedback loops for simplicity

7

WAFER FABRICATION

All processing stages of Motorola products are subjected to demanding manufacturing and quality control standards. A philosophy of "Do it Right the First Time" is instrumental in assuring that Motorola has a reliability record second to none.

The Bipolar and MOS Wafer Fabrication flow charts are examples which highlight the various in-process control points audited by both Manufacturing and Quality people. The majority of these inspections are control audit points with inspection gates at critical points of the process. This is in line with Motorola policy of all personnel being responsible for quality at each manufacturing stage.

Diffusion and ion implantation processing is subject to oxide thickness controls penetration evaluations. Controls are also performed on resistivity and defect density. Diffusion furnaces, metallization, and passivation equipment are subjected to daily qualification requirements by using C-V plotting techniques. C-V techniques are also used to ensure ongoing stability as they do provide a very sensitive measurement of ionic species concentration.

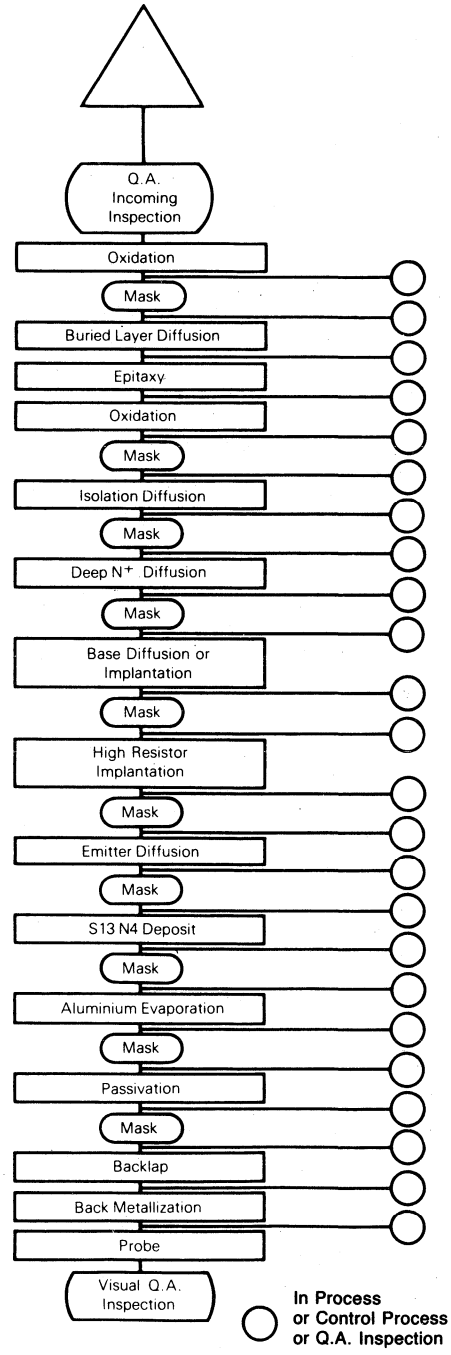
In addition, many other specific controls are used as a means to ensure built-in reliability and provide statistical data, which include:

- Environmental monitoring for humidity, temperature and particles
- Deionized water resistivity, particles and bacteria checks in water
- Epitaxial material: resistivity — thickness — crystal defects
- Oxide: thickness — charges — pinhole density
- Metallization: thickness — adherence — metal composition — ohmic contacts
- Doping profiles
- Pre and post etch inspections
- In process SEM analysis for step coverage: metallization — grain size — phosphorous concentration
- Passivation integrity checks
- Calibration
- Final visual inspection gate

After all processing stages are completed, every wafer lot is subject to a detailed electrical parameter check. Parameters such as threshold voltage, junction breakdown voltages, resistivity, field inversion voltages, etc., are measured and each batch is sentenced accordingly. The data generated at this point is treated statistically as a control on the distribution of each key electrical parameter, thus allowing corrective action adjustments to be implemented in a timely manner.

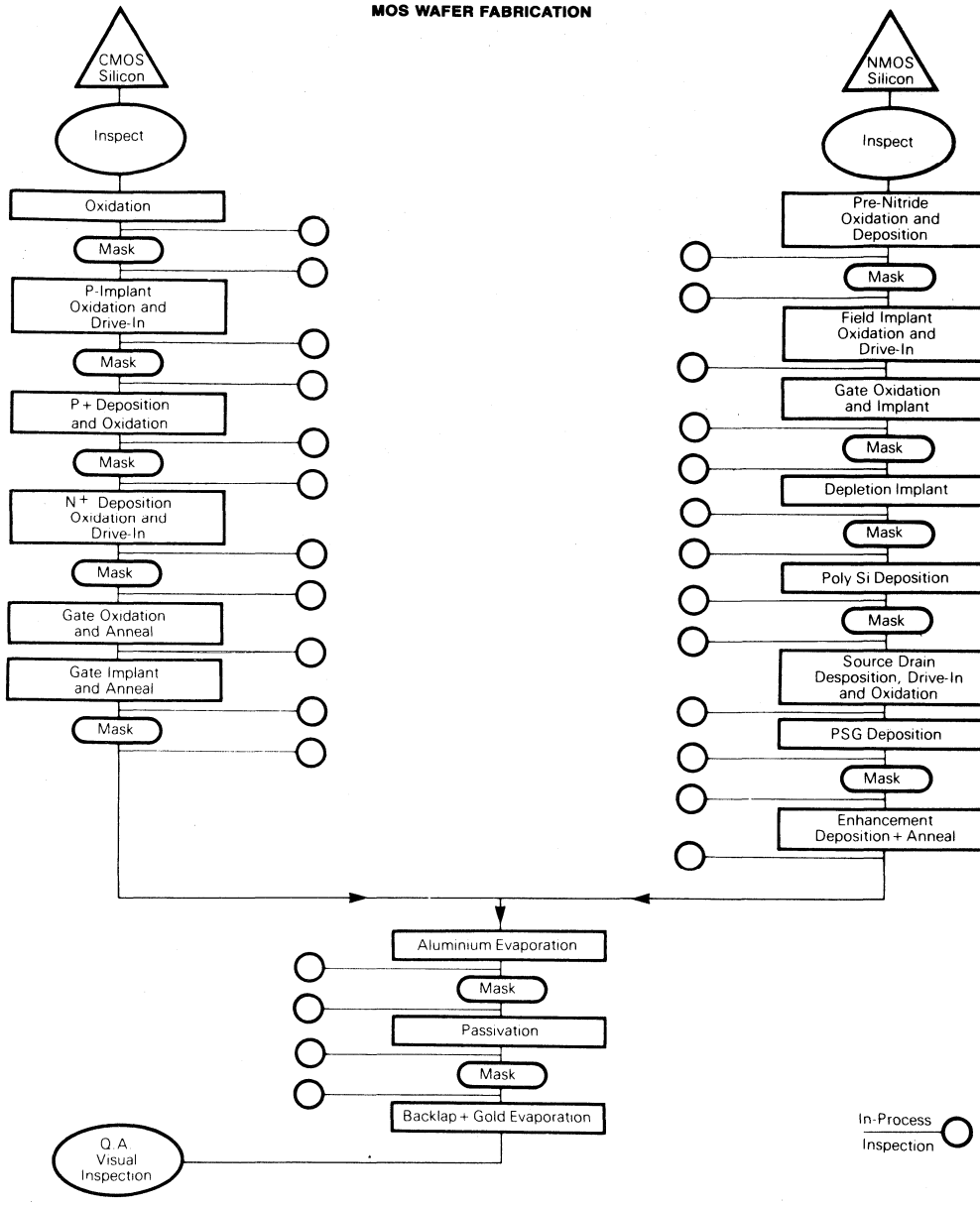
Every wafer lot is submitted to an electrical probe test during which every individual die is tested to its electrical specification. Chips which fail are individually inked.

BIPOLAR WAFER FABRICATION



7

MOS WAFER FABRICATION



ASSEMBLY

The assembly operation is of equal importance to the wafer fabrication process as a manufacturing activity which will affect the reliability of the finished product. Motorola continuously makes major investments in specialized assembly areas located in Malaysia, the Philippines and Korea. These assembly plants employ the latest technologies available to ensure that all Motorola semiconductors are produced to the highest standards of Quality and Reliability. In addition, each wafer fabrication facility has in-house assembly capability which allows some production, specific engineering activity, and qualification of piece-parts suppliers. The major production volumes of Motorola's Integrated Circuits are assembled offshore in the Far East.

Identical Quality and Reliability philosophies are practiced in the assembly areas as within the wafer fabrication facilities. Quality Assurance Audits for immediate corrective actions are performed after major process steps as demonstrated in the flow-chart. In addition, screening options are available. The statistical data obtained from quality audits are reported to the appropriate business centers either daily, weekly, or monthly for review.

Motorola is particularly aware of the major impact moisture can have on the reliability performance of either plastic or ceramic parts. With this in mind, several major new innovations have been introduced to safeguard Motorola products, and thus enhance their overall reliability performance. These include:

- Faraday shield vacuum packed wafer shipping system
- Temperature and humidity controlled wafer inventory stores
- Inert atmosphere for metal can packages encapsulation
- New design lead frames (plastic assembly)
- New molding compounds
- Low moisture content glass
- Moisture content audit procedures
- Super dry piece-part controls

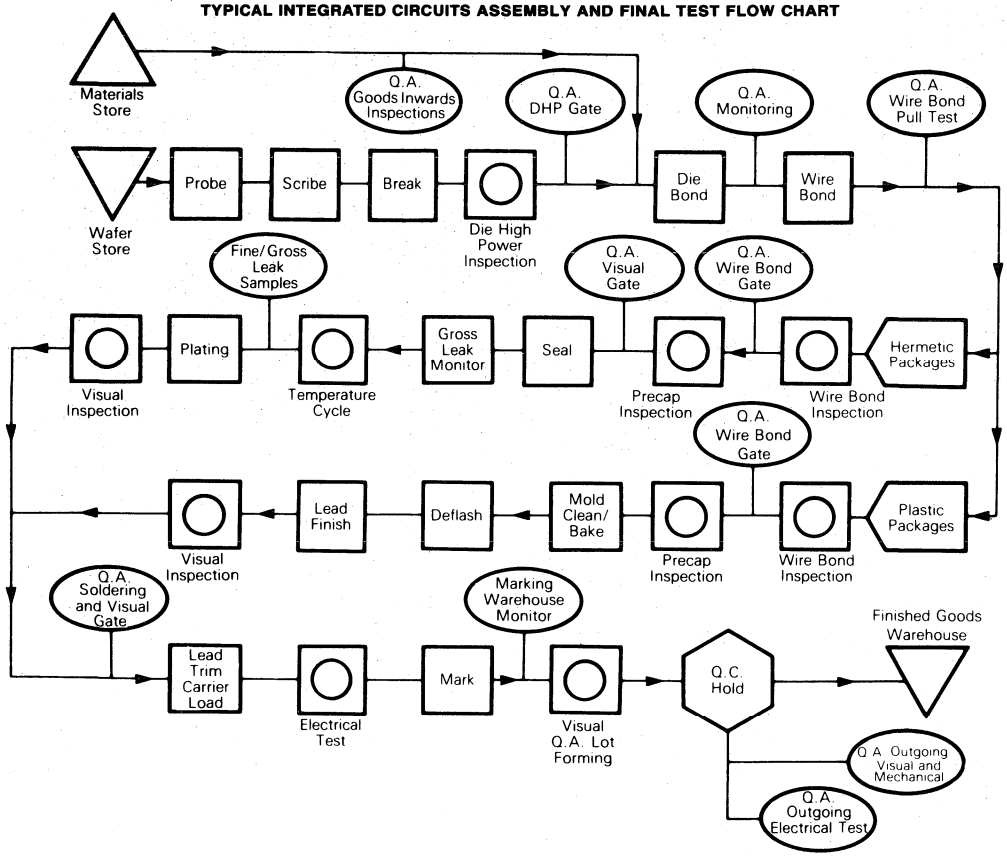
FINAL TESTING

Each of Motorola's facilities has a complete Final Test capability for all of the products fabricated and assembled. The majority of products, after assembly, are tested and Q.A. released at the facility responsible for that product. Some product is tested in the offshore assembly site; however, this is always returned to the facility for Q.A. release prior to final shipment to customer.

Final Test is a comprehensive series of dc, functional and speed oriented electrical tests as well as adapted forced tests. These tests are normally more stringent than data sheet requirements and are finally sampled by Outgoing Quality Assurance.

In practice, the test flow philosophies vary according to product. For instance, most of the Discrete devices are double tested as part of a zero defect quality improvement program. As well, many integrated Circuits are tested at various temperatures. There are also many burn-in options available.

TYPICAL INTEGRATED CIRCUITS ASSEMBLY AND FINAL TEST FLOW CHART



7

OUTGOING QUALITY SAMPLING PLAN

		A.Q.L. 1979	1980	1981	1982	1983	1984	1985
CMOS	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.065	0.065
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.10	0.10
MOS Microprocessors	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.10	0.10
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.10	0.10
NMOS Memories	Function/Parametric	LTPD	LTPD	0.15	0.10	0.10	0.065	0.065
	Visual/Mechanical	(5.0)	(5.0)	0.15	0.15	0.15	0.065	0.065

OUTGOING QUALITY

Although test procedures may vary from product to product within Motorola, the same philosophy applies when considering quality objectives. Motorola's mission is to be a Quality and Reliability leader worldwide.

HIGHLIGHTS:

Motorola recognizes that you, our customers, are truly concerned about improving your own quality image. You are, therefore, concerned about the quality of the product Motorola supplies you.

Our customers measure us by the level of defects in the products we supply at incoming inspection, assembly, and, most important, field reliability.

During the past years, Motorola has achieved impressive reductions in defect rates known as A.O.Q. or Average Outgoing Quality. Instrumental in this success has been the planned continuous reduction in outgoing A.Q.L. to a point where Motorola believes that over all products it can demonstrate the most aggressive A.Q.L.'s in the industry.

This aggressive program has been designed to help eliminate expensive incoming inspection at our customers.

All the facilities also practice an extremely demanding parts per million program (PPM).

The PPM performance of all Motorola products is calculated in each location using the same method. They are, therefore, directly comparable. Motorola is well aware that when discussing PPM with existing potential customers, it is of paramount importance to explain exactly which failure categories are included in the stated PPM figures. Motorola's PPM figures will include:

- Electrical Inoperative Failure
- Electrical Parametric Failures (dc and ac)
- Visual and Mechanical criteria

In many published cases, stated PPM values refer to Electrical Inoperative failures only.

At Motorola, the Electrical Inoperative, the Electrical Parametric, and the Visual/Mechanical failure rates are calculated separately and then combined to reach an overall total. In this way Motorola believes that it is giving its customers a true and accurate assessment of the quality of the product. Unqualified PPM statements can be misleading and cause the customer to expect quality levels which cannot be achieved. For example, Motorola MOS Logic and Analog IC A.O.Q. is separated into Electrical Inoperative/Electrical Parametric (259 PPM) and Visual/Mechanical (419 PPM). Other product families such as Small Signal Plastic Transistors are already reaching 50 PPM in Electrical Inoperative failure rate.

The Motorola PPM graphs are excellent examples of what has been achieved over the last years with regard to quality improvements.

Improvements between 50% and 300% in average outgoing quality are typical across the broad range of Motorola products.

Throughout the semiconductor industry there have been, and there still are, examples of manufacturers offering higher quality standards at a premium. This is **not** a Motorola strategy, we believe that our customers should expect high quality products at no extra cost. This is Motorola's aim and we will continue to aggressively pursue Quality and Reliability improvements which will be passed on to our customers as an obligation on our part.

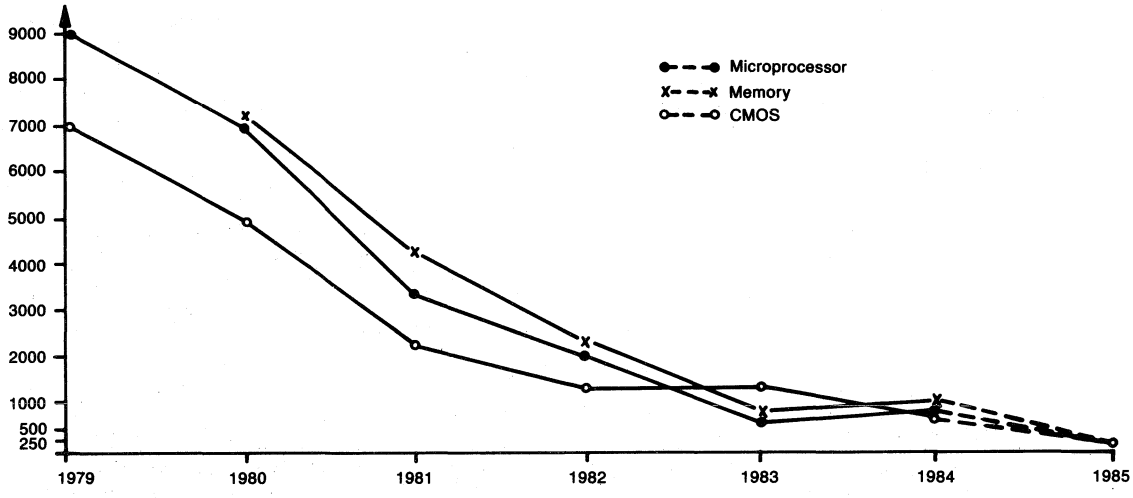
Also, we actively encourage our customers to provide their quality results at their incoming inspection, during their manufacturing process, and from the field in order to better correlate and further improve our quality performance.

MOTOROLA A.O.Q. PLAN

	1980	History Average 1981	1982	Dec 1982	1983	1984	Goal 1985
MOS LOGIC and Analog IC	5000	2370	1380	1150	1399	701	100
Memory	7000	4360	2400	2900	918	899	100
Microprocessor	7000	3860	2450	2900	763	825	100

A.O.Q. Includes all Defects: Visual, Mechanical, Electrical Inoperative, and Parametric.

AVERAGE A.O.Q. IN P.P.M. FOR MOS PRODUCTS FIGURES
INCLUDE FUNCTIONAL/PARAMETRIC/VISUAL/MECHANICAL



RELIABILITY

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of troublefree service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. The following discussion will attempt to present an overview of Motorola's reliability efforts.

BASIC CONCEPTS

It is essential to begin with an explanation of the various parameters of Reliability. These are probably summarized best in the Bathtub Curve (Figure 1). The reliability performance of a device is characterized by three phases: infant mortality, useful life, and wearout. When a device is produced, there is often a small distribution of failure mechanisms which will exhibit themselves under relatively moderate stress levels and therefore appear early. This period of early failures, termed infant mortality is reduced significantly through proper manufacturing controls and screening techniques. The most effective period is that in which only occasional random failure mechanisms appear. The useful life typically spans a long period of time with a very low failure rate. The final period is that in which the devices literally wear out due to continuous phenomena which existed at the time of manufacture. Using strictly controlled design techniques and selectivity in applications, this period is shifted well beyond the lifetime required by the user.

FIGURE 1

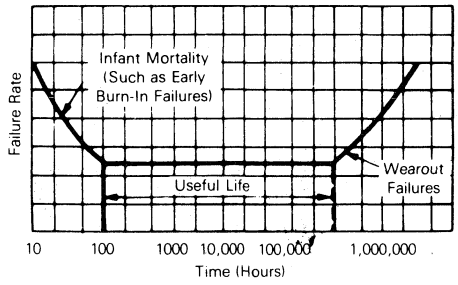
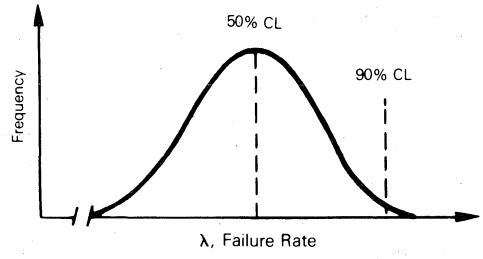


FIGURE 2



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Both the infant mortality and random failure rate regions can be described through the same types of calculations. During this time the probability of having no failures to a specific point in time can be expressed by the equation:

$$P_O = e^{-\lambda t}$$

where λ is the failure rate and t is time. Since λ is changing rapidly during infant mortality, the expression does not become useful until the random period, where λ is relatively constant. In this equation λ is failures per unit of time. It is usually expressed in percent failures per thousand hours. Other forms include FIT (Failures in Time = (%/10^3 hrs) $\times$ 10^{-4} = 10^{-9} failures per hour) and MTTF (Mean Time To Failure) or MTBF (Mean Time Between Failures), both being equal to $1/\lambda$ and having units of hours.

Since reliability evaluations usually involve only samples of an entire population of devices, the concepts of the Central Limit Theorem apply and λ is calculated using x^2 distribution through the equation:

$$\lambda \leq \frac{x^2\,(x,\ 2r + 2)}{2nt}$$

$$\text{where } x = \frac{100 - CL}{100}$$

CL = Confidence Limit in percent
r = Number of rejects
n = Number of devices
t = Duration of test

The confidence limit is the degree of conservatism desired in the calculation. The Central Limit Theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 2). The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to x^2 tables.

The number of rejects is a critical factor since the definition of rejects often differs between manufacturers. While Motorola uses data sheet limits to determine failures, sometimes rejects are counted only if they are catastrophic. Due to the increasing chance of a test not being representative of the entire population, as sample size and test time are decreased, the x^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate.

Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_0(t)e^{-\Theta/kT}$$

where R(t) = Reaction rate as a function of time and temperature

R_0 = A constant
t = Time
Θ = Activation energy in electron volts
k = Boltzman's constant
T = Temperature in degrees Kelvin

To provide time-temperature equivalents this equation is applied to failure rate calculations in the form:

$$t = t_0 e^{\Theta/kT}$$

where t = time

t_0 = A constant

The Arrhenius equation essentially states that reaction rate increases exponentially with temperature. This produces a straight line when plotted in log-linear paper with a slope expressed by Θ. Θ may be physically interpreted as the energy threshold of a particular reaction or failure mechanism. The activation energy exhibited by semiconductors varies from about 0.3 eV. Although the relationships do not prohibit devices from having poor failure rates and high activation energies, good performance usually does not imply a high Θ. Studies by Bell Telephone Laboratories have indicated that an overall Θ for semiconductors is 1.0 eV. This value has been accepted by the Rome Air Development Command for time-temperature acceleration in powered burn-in. Data taken by Motorola on Integrated Circuits have verified this number and it is therefore applied as our standard time-temperature regression for extrapolation of high temperature failure rates to temperatures at which the devices will be used (Figure 3). For Discrete products, 0.7 eV is generally applied.

To accomplish this, the time in device hours (t1) and temperature (T1) of the test are plotted as point P1. A vertical line is drawn at the temperature of interest (T2) and a line with a 1.0 eV slope is drawn through point P1.

Its intersection with the vertical line defines point P2, and determines the number of equivalent device hours (t2). This number may then be used with the x^2 formula to determine the failure rate at the temperature of interest. Assuming T1 of 125°C at t1 of 10,000 hours, a t2 of 7.8 million hours results at a T2 of 50°C. If one reject results in the 10,000 device hours of testing at 125°C, the failure rate at that temperature will be 20%/1,000 hours using a 60% confidence level. One reject at the equivalent 7.8 million device hours at 50°C will result in a 0.026%/1,000 hour failure rate, as illustrated in Figure 4.

Three parameters determine the failure rate quoted by the manufacturer: the failure rate at the test temperature, the activation energy employed, and the difference between the test temperature and the temperature of the quoted λ. A term often used in this manipulation is the "acceleration factor" which is simply the equivalent device hours at the lower temperature divided by the actual test device hours.

Every device will eventually fail, but with the present techniques in Semiconductor design and applications, the wearout phase is extended far beyond the lifetime required. During wearout, as in infant mortality, the failure rate is changing rapidly and therefore loses its value. The

parameter used to describe performance in this area is "Median Life" and is the point at which 50% of the devices have failed. There are currently only few significant wearout mechanisms: electromigration of circuit metallization, electrolytic corrosion in plastic devices and metal fatigue for Power devices.

FIGURE 3
NORMALIZED TIME-TEMPERATURE REGRESSIONS FOR VARIOUS ACTIVATION ENERGY VALUES

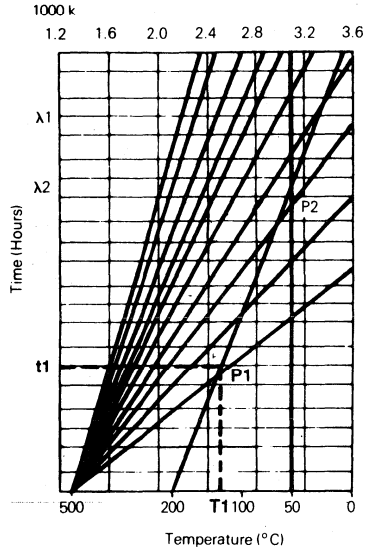
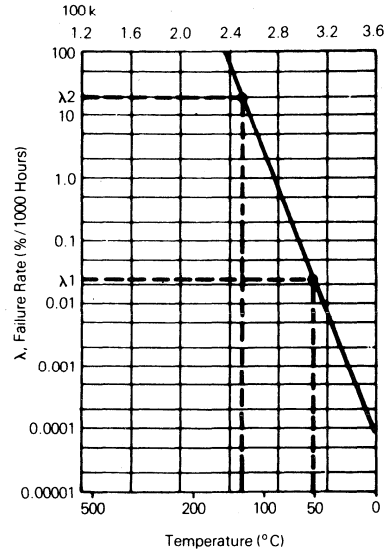


FIGURE 4
FAILURE RATE



For increased flexibility in working with a broad range of device hours, the time-temperature regression lines have been normalized to 500°C and the time scale omitted, permitting the user to define the scale based on his own requirements.

Reliability

RELIABILITY TESTS:
DEFINITION, PURPOSE AND PROCEDURES

These definitions are intended to give the reader a brief understanding of the tests currently used at Motorola for reliability checking. They also state which main failure mechanisms are accelerated by the test.

HIGH TEMPERATURE STORAGE LIFE

An environmental test where only temperature is the stress. Temperature and test duration must be specified. Usually temperature is the maximum storage temperature of the devices under test. Main failure mechanisms are metallization, bulk silicon, corrosion.

HIGH TEMPERATURE REVERSE BIAS (HTRB)

An environmental stress combined with an electrical stress whereby devices are subjected to an elevated temperature and simultaneously reverse biased. To be effective, voltage must be applied to the devices until they reach room temperature at the completion of the test. Temperature, time and voltage levels must be specified. Accelerated failure mechanisms are inversion, channeling, surface contamination.

HIGH HUMIDITY, HIGH TEMPERATURE REVERSE BIAS (H^3TRB)

A combined environmental/electrical stress whereby devices are subjected to an elevated ambient temperature and high humidity, simultaneously reverse biased for a period of time. Normally performed on a sample basis (qualification) on non-hermetic devices. The most common condition is 85°C and 85% relative humidity. More extreme conditions generally are very destructive to the chambers used. Time, temperature, humidity and voltage must be specified. This accelerated test mainly detects corrosion risks.

STEADY STATE OPERATING LIFE

An electrical stress whereby devices are forward (reverse for zeners) biased at full rated power for prolonged duration. Test is normally 25°C ambient and power is 100% of full rated. (For power devices the I/C's maximum operating Ti is used.) Duration, power and ambient, if other than 25°C, must be specified. Accelerated failure mechanisms mainly are metallization, bulk silicon, oxide, inversion, and channeling.

DYNAMIC OPERATING LIFE

An electrical stress whereby devices are alternately subjected to forward bias at full rated power or current and reverse bias.

Duration, power, duty cycle, reverse voltage ambient and frequency must be specified. Used normally for rectifiers and silicon controlled rectifiers. Failure mechanisms are essentially the same as steady state operating life.

INTERMITTENT OPERATING LIFE (POWER CYCLING)

An electrical stress whereby devices are turned on and off for a period of time. During the "on" time the devices are turned on at a power such that the junction temperature reaches its maximum rating. During "off" cycle the devices return to 25°C ambient. Duration, power, or duty cycle must be individually specified. Accelerated failure mechanisms are mainly die bonds, wire bond, metallization, bulk silicon, and oxide.

THERMAL SHOCK (TEMPERATURE CYCLING)

An environmental stress whereby devices are alternately subjected to a low and high temperature with or without a dwell time in between to stabilize the devices to 25°C ambient — the medium is usually air. Temperatures, dwell times and cycles must be specified. Failure mechanisms are essentially die bonds, wire bonds, and package.

THERMAL SHOCK (GLASS STRAIN)

An environmental stress whereby the devices are subjected to a low temperature, stabilized and immediately transferred to a high temperature. The medium is usually liquid. Failure mechanisms essentially are the same as temperature cycling.

EXAMPLE OF NEW PROCESS QUALIFICATION TESTS

Test	Condition	Duration
Operating Life	125°C, 5 V or 15 V	1,000 Hours
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours
Autoclave	121°C, 100% R.H. 15P.S.I.G.	144 Hours
High Temperature Storage	150°C	1,000 Hours
Thermal Cycle (Air to Air)	− 65°C to 150°C 5 Min Dwell	1,000 Cycles
Thermal Shock (Liquid to Liquid)	− 65°C to 150°C 5 Min Dwell	1,000 Cycles
Shock, Vibration, and Constant Acceleration	1,500G, 3 per Axis 150− 2,000 Hz, 20 g 30 kg	0.5 MS 2 Hours
Data Retention Bake (Non-Volatile Memories)	200/250°C	1,000 Hours

MECHANICAL SHOCK

A mechanical stress whereby the devices are subjected to high impact forces normally in two or more of the six orientations: X1, Y1, Z1, X2, Y2, Z2. Tests are to verify the physical integrity of the devices. G forces, pulse duration, and number of shocks and axes must be specified.

VIBRATION VARIABLE FREQUENCY

Same as Vibration Fatigue except that frequency is logarithmically varied form 100 Hz to 1 kHz and back. Number of cycles is normally four. Cycle time, amplitude and total duration must be specified. Failure mechanisms are mainly package, wire bond — this test is not applicable to molded devices.

EXAMPLE OF NEW PACKAGE QUALIFICATION TESTS

Test	Condition	Duration
Operating Life	125°C, 5 V or 15 V	1,000 Hours
Temperature Humidity Bias	85°C, 85% R.H. 5 V or 15 V	1,000 Hours
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	144 Hours
High Temperature Storage	150°C	1,000 Hours
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1,000 Cycles
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1,000 Cycles
Shock, Vibration, and Constant Acceleration	1,500 G, 3 per Axis 150−2,000 Hz, 20 g 30 kg	0.5 ms 2 Hours
Hermeticity	1.85, 10^{-8} atm cc/sec	
Visual Inspection		
Dimensions	Outline Dwg.	
Marking Permanency		
Solderability	230°C	3 Seconds
Wire Bond Strength (Post Seal)	1.5 Gram	
Die Shear		

EXAMPLE OF STANDARD RELIABILITY PROGRAM

Reliability Engineering Department	Motorola Reliability Program For:			
Test Group	**Test**	**SS**	**Frequency**	**Test Methods/Conditions**
Reliability Audit	Thermal Shock	25	1 Product Line Per Week	−25°C, +125°C. Dwell Time 5 mn, 100 Cycles
	High Temperature Reverse Bias	40		TA = 150°C, VCB = .8 VCB max. 168 hours
Life Tests	High Temperature Reverse Bias	25 (+2)	3 Product Lines Per Month	TA = 150°C, VCB = .8 VCB max. 1,000 hours
	High Temperature Storage	25 (+2)		TA = 150°C, 1,000 hours
	Steady State Life	25 (+2)		TA = 125°C, 1,000 hours
	High Humidity	25		TA = 85°C, 85% Humidity VCB = .8 VCB max. 1,000 hours
	High Temperature Reverse Bias	(+2)		
(+2) devices for correlation purpose				

Product Family	Test Conditions	Device Hours	No. Of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Non Hermetic Interface I/C's	Operating T_j = 155°C	591,552	64	1 eV	70°C	0.014
Consumer I/C's	Operating T_j = 125°C	13,082,000	39	1 eV	70°C	0.0029
DO4/DO5 Rectifier	T_j = 150°C VR = .8 BVR	798,000	5	.7 eV	70°C	0.009
Plastic Axial Diodes	T_j = 100°C VR = .8 BVR	295,000	3	.7 eV	70°C	0.21
Button Diodes	T_j = 150°C VR = .8 BVR	520,000	5	.7 eV	70°C	0.014
Small Signal Plastic Transistor	T_j = 150°C VCB = .8 BVCO	579,000	6	.7 eV	70°C	0.014
Small Signal Metal Transistor	T_j = 150°C VCB = .8 BVCBO	3,944,000	12	.7 eV	70°C	0.0039
Case 77 Power Plastic Transistor	T_j = 150°C VBC = .8 BVCBO	364,416	2	.7 eV	70°C	0.0097
TO220 Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	366,080	0	.7 eV	70°C	0.0028
TO3P Power Plastic Transistor	T_j = 150°C VCB = .8 BVCBO	297,024	3	.7 eV	70°C	0.016
TO3 Power Metal Transistor	T_j = 150°C VCB = .8 BVCBO	247,104	3	.7 eV	70°C	0.019

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
CMOS Ceramic	125°C Static Bias	6.5×10^7	11	1 EV	50°C 85°C	0.00074 0.025
CMOS Plastic	125°C Static Bias	2.1×10^8	17	1 EV	85°C	0.0088
6800 Series Plastic	125°C Dynamic Bias 5 V	2.88×10^6	47	1 EV	70°C	0.039
U.V. EPROM Life Test	125°C Dynamic Bias 5 V	434,456	3	1 EV	70°C	0.009
Data Retention	250°C Bake	519,120	3	0.7 EV	70°C	0.0075
EEPROM Life Test	125°C Dynamic Bias 5 V	917,280	25	1 EV	70°C	0.027
Data Retention	250°C	966,672	19	0.7 EV	70°C	0.020
64K DRAM	125°C Dynamic Bias 5.5 V	1.05×10^6	6	0.7 EV	70°C	0.028

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 90% Confidence
LS-TTL	125°C Static Basis −5.2 V			1.0 eV	70°C	0.0029
ECL	125°C Static Bias 5 V	61.74×10^6	7	1.0 eV	85°C	0.0189

Product Family	Test Conditions	Device Hours	No. of Failures	Activation Energy	Derated Temperature	% Per 1,000 Hours At 60% Confidence
Operational Amplifier	Operating $T_j = 135°C$	437,472	2	1 eV	70°C	0.0026
Hermetic Interface I/C's	Operating $T_j = 135°C$	718,848	4	1 eV	70°C	0.0033

The reliability approach at Motorola Semiconductors is based on designing-in reliability rather than testing for reliability only. This concept is reflected by Motorola's mandatory procedures which require product, process, and packaging qualification on three independently produced lots before any product is released to volume production. Reliability engineering approval, supported by an officially documented report, is required before any product is released to manufacturing. Tests at both maximum rated and accelerated stress levels are performed. Acceleration is important to determine how and at what stress level a new design, product process, or package would fail. This information provides an indication of which design changes can be implemented to ensure a wider and safer margin between the maximum rated stress condition and the devices stress limitation.

As well as qualifying all new products, processes, and piece-parts, each Motorola manufacturing facility operates an ongoing reliability monitor which covers all process and packaging options. This program provides a continuous up-to-date data base which is summarized in periodical reports.

Reliability statistics supporting all Motorola's Semiconductor devices can be obtained from any of the Motorola Sales Offices upon request. The present operating life test results demonstrate Motorola's reputation for producing semiconductors with reliability second to none.

The Quality organization in each facility is responsible for preparing and maintaining a Quality Manual which describes in detail the quality systems and associated Reliability and Quality Assurance organization, policies, and procedures. This manual must be appraised and ultimately approved by the appropriate approval authority.

Package Dimensions

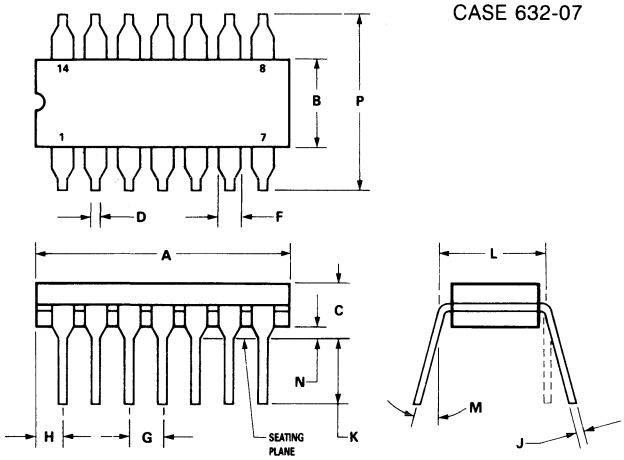
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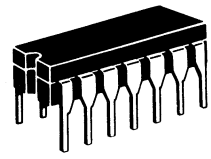
PACKAGE DIMENSIONS

The standard package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter. Surface mount packages may be special ordered by specifying the following suffixes: "D" (narrow SOIC), "DW" (wide SOIC), or "FN" (PLCC). For example, to order a quad NOR gate, use MC14001BCD. For package availability, refer to brochure BR274.

14-PIN PACKAGE

CERAMIC PACKAGE
CASE 632-07



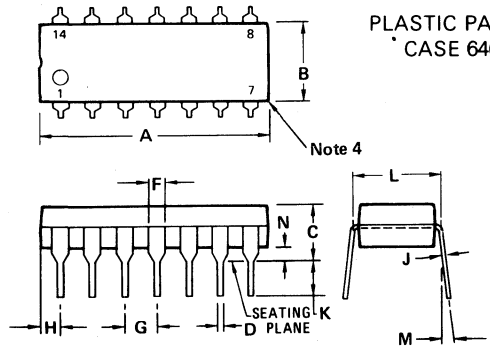


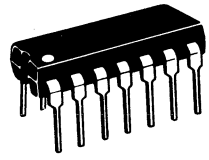
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC *		0.100 BSC *	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	4.32	0.125	0.170
L	7.62 BSC *		0.300 BSC *	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

*BSC = Basic Spacing Between Centerlines

NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 632-01 OBSOLETE, NEW STD. 632-03. SEE ISSUE "C" FOR REFERENCE.
4. DIMENSION "A" AND "B" (632-07) DO NOT INCLUDE GLASS RUN-OUT.
5. 632-06 OBSOLETE, NEW STD 632-07
6. LEADS WITHIN 0.25 mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

PLASTIC PACKAGE
CASE 646-05





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC*		0.100 BSC*	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC*		0.300 BSC*	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

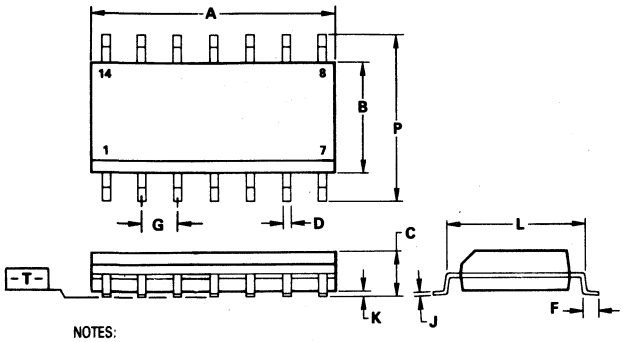
*BSC = Basic Spacing Between Centerlines

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

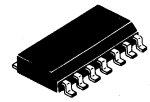
8

14-PIN PACKAGE

SOIC PACKAGE
CASE 751A



NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ A Ⓢ

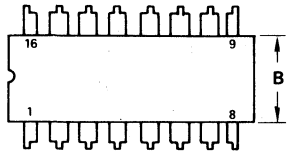


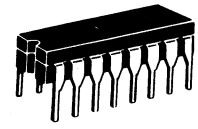
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.54	8.74	0.336	0.344
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC *		0.050 BSC *	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

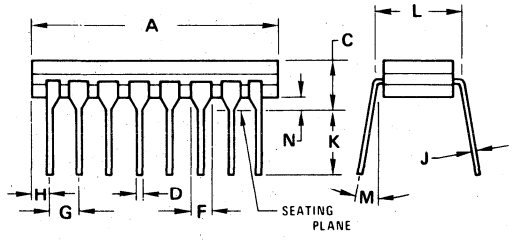
*BSC = Basic Spacing Between Centerlines

16-PIN PACKAGE

CERAMIC PACKAGE
CASE 620-08





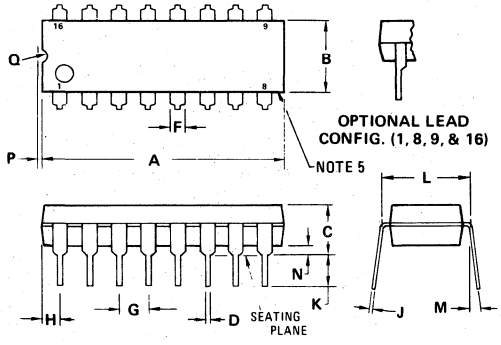


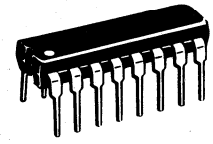
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC*		0.100 BSC*	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC*		0.300 BSC*	
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

*BSC = Basic Spacing Between Centerlines

PLASTIC PACKAGE
CASE 648-05





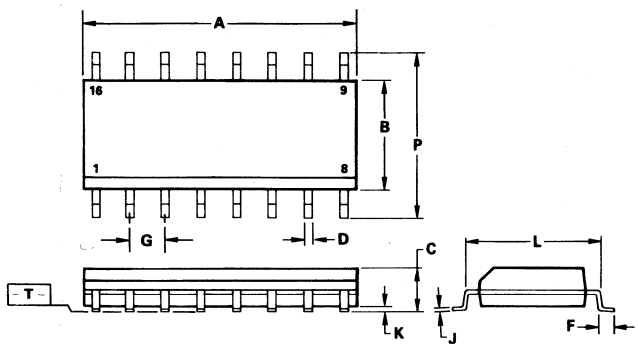
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

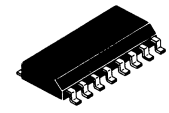
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC*		0.100 BSC*	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC*		0.300 BSC*	
M	0^0	10^0	0^0	10^0
N	0.51	1.02	0.020	0.040

*BSC = Basic Spacing Between Centerlines

16-PIN PACKAGE

SOIC PACKAGE
CASE 751B





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC *		0.050 BSC *	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

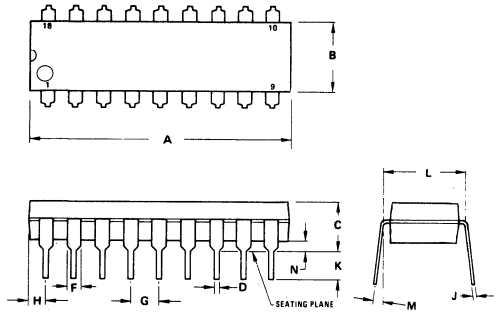
*BSC = Basic Spacing Between Centerlines

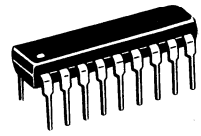
NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ A Ⓢ

8

18-PIN PACKAGE

PLASTIC PACKAGE
CASE 707-02





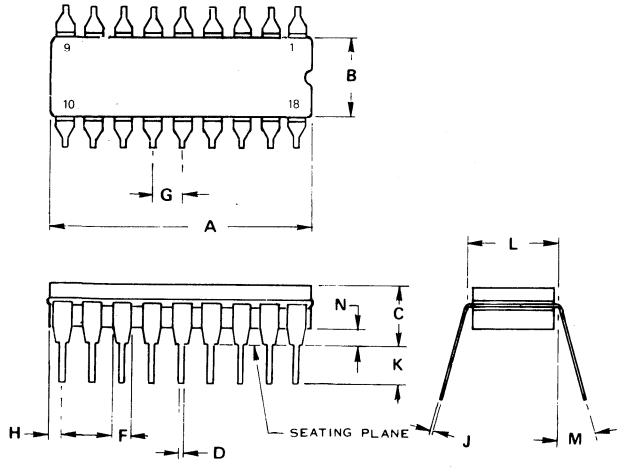
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC*		0.100 BSC*	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC*		0.300 BSC*	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

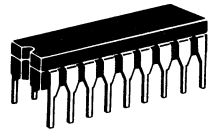
*BSC = Basic Spacing Between Centerlines

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CERAMIC PACKAGE
CASE 726-04





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC*		0.100 BSC*	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC*		0.300 BSC*	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

*BSC = Basic Spacing Between Centerlines

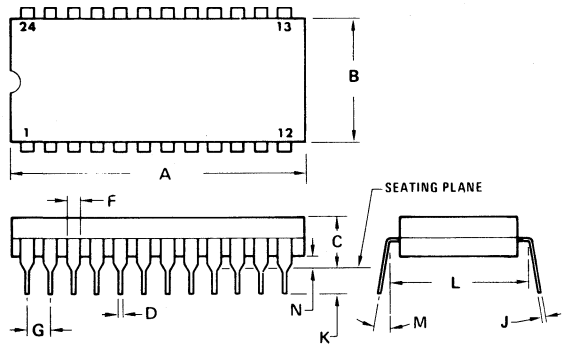
NOTES:

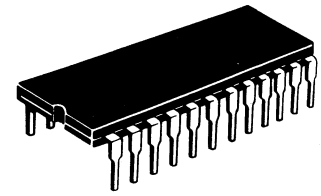
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

8

24-PIN PACKAGE

CERAMIC PACKAGE
CASE 623-05



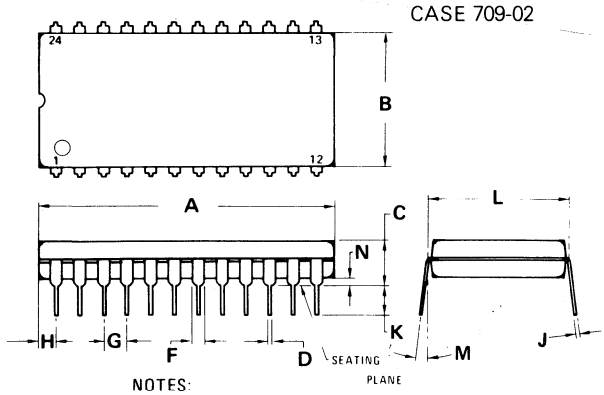


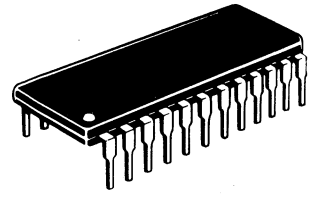
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC *		0.100 BSC *	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC *	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

*BSC = Basic Spacing Between Centerlines

PLASTIC PACKAGE
CASE 709-02





NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

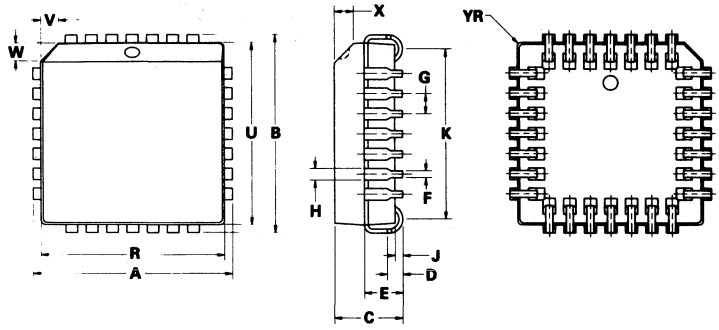
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC*		0.100 BSC*	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC*		0.600 BSC*	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

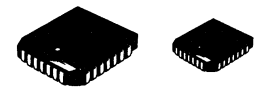
*BSC = Basic Spacing Between Centerlines

PACKAGE DIMENSIONS (Continued)

28-PIN PACKAGE

PLCC PACKAGE
CASE 776-01





NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC*		0.050 BSC *	
H	0.66	0.81	0.026	0.032
J	0.38	0.63	0.015	0.025
K	9.91	10.92	0.390	0.430
R	11.43	12.57	0.450	0.456
U	11.43	12.57	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020

*BSC = Basic Spacing Between Centerlines

8

1 Master Index

2 Product Selection Guide
Equivalent Gate Count

3 The "Better" Program

4 B and UB Series Family Data

5 CMOS Handling and Design Guidelines

6 Data Sheets

7 CMOS Reliability

8 Package Dimensions

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